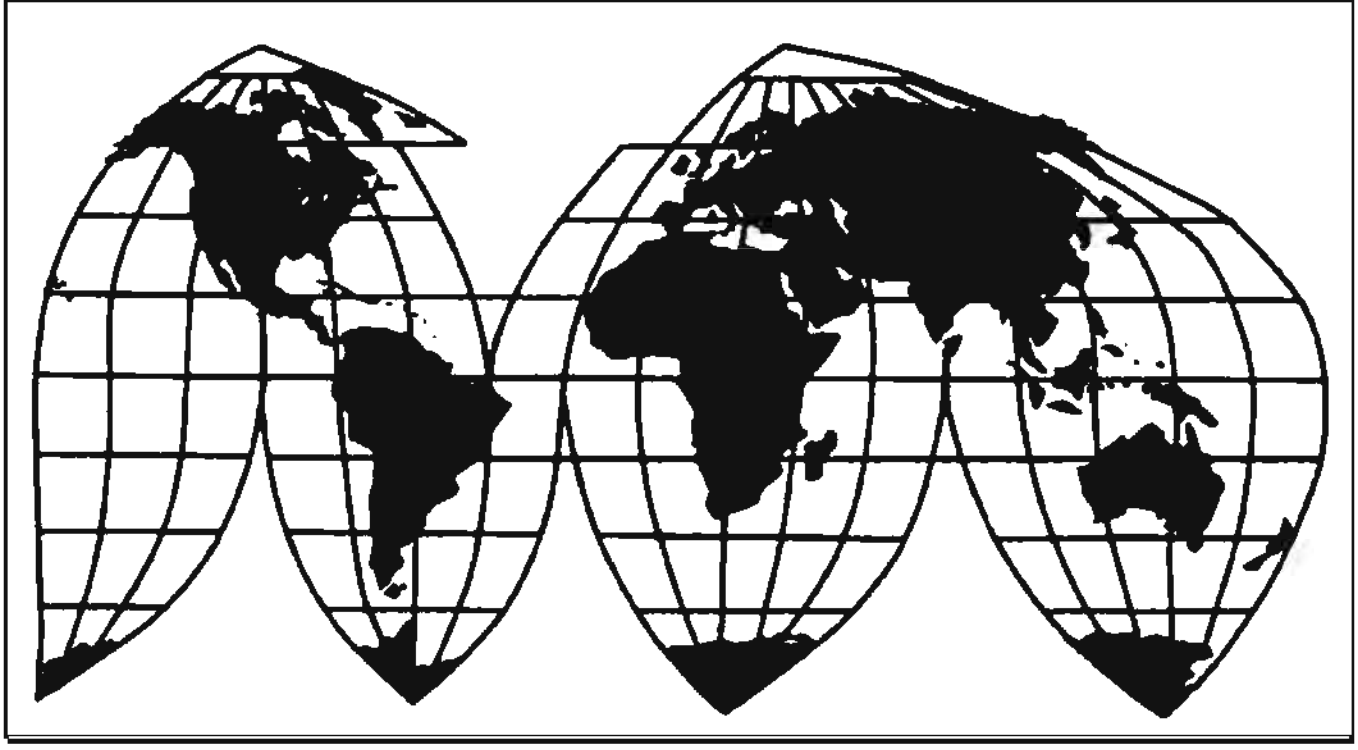
In the Matter of

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF

Investigation No. 337-TA-1089

Publication 5250 **February 2022**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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U.S. International Trade Commission

Washington, DC 20436
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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN MEMORY MODULES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-1089**

NOTICE OF THE COMMISSION'S FINAL DETERMINATION FINDING NO VIOLATION OF SECTION 337; TERMINATION OF THE INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has found no violation of section 337 of the Tariff Act of 1930, as amended. The investigation is hereby terminated.

FOR FURTHER INFORMATION CONTACT: Robert Needham, Office of the General Counsel, U.S. International Trade Commission, 500 E Street SW, Washington, DC 20436, telephone 202-205-5468. Copies of non-confidential documents filed in connection with this investigation may be viewed on the Commission's electronic docket (EDIS) at https://edis.usitc.gov. For help accessing EDIS, please email EDIS3Help@usitc.gov. General information concerning the Commission may also be obtained by accessing its Internet server at https://www.usitc.gov. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal, telephone 202-205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. of Irvine, California ("Netlist"). 82 FR 57290-91. The complaint, as supplemented, alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337, in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain memory modules and components thereof that infringe claims 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of U.S. Patent No. 9,606,907 ("the '907 patent") and claims 12-15, 17-25, 27, and 29 of U.S. Patent No. 9,535,623 ("the '623 patent"). *Id.* The Commission's notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (together, "SK hynix"). *Id.* at 57291. The Office of Unfair Import Investigations ("OUII") is also participating in this investigation. *Id.*

The Commission subsequently terminated the investigation with respect to claims 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 12-15, 17-25, 27, and 29 of the '623 patent based on Netlist's partial withdrawal of its complaint. *See* Order. No. 12 (Mar. 19, 2018), *not reviewed*, Notice (Apr. 5, 2019); Order. No. 19 (Sept. 25, 2018), *not reviewed*, Notice (Oct. 15, 2018); Order. No. 27 (Dec. 6, 2018), *not reviewed*, Notice (Dec. 21, 2018). Accordingly, at the time of the Final ID, the remaining asserted claims were claims 1-8, 10, 12, 14, and 15 of the '907 patent and claims 1-5 and 7-11 of the '623 patent.

On October 19, 2019, the ID issued a final initial determination ("Final ID") finding a violation of section 337 with respect to claims 6 and 12 of the '907 patent. Final ID at 164-65. The ID found that Netlist showed that SK hynix infringes claims 1-8, 10, 12, 14, and 15 of the '907 patent, but failed to show that SK hynix infringed any claim of the '623 patent. The ID also found that SK hynix showed that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious, but failed to show the invalidity of claims 6 and 12. Finally, the ID found that Netlist satisfied the domestic industry requirement with respect to the '907 patent, but did not satisfy the domestic industry requirement with respect to the '623 patent.

On January 31, 2020, the Commission determined to review the final ID in part. Specifically, the Commission determined to review the following issues: (1) the construction of the limitation "receive" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (2) the construction of the limitation "produce first module control signals and second module control signals in response to the set of input address and control signals" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (3) the domestic industry requirement with respect to both of the '623 and '907 patents; and (4) the findings with respect to both of the '623 and '907 patents regarding whether SK hynix showed that Netlist violated its obligations, if any, to offer a license on reasonable and non-discriminatory (RAND) terms. The Commission determined not to review any other findings presented in the Final ID, including the finding of no violation with respect to the '623 patent based on Netlist's failure to show infringement and the technical prong of the domestic industry requirement.

The Commission also sought briefing from the parties on four issues and on remedy, bonding and public interest. On February 14, 2020, Netlist, SK hynix, and OUII filed their initial submissions in response to the Commission's request for briefing. On February 24, 2020, Netlist, SK hynix, and OUII filed their reply submissions in response to the Commission's request for briefing. The Commission also received a submission from third-party Hewlett Packard Enterprise Company.

Having examined the record of this investigation, including the Final ID, the petitions, responses, and other submissions from the parties, the Commission has determined that Netlist has failed to show a violation of section 337. The Commission has determined to construe "receive" to occur when a signal or data reaches a circuit element's input, and, under that construction, finds that Netlist failed to satisfy that

limitation for infringement and the technical prong of the domestic industry requirement for any asserted claim of the ’907 patent. The Commission has also determined to construe the limitation “produce first module control signals and second module control signals in response to the set of input address and control signals” to require a response to at least one input address signal and at least one control signal, and, under that construction, finds that Netlist failed to satisfy that limitation for infringement and the technical prong of the domestic industry requirement for any asserted claim of the ’907 patent. The Commission further finds that, regardless of the constructions for these limitations, Netlist failed to provide sufficient evidence on its domestic industry products to satisfy the technical prong of the domestic industry requirement. Additionally, the Commission has determined to take no position on whether Netlist satisfied the economic prong of the domestic industry requirement for either the ’907 or ’623 patents. The Commission also affirms the Final ID’s finding that SK hynix showed that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious. Finally, the Commission has determined to reverse the ALJ’s findings that the ’907 patent is essential to a JEDEC standard and that the JEDEC Patent Policy is unenforceable, has determined to affirm the ALJ’s finding that the ’623 patent is not shown to be essential to a JEDEC standard, and has determined to vacate all other finding relating to obligations to license on reasonable and nondiscrimatory terms.

Accordingly, the Commission finds no violation of section 337 based on Netlist’s failure to establish infringement and the technical prong of the domestic industry requirement, and on SK hynix’s showing that claims 1-5, 7, 8, 10, 14, and 15 of the ’907 patent are invalid as obvious. The Commission’s determinations are explained more fully in the accompanying Opinion. All other findings in the ID under review that are consistent with the Commission’s determinations are affirmed. The investigation is hereby terminated.

The authority for the Commission’s determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. 1337), and in part 210 of the Commission’s Rules of Practice and Procedure (19 CFR part 210).

By order of the Commission.

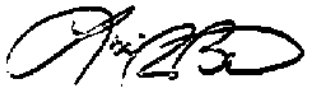
Lisa R. Barton
Secretary to the Commission

Issued: April 7, 2020

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **Inv. No. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by via EDIS the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on **April 7, 2020**.



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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN MEMORY MODULES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-1089**

COMMISSION OPINION

The Commission has determined that there has been no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, with respect to U.S. Patent Nos. 9,606,907 ("the '907 patent") and 9,535,623 ("the '623 patent") on review of the Final Initial Determination ("ID") of the presiding administrative law judge ("ALJ"). This opinion sets forth the Commission's reasoning in support of that determination.

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. of Irvine, California ("Netlist"). 82 Fed. Reg. 57290-91. The complaint alleged violations of section 337 in the importation into the United States, the sale for importation, and the sale after importation within the United States of certain memory modules and components thereof by reason of infringement of one or more of claims 1-8, 10, 12, 14-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 1-5, 7-15, 17-25, 27, and 29 of the '623 patent. *Id*. at 57291. The notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (collectively, "SK hynix"). *Id.* The Office of Unfair Import Investigations ("OUII") is a party to the investigation. *Id.*

The Commission subsequently terminated the investigation with respect to certain claims based on Netlist's withdrawal of those allegations. Specifically, the Commission terminated the investigation with respect to claims 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 12-15, 17-25, 27, and 29 of the '623 patent based on Netlist's partial withdrawal of its complaint. *See* Order. No. 12 (Mar. 19, 2018), *not reviewed*, Notice (Apr. 5, 2019); Order. No. 19 (Sept. 25, 2018), *not reviewed*, Notice (Oct. 15, 2018); Order. No. 27 (Dec. 6, 2018), *not reviewed*, Notice (Dec. 21, 2018). Accordingly, at the time of the Final ID, the remaining asserted claims were claims 1-8, 10, 12, 14, and 15 of the '907 patent and claims 1-5 and 7-11 of the '623 patent.

On October 19, 2019, the ALJ issued the Final ID finding a violation of section 337 with respect to claims 6 and 12 of the '907 patent. Final ID at 164-65. The ALJ found that Netlist showed that SK hynix infringed claims 1-8, 10, 12, 14, and 15 of the '907 patent, but failed to show that SK hynix infringed any claim of the '623 patent. *Id.* The ALJ also found that SK hynix showed that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious, but failed to show the invalidity of claims 6 and 12. *Id.* at 165. Finally, the ALJ found that Netlist satisfied the domestic industry requirement with respect to the '907 patent, but did not satisfy the domestic industry requirement with respect to the '623 patent.

On October 29, 2019, the Commission sought submissions from the public regarding the public interest raised by the ALJ's recommend limited exclusion order. 84 Fed. Reg. 57884. The Commission received submissions on the public interest from SK hynix; Netlist; the U.S. Federal Trade Commission; Congressman Ted Budd; Congressman John Carter; Congresswoman Anna G. Eshoo; Congressman Henry C. Johnson; Congresswoman Katie Porter; Ericsson, Inc.; Dell, Inc.; Hewlett Packard Enterprise; JEDEC; ACT The App

Association and several individuals—Cameron Bopp, James Laipple, K. Elbarjaj, Franklin P. Stone, and Stuart Douglass.

On November 4, 2019, SK hynix[1] and OUII[2] filed petitions for review. SK hynix petitioned for review of several of the ALJ's findings on claim construction, infringement, the domestic industry, and invalidity with respect to the '907 patent, and also challenged several of the ALJ's rulings on its Reasonable and Non-Discriminatory ("RAND") defenses and estoppel due to *inter partes* review ("IPR") proceedings at the Patent Trial and Appeal Board ("PTAB") regarding the '907 patent. OUII petitioned for review of several of the ALJ's findings on claim construction, infringement, the domestic industry, and invalidity with respect to the '907 patent. Also on November 4th, Netlist filed a contingent petition for review on several invalidity issues and the ALJ's recommendation on a cease and desist order with respect to the '907 patent.[3] No one petitioned for review with respect to the '623 patent findings. On November 12, 2019, the parties filed responses to each other's petitions.[4]

On January 31, 2020, the Commission determined to review the following issues: (1) the construction of the limitation "receive" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (2) the construction of the limitation "produce first module control signals and second module control signals in response to the set of input address

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[1] Respondents' Petition for Review (Nov. 4, 2019) ("SK hynix Pet.").

[2] The Office of Unfair Import Investigation's Petition for Review in Part of the Final Initial Determination (Nov. 4, 2019) ("OUII Pet.").

[3] Complainant Netlist, Inc.'s Contingent Petition for Review of the Initial Determination (Nov. 4, 2019) ("Netlist Pet.").

[4] Complainant Netlist, Inc.'s Omnibus Response to Respondents' and Staff's Petitions for Review (Nov. 12, 2019) ("Netlist Resp."); Respondents' Combined Response to (1) Petition for Review by the Office of Unfair Import Investigations and (2) Contingent Petition for Review by Complainant (Nov. 12, 2019) ("SK hynix Resp."); Response of the Office of Unfair Import Investigations to the Private Parties' Petitions for Review of the Initial Determination on Violation of Section 337 (Nov. 12, 2019) ("OUII Resp.").

and control signals" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (3) the domestic industry requirement with respect to both of the '623 and '907 patents; and (4) the findings with respect to both of the '623 and '907 patents regarding whether SK hynix showed that Netlist violated its obligations, if any, to offer a license on reasonable and non-discriminatory terms. The Commission did not determine to review the ALJ's conclusion that there was no violation of section 337 with respect to the '623 patent based on a lack of infringement. The Commission also sought briefing on certain issues under review and on remedy, the public interest, and bonding.

On February 14, 2020, the Commission received initial submissions from Netlist, SK hynix, and OUII.[5] The Commission also received a submission on the public interest from third-party Hewlett Packard Enterprise Company. On February 24, 2020, the Commission received reply submissions from Netlist, SK hynix, and OUII.[6]

B. The '907 Patent

The '907 patent is entitled "Memory Module with Distributed Data Buffers and Method of Operation" and claims priority as a continuation of an application filed on April 15, 2010 and as a continuation-in-part of an application that was filed on July 16, 2009. JX-2001 ('907 patent). The patent generally describes a memory module in which a data buffer circuit reduces the overall electrical load by transmitting command data only to the selected memory device while not transmitting the command data to non-selected devices. The only independent claim at issue, claim 1, reads as follows, with the terms at issue highlighted in bold:

[5] These documents will be referred to as "Netlist Init. Sub.," "SK hynix Init. Sub.," and "OUII Init. Sub.," respectively.

[6] These documents will be referred to as "Netlist Rep. Sub.," "SK hynix Rep. Sub.," and "OUII Rep. Sub.," respectively.

1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to **produce first module control signals and second module control signals in response to the set of input address and control signals**;

a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while **the second memory devices do not output or receive any data associated with the memory read or write command**;

M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and

> between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

JX-2001 ('907 patent) at 19:2-58.

C. The Accused Products

Netlist accused many models of SK hynix's JEDEC-compliant Double Data Rate 4 ("DDR4") Load-Reduced Dual In-Line Memory Module ("LRDIMM") products of infringing the '907 patent. Final ID at 7-8. The specific accused models are listed in a table on pages 7-8 of the Final ID. *Id.*

D. The Domestic Industry Products

The asserted domestic industry articles are Netlist's 16 GC 2Rx4 DDR HV-LRDIMM and 32GB 2Rx4 DDR HV-LRDIMM. Final ID at 10. These products are specific model numbers of Netlist's Field Programmable Gate Array ("FPGA") HybriDIMM product. *Id.* at 139. Netlist has since transitioned to its Application-Specific Integrated Circuit ("ASIC") HybriDIMM product, but expressly stated that it was not relying upon that product for the domestic industry. *Id.* at 139 n.13.

II. STANDARD

With respect to the issues under review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge." 19 C.F.R. § 210.45(c). The Commission also "may take no position on specific issues or portions of the initial determination," and "may make any finding or

conclusions that in its judgment are proper based on the record in the proceeding." *Id.*

III. DISCUSSION OF THE ISSUES ON REVIEW

The Commission determines to make the findings, conclusions, and supporting analysis set forth below. Any findings, conclusions, and supporting analysis in the ID that are under review and are not inconsistent with the Commission's analysis and conclusions below are hereby affirmed and adopted.

A. The "Receive" Limitation in the Asserted Claims of the '907 Patent

For the reasons set forth below, the Commission determines to construe "receive" according to its plain and ordinary meaning, and thus finds that a circuit element "receives" a signal or data when the signal or data reaches a circuit element's input. Under that construction, the Commission finds that Netlist failed to establish infringement or the technical prong of the domestic industry requirement for any asserted claim of the '907 patent, and affirms under modified reasoning the ALJ's finding that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious.

1. Claim Construction

a. Overview

The issue under review concerns the construction of the term "receive." The term "receive" appears several times in the asserted claims, but most notably in the following limitation of claim 1:

> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or **receive** each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or **receive** any data associated with the memory read or write command

'907 patent, claim 1 (emphasis added). Claim 1 uses the term "receive" similarly elsewhere—"a

module control circuit configured to receive a set of input address and control signals . . .” and “M buffer circuits each configured to receive the second module control signals . . .” *Id.*

During claim construction, the parties disputed the construction of the term “output or receive . . . data” / “do not output or receive any data.” Netlist contended that the term should be construed as “transmit or acquire data” / “do not transmit or acquire data.” SK hynix argued that the term should be construed as its plain and ordinary meaning, but with a complex understanding as to what the plain and ordinary meaning is. OUII argued that the term should be construed as “non-selected devices do not receive any data or send any data associated with the memory controller read/write command.”

Judge Pender, who presided over the claim construction hearing, acknowledged that the ’907 patent used “receive” consistent with its plain and ordinary meaning. Order No. 17, at 32 (Aug. 24, 2018). He noted that SK hynix’s claim construction was persuasive because “it revolves around a plain and ordinary meaning of ‘receive’—a circuit element ‘receives’ a signal when that signal reaches one of the circuit element’s inputs,” and because it is also consistent with the specification. *Id.* The ALJ further explained that “the ’907 patent does not expressly define what is meant by ‘output’ or ‘receive’” and acknowledged that the patent uses “receive” in a variety of contexts, which “support[s] the idea that the ’907 patent uses ‘output’ and ‘receive’ according to general, plain and ordinary meanings.” *Id.*

The ALJ, however, ultimately adopted Netlist’s proposed construction of “output or receive” as “transmit or acquire,” “even though I find it may not match the plain and ordinary meaning of ‘output’ and ‘receive.’” *Id.* at 25. Generally, the ALJ favored Netlist’s argument that the claims covered a “straight line” arrangement (in which the first and second memory devices share data lines from their respective buffer circuits) over SK hynix’s argument that the

claims required a "fork-in-the-road" arrangement (in which the first and second memory devices have separate data lines from their respective buffer circuits). *Id.* at 25. The ALJ relied upon unasserted and unargued claim 30, which required the limitation "first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command," and found that the "by receiving" language implied that "receiving" is an action performed by the memory devices rather than the result of an external act. *Id.* at 27.

Chief Judge Bullock, who took over the investigation and presided over the hearing and issued the Final ID, further explained the meaning of "receive" in the Final ID. He stated that "[t]he parties are effectively in agreement that Order No. 17 construed 'receive' as 'acquire,' and that 'acquire' was understood in that order as meaning 'the first stage of a write operation.'" Final ID at 92. Accordingly, between the findings of Judge Pender and Chief Judge Bullock, the term "receive" has been construed to mean "a first stage of a write operation."

b. Petition and Response

In its petition for review, SK hynix argued that claim terms are generally given their plain and ordinary meaning, and thus the ALJ erred by failing to give "receive" its plain and ordinary meaning that was expressly set forth in Order No. 17—"a circuit element 'receives' a signal when that signal reaches one of the circuit element's inputs." SK hynix Pet. at 12. SK hynix argued that the plain and ordinary meaning is consistent with the specification, and that the ALJ's reliance on the unasserted and unbriefed claim 30 does not apply to the claimed invention of the asserted claims. *Id.* at 12-18.

Netlist argued that SK hynix never previously argued to construe the term "receive" on its own, and therefore waived the above argument by failing to present it to the ALJ. Netlist

Resp. at 7-11, 17. According to Netlist, Judge Pender properly construed "receive" to mean "acquire" in the context of the '907 patent, *id.* at 11-14, and Chief Judge Bullock properly applied the construction to find infringement, *id.* at 14-15.

OUII argued that the ALJ's claim construction should not be reviewed. OUII Pet. at 29-35. While OUII believed that the '907 patent is limited to a selective buffer circuit based on repeated disclaimers made during prosecution, OUII believed that concept can be incorporated by reviewing the construction of "buffer circuit" only. *Id.*

c. Analysis

While the parties' claim construction arguments focused on the contrast of terms not found in the patent (*i.e.*, "straight line" versus "fork-in-the-road"), the Commission finds that the parties contested whether this limitation should be given its plain and ordinary meaning. In claim construction, "the words of a claim are generally given their ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). The exceptions are when "the patentee sets out a definition and acts as his own lexicographer" or when "the patentee disavows the full scope of a claim term." *Thorner v. Sony Comput. Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Here, as discussed above, Judge Pender found that the patentee did not define "receive" and that the plain and ordinary meaning of "receive" in the context of the '907 patent is that "a circuit element 'receives' a signal when that signal reaches one of the circuit element's inputs." Order No. 17 at 32. No party disputed Judge Pender's characterization of the plain and ordinary meaning of "receive." Accordingly, the Commission has determined to adopt Judge Pender's recitation of the plain and ordinary meaning of "receive" and construe "receive" to occur when a signal or data reaches a circuit element's input.

Netlist argues that "receive" should be construed as "acquire" based on the context of the '907 patent and the skill in the art, but Netlist fails to explain why the specification or skill in the art would support construing "receive" as "acquire." *See* Netlist Resp. at 11-14. As the ALJ noted, the specification does not give any special meaning to "receive," and at times, the specification uses "receive" in exactly the plain and ordinary meaning described by Judge Pender. *See* '907 Patent at 16:3-21 (describing "control logic circuit 502 receives, for example, an 'enable A' signal . . ." and "data signals . . . are received at the first or second terminals Y1, Y2 . . ."). Moreover, claim 1 recites "receive" four times, and it would be inconsistent to construe two instances of "receive" to mean "acquire" and the other two instances to mean something else. *See, e.g.*, *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001) ("[A] claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent.").

Moreover, interpreting "receive" to have its plain and ordinary definition is consistent with the specification of the '907 patent. The specification explains that, under prior art systems, a memory controller communicated read and write commands to all memory devices even though each command was intended for only one selected memory device. JX-2001 ('907 Patent) at 4:56-61; 5:7-13. Under these prior art systems, adding more memory devices to increase memory space required exponentially more command signals, which in turn caused heavy loads on the system that reduced speed, increased heat dissipation, caused signal propagation delay, necessitated asynchronous behavior, and created a need for extensive modification. *Id.* at 4:7-35; 5:14-34; 6:33-55; 7:6-34. The '907 patent solved that problem through "load-reduced memory modules" that selectively send commands only to the selected

memory device while sending no commands to nonselected memory devices.[7] In other words, in the described invention of the '907 patent, the system does not send commands to nonselected memory devices, so the nonselected memory devices never "receive" a signal or data on their circuit element's inputs. The Commission's construction of "receive" is therefore consistent with the specification.

Netlist's proposed construction, on the other hand, would allow the system to send signals to both selected and nonselected memory devices as long as only the selected memory devices acted upon the command. Such a system, however, is akin to prior art systems and defeats the purpose of the invention of the '907 patent. Thus, the Commission declines to adopt Netlist's construction of "receive" to mean "acquire."

2. Infringement

The Commission finds that the accused products do not infringe any asserted claim of the '907 patent under the Commission's ordinary language construction of "receive." The asserted claims of the '907 patent require that the second, nonselected memory devices "do not output or receive any data associated with the memory read or write command." The Final ID expressly found that data signals are received on the input pins of nonselected memory devices in the accused products:

> The parties' experts are in agreement that, during a write operation, the **incoming data signal lands on the input pins of all Accused Product memory devices regardless of whether they are selected (i.e., targeted) or no**t—specifically, the input pin of a RCVRS

[7] *See id.* at Abstract (referring to "enabling data communication" to one memory device and "isolating at least one second memory device"); *id.* at 2:47-59 and 8:32-44 (referring to "selectively allowing or inhibiting data transmission" among the memory devices); *id.* at 2:63-66 (referring to "circuits configured to selectively isolate the plurality of memory devices from the system memory controller"); *id.* at 11:27-12:5 (referring to a circuit that "selectively switches between two or more memory devices . . . so as to operatively couple at least one selected memory device . . . to the system memory controller").

> circuit. (RX-3869C at Q/A 35, 68, 70; see CX-2003C at Q/A 388, 405)

Final ID at 92 (emphasis added). The Commission finds that the parties' experts agreed that the alleged first and second memory devices are connected by a shared data bus, and thus the same read/write command data signals arrive at the input of both memory devices' RCVRS circuit regardless of whether or not the memory device is selected. RX-3869C (Subramanian RWS) at Q/A 35, 68, 70; CX-2003C (Levitt DWS) at Q/A 401, 405, 408. Accordingly, because the evidence shows that the accused second memory devices do receive "data associated with the memory read or write command" on their circuit inputs, the Commission finds that the accused products do not infringe any of the asserted claims of the '907 patent.

3. Domestic Industry

The technical prong of the domestic industry requirement involves an examination of "whether the industry produces articles covered by the asserted claims," which "is essentially the same as that for infringement, *i.e.*, a comparison of the domestic products to the asserted claims." *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). Netlist asserts that the domestic industry must rise or fall with infringement; on that basis, the Commission finds that Netlist also failed to establish the technical prong of the domestic industry requirement as to the '907 patent based on its failure to establish infringement. Additionally, for reasons discussed *infra*, the Commission finds that Netlist failed to provide sufficient evidence to satisfy the technical prong of the domestic industry requirement as to the '907 patent.

4. Invalidity

The Commission finds that its construction of "receive" does not alter the Final ID's conclusions that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious. The ALJ found that these claims are invalid as obvious in light of the Quad Bank Memory ("QBM")

prior art, which is a series of technical documents regarding the creation of two models of QBM products. Final ID at 116-29. With respect to the above "receive" limitation, the ALJ found that the limitation was satisfied based on Dr. Subramanian's testimony. *Id.* at 121-23. Dr. Subramanian testified that "[a] Skilled Artisan would have also understood that it was obvious at the time to use isolation switches to disconnect inactive memory devices from a shared data bus," and demonstrated that the QBM products used DDR1 SDRAM devices and that the relevant contemporary JEDEC standard described such use of isolation switches. RX-2006C (Subramanian DWS) at Q/A 1052-53. In other words, Dr. Subramanian testified that a person of ordinary skill in the art would have found it obvious to use isolation switches to ensure that the nonselected memory device did not receive data associated with read and write commands. Accordingly, the Commission's modification to the construction of "receive" does not change the ALJ's invalidity result.

B. The "Produce First Module Control Signals and Second Module Control Signals in Response to the Set of Input Address and Control Signals" Limitation in the Asserted Claims of the '907 Patent

For the reasons set forth below, the Commission determines to construe the limitation "produce first module control signals and second module control signals in response to the set of input address and control signals" to require a response to at least one input address signal and at least one control signal, but without any requirement that any specific module control signal be based on both input address signals and control signals. Under that construction, the Commission finds that Netlist failed to establish infringement or the technical prong of the domestic industry requirement for any asserted claim of the '907 patent, and affirms under modified reasoning the ALJ's finding that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious.

1. Claim Construction

a. Overview

All of the asserted claims of the ’907 patent require the limitation “produce first module control signals and second module control signals in response to the set of input address and control signals.” In the Final ID, the ALJ found that the language “in response to the set of input address and control signals” is satisfied by a response to solely input address signals or by a response to solely control signals, as “a response to any one of those signals is a response to the set.” Final ID at 77.

b. Petition and Response

SK hynix argued in its petition that the plain language of the claim requires that each of the first module control signals and second module control signals must be based on both input address signals and control signals. SK hynix Pet. at 48-50. Netlist and OUII argued that the ALJ correctly construed the term. Netlist Resp. at 48-50; OUII Resp. at 22-23.

c. Analysis

When a claim involves commonly used terms, claim construction “involves little more than the application of the widely accepted meaning of commonly understood words.” *Philips*, 415 F.3d at 1314. Here, the language “set of input address and control signals” requires at least one input address signal and at least one control signal, because otherwise there is no “set” of input address and control signals. Consequently, the claim language that calls for the production of module control signals “in response to the set of input address and control signals” requires that those module control signals be produced in response to at least one input address signal and at least one control signal. This construction is consistent with the portions of the specification referring to the production of signals in response to both address and control signals. JX-2001 (’907 patent) at 15:59-64 (“address and control signals pass from the memory controller 420 to

the control circuit 430 which produces controls sent to the logical circuitry 502 . . . ."); id. at 17:57-18:59 (same). Accordingly, the Commission finds that the limitation "produce first module control signals and second module control signals in response to the set of input address and control signals" requires producing first module control signals and second module control signals in response to at least one input address signal and at least one control signal.

Netlist contends that the limitation should be construed to be satisfied if the module control signals are produced in response to either input address signals or control signals. Netlist Resp. at 48-50. That interpretation, however, describes a response to address signals or a response to control signals, not a response to a "set" of address and control signals as required by the claims. The Commission rejects Netlist's attempt to improperly rewrite the claim language.

SK hynix contends that the claim language requires that the first module control signals and the second module control signals each be based on both at least one address signal and at least one control signal. SK hynix Init. Sub. at 5-7. That construction is too restrictive. While the claim language does require that the production be in response to "a set of input address and control signals," it does not require that any specific module control signal be based on both input address and control signals. Accordingly, while the Commission finds that this limitation requires a response to at least one input address signal and at least one control signal, the limitation does not require any specific module control signal be produced in response to both input address signals and control signals.

2. Infringement

Under the construction set forth above, the Commission finds that the accused products do not infringe any asserted claim of the '907 patent. The asserted claims of the '907 patent impose the following requirements on the "first module control signals:"

- "produce first module control signals and second module control signals in

response to the set of input address and control signals;" and

- "in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command."

In other words, while the "first module control signals" must be produced as set forth above, the "first module control signals" must also result in a response in which the first memory devices output or receive command signals while the second memory devices do not output or receive command signals.

Netlist, however, failed to show that any alleged "first module control signals" satisfy all of these limitations. First, although Netlist demonstrated that the accused products produce an inverted address signal in response to an input address signal, Netlist failed to show that the accused products respond to that inverted address signal by having first memory devices output or receive command signals while second memory devices do not. Second, although Netlist demonstrated that the accused products contain a component that has a mode that produces signals in response to control signals, Netlist failed to show that the accused products use that mode. Each of these points are discussed in more detail below.

First, although Netlist showed that the accused products invert certain address signals, Netlist never explained how the accused products use those inverted address signals, and thus failed to explain how the inverted address signals satisfied the remainder of the limitations of the claim. Netlist's only alleged use of "input address signals" to create an alleged "first module control signals" is through a process called "address inversion." CX-2003C (Levitt DWS) at Q/A 362-63. Netlist's expert, Dr. Levitt, testified that the JEDEC RCD standard states that the RCD component receives an address signal, and then outputs the address signal to the A-Side DRAM device and outputs the inverted address signal to the B-Side DRAM device. *Id.* Inverting an

address signal could be viewed as producing a signal in response to an input address signal.

The claims, however, are not satisfied by the mere production of "first module control signals" based on an input address signal. Rather, as shown above, the "first module control signals" must also result in a response in which the first memory devices output or receive command signals while the second memory devices do not. Netlist failed to present evidence on whether the accused products use the inverted address signal at all, let alone how the inverted address signal is used so that the first memory devices output or receive command signals while the second memory devices do not. Netlist Initial Post-Hearing Br. at 27, 35 (referring to address inversion for the production of "first module control signals," but failing to address output inversion for later limitations); CX-2003C (Levitt DWS) at Q/A 362-63, 382 (same); Netlist Reply Post-Hearing Br. (containing no references to address inversion).

Thus, while Netlist may have explained how the inverted address signal is produced based on an input address signal, Netlist did not explain how a response to the inverted address signal causes the first memory devices to output or receive data while the second memory devices do not output or receive data. Because both features are required to constitute "first module control signals" within the meaning of the asserted claims, Netlist failed to demonstrate that address inversion satisfies the production of "first module control signals." Accordingly, there is no evidence that any alleged "first module control signal" or "second module control signal" in the accused products is produced in response to input address signals, and thus there is no evidence that the limitation "to produce first module control signals and second module control signals in response to the set of input address and control signals" is satisfied.

Second, although Netlist identified a mode in a component of the accused products that allegedly produces "first module control signals" in response to control signals, Netlist failed to

show that the accused products use that allegedly infringing mode. Other than the "address inversion" discussed above, the only alleged "set of input address and control signals" are control signals used in a certain mode described in the JEDEC Registering Clock Driver ("RCD") specification—Encoded QuadCS Mode. CX-2003C (Levitt DWS) at Q/A 360-61. The RCD is a component of the accused products, and the JEDEC RCD standard explains that the RCD has "three basic modes of operation"—"Direct DualCS mode" (the "normal operating mode"), "Direct QuadCS mode," and "Encoded QuadCS mode," but Netlist only accuses the Encoded QuadCS mode of infringement. *Id.* at Q/A 360 (quoting CX-0417). Netlist, however, failed to analyze the accused products or the domestic industry products to determine whether those products utilize Encoded QuadCS Mode. Products do not necessarily use every feature of each of its components, so Netlist's failure to show that the accused products use Encoded QuadCS mode has created an absence of record evidence on the issue. Accordingly, there is no record evidence that the accused products produce first module control signals in response to chip-select signals in Encoded QuadCS mode, and therefore none of Netlist's alleged "first module control signals" satisfy the limitations of the claim.

Netlist contends that its apparatus claims cover what a device is rather than what a device does, and that it has no obligation to show that the accused products implement Encoded QuadCS mode. Netlist Rep. Sub. at 4. But the mere fact that a JEDEC standard requires that the RCD component be able to implement Encoded QuadCS mode does not necessarily mean that every device incorporating that RCD component will utilize Encoded QuadCS mode. Accordingly, while compliance with the JEDEC standard may suggest that the RCD component is capable of operating in three modes, including Encoded QuadCS mode, Netlist has not established that the accused products have been enabled to operate in each of the three modes,

and more particularly in the Encoded QuadCS mode. Therefore, Netlist has not shown that this claim limitation is met by the accused products.

3. Domestic Industry

Netlist contends that its domestic industry products practice the asserted claims for the same reasons that the accused products infringe. 2003C (Levitt DWS) at Q/A 290, 633. But Netlist also failed to establish that its domestic industry products use address inversion or Encoded QuadCS mode as required by the asserted claims of the '907 patent. CX-2003C at Q/A 637-38 (failing show that Encoded QuadCS mode is used in the accused products); *id.* at Q/A 639-40, 651-711 (describing address inversion, but failing to describe how address inversion is used in the remainder of the claim). Accordingly, Netlist failed to demonstrate the technical prong of the domestic industry requirement as to the '907 patent for the same reasons that it failed to demonstrate infringement. Additionally, for reasons discussed *infra*, the Commission finds that Netlist failed to provide sufficient evidence to satisfy the technical prong of the domestic industry requirement.

4. Invalidity

The Commission finds that its construction of "produce first module control signals and second module control signals in response to the set of input address and control signals" does not alter the Final ID's conclusions that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious in light of the QBM prior art. The ID concluded that SK hynix showed that it would have been obvious to produce module control signals based on a set of address and control signals. Final ID at 119-23. The ID relied on the testimony of Dr. Subramanian, who testified that it would have been obvious to use a buffer with the QBM reference to produce control module signals based on a set of address and control signals. RX-2006C (Subramanian DWS) at Q/A 1049. Dr. Subramanian further testified it would have been obvious to combine the QBM

prior art with a rank multiplication configuration, which involves using both a chip-select and a decoded address signal to increase memory space, and thus produce a first module control signal in response to both input address and control signals. *Id.* He further testified that it would have been obvious to combine that QBM reference with module control functionality, which would result in the second module control signals for the QBM switches to be produced in response to both input address and control signals. *Id.* In other words, the ID relied upon evidence showing that it would have been obvious to produce each of the first and second module control signals in response to both input address and control signals, so the Commission's modification to this construction of "produce…" does not change the ALJ's invalidity result. Accordingly, the Commission affirms the ID's finding that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious in light of QBM based on the modified claim constructions set forth herein and for the reasons set forth above and in the Final ID.

C. Additional Grounds for Finding the Technical Prong of the Domestic Industry Requirement Not Satisfied with Respect to the '907 Patent

As explained above, the Commission finds that Netlist failed to establish the technical prong of the domestic industry requirement as to the '907 patent for the same reasons Netlist failed to establish infringement.[8] In addition, for the reasons set forth below, the Commission determines that Netlist failed to establish the technical prong of the domestic industry requirement as to the '907 patent by failing to analyze adequately its domestic industry product and present evidence on the actual functionality of its domestic industry products.

[8] Netlist failed to establish the technical prong of the domestic industry requirement as to the '623 patent. Netlist concedes that the technical prong with respect to that patent rises and falls with infringement, Final ID at 62, and Netlist did not petition for review of the Final ID's finding that Netlist failed to establish infringement of the '623 patent.

1. Overview

The ALJ found that the technical prong of the domestic industry requirement for the ’907 patent rose and fell with his findings on infringement for the ’907 patent. Final ID at 103-04. He found that SK hynix waived its challenge to the technical prong by not including that argument in its pre-hearing brief. *Id.* at 103. The ALJ also rejected OUII’s argument that Netlist failed to carry its burden by failing to analyze the circuitry of the alleged domestic industry products, and instead found that Netlist’s analysis of the JEDEC standard is sufficient to establish the technical prong by the preponderance of the evidence. *Id.*

2. The Parties’ Arguments

Netlist argued that the alleged domestic industry products’ compliance with JEDEC standards is sufficient to satisfy each and every limitation of the asserted claims of the ’907 patent. Netlist Init. Sub. at 10-21. Netlist then argued that the evidence showed that each limitation was satisfied by reference to JEDEC standards, including by arguing that the domestic industry product satisfied the “do not receive” limitation because the memory device does not “acquire” data or perform the first stage of a write operation. *Id.* at 13-21.

SK hynix argued that, under its proposed constructions for “receive” and “produce,” the ’907 patent is not essential to any JEDEC standard, and thus Netlist’s reliance on JEDEC standards is fundamentally insufficient to show infringement. SK hynix Init. Sub. at 14-15. SK hynix also argued that, under the ALJ’s constructions, the Final ID found infringement of the “receive” / “do not receive” limitation based on the internal circuitry of the SK hynix memory device, but Netlist failed to present any such evidence of such internal circuitry for the domestic industry products. *Id.* at 16-22; SK hynix Rep. Sub. at 8-11.

OUII argued that Netlist’s domestic industry argument is a baseless assertion that the accused products and domestic industry products are identical. OUII Rep. Sub. at 8-23. OUII

contended that compliance with JEDEC standards was insufficient to establish the technical prong of the domestic industry requirement because, while the accused products and domestic industry products use JEDEC-compliant components, there was no evidence that the collective implementation of these different components results in the accused and domestic industry products having identical relevant functionality. OUII Init. Sub. at 29-30. OUII further argued that Netlist's expert did not even have access to the domestic industry products' circuitry, and thus Netlist failed to present any evidence regarding the relevant circuitry of its domestic industry products. *Id.* at 30-31; OUII Rep. Sub. at 8-23.

3. Analysis

As an initial matter, the Commission found above that the JEDEC-compliant accused products do not infringe any asserted claims of the '907 patent, which shows that JEDEC-compliance does not necessarily require the practice of the claims of the '907 patent. Because Netlist relies solely on JEDEC compliance to show that its domestic industry products practice claims of the '907 patent, Netlist's technical prong argument fails for that reason alone.

But even if that were not the case, the Commission finds that Netlist failed to demonstrate the technical prong of the domestic industry requirement by failing to present any evidence on the actual functionality of its domestic industry products. The asserted claims of the '907 patent are highly detailed, and include, for example, a requirement that the "second memory devices do not output or receive any data associated with the memory read or write command." This limitation requires an absolute prohibition (*i.e.*, that the devices "do not output or receive") over a broad class of data (*i.e.*, "any data" that is even "associated with the memory read or write command"). Regardless of the meaning of "receive," the satisfaction of the above limitation requires an analysis of the entire memory device (or at least all of its inputs and outputs) to ensure that no data associated with the "command" is received or outputted by the memory

device.

Netlist failed to supply such an analysis. Netlist's expert, Dr. Levitt, relied solely upon the JEDEC DDR4 SDRAM specification's statement that the system will read or write to a first or second memory depending on whether the CS pin has a low or high value. CX-2003C at Q/A 659-61. But while the JEDEC standard describes how to select the first memory device, the JEDEC standard does not address whether the nonselected second memory device does or does not output or receive "any data associated with the memory read or write command," as required by the claims. In other words, Netlist's only evidence for the "do not output or receive" limitation is a JEDEC standard that does not even address whether the nonselected memory device outputs or receives the data. Accordingly, the Commission finds that Netlist failed to present any evidence that the accused products satisfy the limitation "the second memory devices do not output or receive any data associated with the memory read or write command."

Nor did Netlist elsewhere analyze the domestic industry products for this limitation. Netlist's entire technical prong argument in its post-hearing brief consisted of a single paragraph that concluded without explanation that the accused and domestic industry products are identical. Netlist Initial Post-Hearing Br. at 54. Although the claim language involves the memory device's receipt and output of signals, Netlist's only expert on the issue repeatedly testified that he never even looked at the circuitry of the memory devices in the domestic industry devices. Hearing Tr. (Levitt) at 431:13-432:9. Dr. Levitt contended that he did not need to analyze the circuitry because the domestic industry devices still needed to provide JEDEC-standard functionality, but he admitted that the relevant JEDEC standard is just a block diagram that does not dictate any specific circuit configuration. Hearing Tr. (Levitt) at 446:3-15. Moreover, as discussed above, Netlist's cited JEDEC standards are silent on whether the nonselected memory

devices receive or output "any data" as required by the claims, so Netlist needed to show that the domestic industry products had circuitry that satisfied the limitation. By failing to look at the actual circuitry of the memory devices, Dr. Levitt had no basis to conclude that the second memory device does not output or receive "any data associated with the memory read or write command." Accordingly, the Commission finds no domestic industry on this independent basis.

D. The Economic Prong of the Domestic Industry Requirement as to the '623 and the '907 Patents

On review, the Commission has determined to take no position on whether Netlist satisfied the economic prong of the domestic industry requirement to both of the '623 and '907 patents.

E. The Requirement to Offer a License on "Reasonable and Non-Discriminatory" Terms

For the reasons set forth below, the Commission finds that the JEDEC Patent Policy was not shown to be unenforceable and that neither the '907 patent nor the '623 patent was shown to be essential to any JEDEC standard. The Commission discusses these findings below, reverses the Final ID's determination that the JEDEC Patent Policy was shown to be unenforceable, reverses the Final ID's determination that the '907 patent was shown to be essential to a JEDEC standard, and vacates other findings on RAND in the Final ID.

1. Enforceability

a. Overview

Pursuant to the JEDEC Manual and Patent Policy, Netlist and SK hynix agreed to provide licenses under reasonable and nondiscriminatory terms in certain circumstances. RX-2659 (JEDEC Manual). The Final ID found that the JEDEC Patent Policy agreement is unenforceable under New York contract law because the terms "reasonable" and "non-discriminatory" are ambiguous. *Id.* at 175-76.

b. Parties' Arguments

No party argued that the JEDEC Patent Policy is not enforceable.

c. Analysis

The Commission has determined to reverse the ID's finding that the JEDEC Patent Policy is unenforceable. The Final ID relied on *Cobble Hill Nursing Home, Inc. v. Henry and Warren Corp.*, which stated that "before rejecting an agreement as indefinite, a court must be satisfied that the agreement cannot be rendered reasonably certain by reference to an extrinsic standard that makes its meaning clear," such as "reference to an extrinsic event, commercial practice or trade usage." 548 N.E.2d 203, 206 (N.Y. 1989). The Commission finds that the ALJ erred by not assessing whether the frequent use of "reasonable and nondiscriminatory" terms by standard-setting organizations shows that the phrase is reasonably certain in commercial practice or trade usage, particularly in light of the numerous court cases that have found such agreements enforceable. *See, e.g, TCL Commc'n Tech. Holdings, Ltd. v. Telefonaktiebolaget LM Ericsson*, 2018 WL 4488286 (C.D. Cal. Sept. 14, 2018).[9] The use of these terms by numerous standard-setting organizations in similar agreements and the decisions of courts to interpret the provisions suggests that this agreement is enforceable, especially in light of *Cobble Hill*'s holding that a contract should be declared unenforceable only as "a last resort." 548 N.E.2d at 206. Accordingly, the Commission finds that the record does not demonstrate that the JEDEC Patent Policy is unenforceable under New York law, and therefore reverses the ID's finding that it is unenforceable.

[9] *See also, e.g., Microsoft Corp. v. Motorola, Inc.*, 696 F.3d 872, 884-85 (9th Cir. 2012); *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, Case No. 6:18-cv-00243-JRG, 2019 WL 4734950 (E.D. Tex. May. 22, 2019); *Realtek Semiconductor Corp. v. LSI Corp.*, 946 F. Supp. 2d 998, 1005-08 (N.D. Cal. 2013); *Apple, Inc. v. Motorola Mobility, Inc.*, 886 F. Supp. 2d 1061, 1083-87 (W.D. Wis. 2012).

2. Essentiality

a. Overview

The ID made a contingent finding on essentiality, stating that "if the Commission determines that the '907 patent is infringed in this Investigation, the undersigned finds that the evidence of record would support the conclusion that the Asserted Claims of the '907 patent are essential to a JEDEC standard." *Id.* at 175. Under that reasoning, the Final ID concluded that the '907 patent is essential because it found infringement of two of the '907 patent claims, and that the '623 patent is not essential because its claims are not infringed. *Id.* at 174-175.

b. Parties' Arguments

Netlist argued that the asserted claims of the '907 patent are essential to the JEDEC DDR4 LRDIMM standard based on: (1) Netlist's commitment of the '907 patent as essential to the JEDEC DD4 LRDIMM standard; (2) Netlist's adherence to JEDEC policy governing essential patent claims; (3) Netlist's steadfast contention that the asserted claims are essential; and (4) the Final ID's finding that the admittedly-DDR4-JEDEC-compliant accused products infringed the asserted claims of the '907 patent. Netlist Initial Sub. at 8-10.

SK hynix argued that, under the proper construction for "receive" and/or "produce . . .", the '907 patent is not essential to any JEDEC standard. SK hynix Init. Sub. at 12-13. SK hynix, however, argued that, if the Commission rejects SK hynix's arguments and finds a violation, then the '907 patent is essential to a JEDEC standard based on Netlist's binding admissions. *Id.* at 13-14.

OUII argued that there is no evidence in the record showing that the '907 patent is essential to any JEDEC standard. OUII Init. Sub. at 22-29. OUII contended that Netlist relied solely upon the JEDEC DDR4 standard for infringement, but failed to provide any evidence as to whether its cited portions of the DDR4 standard were mandatory or whether the accused

products actually used the cited functionality. *Id.* at 23-27. OUII further argued that SK hynix provided no evidence that compliance with any JEDEC standard necessarily infringes an asserted claim of the '907 patent. *Id.* at 28-29. In its reply brief, OUII pointed out that neither Netlist nor SK hynix identified any evidence that supports a finding of essentiality, and instead pointed to Netlist's mere representations that the patent is standard essential. *Id.* at 7.

c. Analysis

As an initial matter, the Commission finds the JEDEC-compliant accused products do not infringe either the '907 or '623 patent. Accordingly, Netlist failed to show that compliance with JEDEC standards would necessarily infringe the '907 or '623 patents, and therefore those patents are not shown to be essential to any JEDEC standard.

Regardless of that finding, the Commission finds that the Final ID's analysis is flawed. The Final ID concluded that, if a patent is infringed by a standard-compliant product, then the patent is essential to that standard. But under the JEDEC Patent Policy, a claim is essential to a JEDEC standard only if compliance with the required portions of the JEDEC standard would necessarily infringe the claim:

> **Essential Patent Claims:** Those Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard.
>
> NOTE Essential Patent Claims do not include Patent claims covering aspects that are not required to comply with a JEDEC Standard, or are required only for compliance with sections that are marked "example," "non-normative," or otherwise indicated as not being required for compliance, or related to underlying enabling technologies or manufacturing techniques not specified in the standard.

RX-2659 (JEDEC Manual) at .00030-31. Accordingly, to show standard essentiality, a party needs to show not only that the standard-compliant product infringes but also that compliance

with the mandatory portions of the standard necessarily requires infringement. Because the Final ID did not address whether mandatory portions of the standard required infringement, the Final ID erred by finding essentiality.

The record shows that no party presented any evidence explaining why the asserted claims of the ’907 patent or the ’623 patent are essential to any JEDEC standard. Netlist purported to “admit” that its patents are standard-essential to bolster its infringement case, but provided no evidence or argument in support of that admission. SK hynix seeks to rely on Netlist’s “admission,” but SK hynix too provided no evidence or argument that the asserted claims of the ’907 or ’623 patents are standard essential. Indeed, at no point in their essentiality analyses did Netlist or SK hynix identify a specific patent claim or a specific JEDEC standard, let alone explain why the mandatory portions of that standard necessarily require the infringement of that patent claim. Accordingly, the Commission finds that neither the ’907 patent nor the ’623 patent are standard essential based on the lack of evidence regarding essentiality.

IV. CONCLUSION

For the foregoing reasons, the Commission finds that Netlist failed to establish a violation of section 337 by SK hynix.

By order of the Commission.

Lisa R. Barton
Secretary to the Commission

Issued: April 21, 2020

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **Inv. No. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **COMMISSION OPINION** has been served by via EDIS the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on **April 21, 2020**.

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	**Investigation No. 337-TA-1089**

NOTICE OF COMMISSION DETERMINATION TO REVIEW IN PART A FINAL INITIAL DETERMINATION FINDING A VIOLATION OF SECTION 337; SCHEDULE FOR FILING WRITTEN SUBMISSIONS ON THE ISSUES UNDER REVIEW AND ON REMEDY, THE PUBLIC INTEREST, AND BONDING; EXTENSION OF THE TARGET DATE

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review in part a final initial determination ("ID") issued by the presiding administrative law judge ("ALJ"), finding a violation of section 337 of the Tariff Act of 1930. The Commission requests briefing from the parties on certain issues under review, as indicated in this notice. The Commission also requests briefing from the parties and interested persons on the issues of remedy, the public interest, and bonding. The Commission has also determined to extend the target date for the completion of the above-captioned investigation to April 7, 2020.

FOR FURTHER INFORMATION CONTACT: Robert Needham, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 708-5468. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. of Irvine, California ("Netlist"). 82 Fed. Reg. 57290-91. The complaint, as supplemented, alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337, in the importation

into the United States, the sale for importation, and the sale within the United States after importation of certain memory modules and components thereof that infringe claims 1-8, 10, 12, 14, 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of U.S. Patent No. 9,606,907 ("the '907 patent") and claims 1-5, 7-15, 17-25, 27, and 29 of U.S. Patent No. 9,535,623 ("the '623 patent"). *Id.* The Commission's notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (together, "SK hynix"). *Id.* at 57291. The Office of Unfair Import Investigations ("OUII") is also participating in this investigation. *Id.*

The Commission subsequently terminated the investigation with respect to claims 16-22, 24, 25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 12-15, 17-25, 27, and 29 of the '623 patent based on Netlist's partial withdrawal of its complaint. *See* Order. No. 12 (Mar. 19, 2018), *not reviewed*, Notice (Apr. 5, 2019); Order. No. 19 (Sept. 25, 2018), *not reviewed*, Notice (Oct. 15, 2018); Order. No. 27 (Dec. 6, 2018), *not reviewed*, Notice (Dec. 21, 2018). Accordingly, at the time of the Final ID, the remaining asserted claims were claims 1-8, 10, 12, 14, and 15 of the '907 patent and claims 1-5 and 7-11 of the '623 patent.

On October 19, 2019, the ALJ issued a final initial determination ("Final ID") finding a violation of section 337 with respect to claims 6 and 12 of the '907 patent. Final ID at 164-65. The ALJ found that Netlist showed that SK hynix infringes claims 1-8, 10, 12, 14, and 15 of the '907 patent, but failed to show that SK hynix infringed any claim of the '623 patent. The ALJ also found that SK hynix showed that claims 1-5, 7, 8, 10, 14, and 15 of the '907 patent are invalid as obvious, but failed to show the invalidity of claims 6 and 12. Finally, the ALJ found that Netlist satisfied the domestic industry requirement with respect to the '907 patent, but did not satisfy the domestic industry requirement with respect to the '623 patent.

On November 4, 2019, SK hynix and OUII petitioned for review of the Final ID with respect to many issues involved in the finding of violation with respect to the '907 patent. Also on November 4, 2019, Netlist contingently petitioned for review of the Final ID with respect to certain issues related to the '907 patent. On November 12, 2019, the parties filed responses to each other's petitions. Because Netlist did not petition for review of the Final ID's finding that SK hynix did not violate section 337 with respect to the '623 patent, the Commission finds that Netlist has abandoned that contention and that there is no violation of section 337 with respect to the '623 patent. *See* 19 CFR 210.43(b)(2) (stating that "[a]ny issue not raised in petition for review will be deemed to have been abandoned by the petitioning party").

Having examined the record of this investigation, including the ALJ's final ID, the petition for review, and the responses thereto, the Commission has determined to review the final ID in part. Specifically, the Commission has determined to review the following issues: (1) the construction of the limitation "receive" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (2) the construction of the limitation "produce first module control signals and second module

control signals in response to the set of input address and control signals" in the asserted claims of the '907 patent, as well as related issues of infringement and invalidity; (3) the domestic industry requirement with respect to both of the '623 and '907 patents; and (4) the findings with respect to both of the '623 and '907 patents regarding whether SK hynix showed that Netlist violated its obligations, if any, to offer a license on reasonable and non-discriminatory (RAND) terms. The Commission has determined not to review any other findings presented in the Final ID.

The Commission has also determined to extend the target date for the completion of the investigation until April 7, 2020.

In connection with its review, the Commission is interested in briefing on certain issues. The Commission is not requesting new argument, so for each response, the parties are to identify where they previously made such an argument in their pre- and post-hearing briefs. The Commission is interested in briefing on the following issues:

1. If the Commission were to view the limitation "set of input address and control signals" as referring to a group of input address and control signals, what evidence is there in the record regarding whether or not the accused products and domestic industry products satisfy the limitation "produce first module control signals and second module control signals in response to the set of input address and control signals"?

2. Please explain, with reference to supporting evidence in the record, whether the '907 and '623 patents are essential to any JEDEC standard.

3. Please explain, with reference to supporting evidence in the record, whether the alleged domestic industry products' compliance with JEDEC standards is sufficient to satisfy each and every limitation of a claim of the '907 patent.

4. Please describe the status of Netlist's activities and investments with respect to the articles protected by the '907 and '623 patents at the time of Netlist's filing of the complaint in this investigation. Additionally, please describe the current status of Netlist's domestic industry investments and activities with respect to the articles protected by the '907 and '623 patents.

The parties are invited to brief only the discrete issues described above, with reference to the applicable law and evidentiary record. The parties are not to brief other issues on review, which are adequately presented in the parties' existing filings.

In connection with the final disposition of this investigation, the statute authorizes issuance of (1) an order that could result in the exclusion of the subject articles from entry into the United States, and/or (2) cease and desist orders that could result in the respondents being required to cease and desist from engaging in unfair acts in the importation and sale of such articles. Accordingly, the Commission is interested in receiving written submissions that address the form of remedy, if any, that should be ordered. If a party seeks exclusion of an article from entry into the United States for purposes other than entry for consumption, the party should so indicate and provide information establishing that activities involving other types of entry either are adversely affecting it or likely to do so. For background, see *Certain Devices for Connecting Computers via Telephone Lines*, Inv. No. 337-TA-360, USITC Pub. No. 2843, Comm'n Op. at 7-10 (December 1994).

The statute requires the Commission to consider the effects of that remedy upon the public interest. The public interest factors the Commission will consider include the effect that an exclusion order and/or a cease and desist order would have on (1) the public health and welfare, (2) competitive conditions in the U.S. economy, (3) U.S. production of articles that are like or directly competitive with those that are subject to investigation, and (4) U.S. consumers. The Commission is therefore interested in receiving written submissions that address the aforementioned public interest factors in the context of this investigation. The Commission is particularly interested in briefing on the following issues:

1. Please discuss whether the market demand in the United States for memory modules and components thereof would be satisfied if the Commission issued remedial relief against SK hynix regarding the '907 patent. Please address whether that that demand could be satisfied by non-infringing RDIMMs, Netlist licensees, or others.

2. Please discuss the types of U.S. consumers that purchase and use the accused products, and discuss the potential impact on those consumers if the Commission were to issue remedial relief against SK hynix regarding the '907 patent.

3. Please explain whether and to what extent servers require uniform memory modules, so the operator of a server would have to replace the whole server system based on the failure of a single memory module if that specific memory module was no longer available. Please explain whether the issuance of remedial relief against SK hynix regarding the '907 patent would have such an effect, and, if so, the extent of that effect.

If the Commission orders some form of remedy, the U.S. Trade Representative, as delegated by the President, has 60 days to approve, disapprove, or take no action on the Commission's determination. *See* Presidential Memorandum of July 21, 2005, 70 FR 43251 (July 26, 2005). During this period, the subject articles would be entitled to enter the United States under bond, in an amount determined by the Commission and

prescribed by the Secretary of the Treasury. The Commission is therefore interested in receiving submissions concerning the amount of the bond that should be imposed if a remedy is ordered.

WRITTEN SUBMISSIONS: The Commission requests that the parties to the investigation file written submissions on the issues identified in this notice. The Commission encourages parties to the investigation, interested government agencies, and any other interested parties to file written submissions on the issues of remedy, the public interest, and bonding. Such initial written submissions should include views on the recommended determination by the ALJ on remedy, the public interest, and bonding, which issued in the same document as the Final ID on October 21, 2019. Netlist and the Commission Investigative Attorney are also requested to identify the form of the remedy sought and to submit proposed remedial orders for the Commission's consideration in their initial written submissions. Netlist is further requested to state the date when the '907 patent expires, provide the HTSUS numbers under which the subject articles are imported, and supply a list of known importers of the subject article. The written submissions, exclusive of any exhibits, must not exceed 50 pages, and must be filed no later than close of business on February 14, 2020. Reply submissions must not exceed 25 pages, and must be filed no later than the close of business on February 21, 2020. No further submissions on these issues will be permitted unless otherwise ordered by the Commission.

Persons filing written submissions must file the original document electronically on or before the deadlines stated above and submit 8 true paper copies to the Office of the Secretary by noon the next day pursuant to section 210.4(f) of the Commission's Rules of Practice and Procedure (19 CFR § 210.4(f)). Submissions should refer to the investigation number ("Inv. No. 337-TA-1089") in a prominent place on the cover page and/or the first page. (*See* Handbook for Electronic Filing Procedures, http://www.usitc.gov/secretary/fed_reg_notices/rules/handbook_on_electronic_filing.pdf). Persons with questions regarding filing should contact the Secretary (202-205-2000).

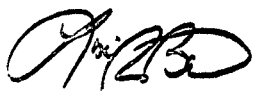
Any person desiring to submit a document to the Commission in confidence must request confidential treatment. All such requests should be directed to the Secretary to the Commission and must include a full statement of the reasons why the Commission should grant such treatment. *See* 19 C.F.R. § 201.6. Documents for which confidential treatment by the Commission is properly sought will be treated accordingly. All information, including confidential business information and documents for which confidential treatment is properly sought, submitted to the Commission for purposes of this Investigation may be disclosed to and used: (i) by the Commission, its employees and Offices, and contract personnel (a) for developing or maintaining the records of this or a related proceeding, or (b) in internal investigations, audits, reviews, and evaluations relating to the programs, personnel, and operations of the Commission including under 5 U.S.C. Appendix 3; or (ii) by U.S. government employees and contract personnel[1],

[1] All contract personnel will sign appropriate nondisclosure agreements.

solely for cybersecurity purposes. All nonconfidential written submissions will be available for public inspection at the Office of the Secretary and on EDIS.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. 1337), and in part 210 of the Commission's Rules of Practice and Procedure (19 CFR part 210).

By order of the Commission.



Lisa R. Barton
Secretary to the Commission

Issued: January 31, 2020

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **Inv. No. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on **January 31, 2020**.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Complainants Netlist, Inc.:

James M. Wodarski
MINTZ LEVIN COHN FERRIS GLOVSKY AND POPEO PC
One Financial Center
Boston, MA 02111

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other:_____

On Behalf of Respondents SK Hynix Inc., SK Hynix America Inc., and SK Hynix memory solutions Inc.:

Michael R. Franzinger
SIDLEY AUSTIN LLP
1501 K Street, N.W.
Washington, DC 20005

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other:_____

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of	
CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	**Inv. No. 337-TA-1089**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Chief Administrative Law Judge Charles E. Bullock

(October 21, 2019)

Appearances:

For the Complainant Netlist, Inc.:

James M. Wodarski, Esq., Michael T. Renaud, Esq., Andrew H. DeVoogd, Esq., Kristina R. Cary, Esq., Matthew S. Galica, Esq., Tiffany M. Knapp of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo PC of Boston, MA.

Aarti Shah, Esq. of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo PC of Washington, DC.

Stephen J. Akerley, Esq. of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo PC of San Francisco, CA.

For the Respondents SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.:

Brian R. Nester, Esq., Michael R. Franzinger, Esq., Wonjoo Suh, Esq. of Sidley Austin LLP of Washington, DC.

Ryuk Park, Esq. of Sidley Austin LLP of Palo Alto, CA.

David T. Pritikin, Esq., Richard A. Cederoth, Esq., David C. Giardina, Esq. of Sidley Austin LLP of Chicago, IL.

Theodore W. Chandler, Esq. of Sidley Austin LLP of Los Angeles, CA.

Michael D. Hatcher, Esq. of Sidley Austin LLP of Dallas, TX.

For the Commission Investigative Staff:

Margaret D. Macdonald, Esq., Director; David O. Lloyd, Esq., Supervisory Attorney; Monisha Deka, Esq., Investigative Attorney of the Office of Unfair Import Investigations, U.S. International Trade Commission, of Washington, D.C.

TABLE OF CONTENTS

TABLE OF ABBREVIATIONS

CDX	Complainant's demonstrative exhibit
CIB	Complainant's initial post-hearing brief
CPB	Complainant's pre-hearing brief
CPX	Complainant's physical exhibit
CRB	Complainant's reply post-hearing brief
CX	Complainant's exhibit
Dep.	Deposition
JX	Joint Exhibit
RDX	Respondents' demonstrative exhibit
RIB	Respondents' initial post-hearing brief
RPX	Respondents' physical exhibit
RPB	Respondents' Pre-hearing brief
RRB	Respondents' reply post-hearing brief
RX	Respondents' exhibit
SIB	Staff's initial post-hearing brief
SPB	Staff's pre-hearing brief
SRB	Staff's reply post-hearing brief
[Name], Tr.	Evidentiary Hearing Transcript

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of	
CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	**INV. NO. 337-TA-1089**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Chief Administrative Law Judge Charles E. Bullock

(October 21, 2019)

Pursuant to the Notice of Investigation, 82 Fed. Reg. 57290-1 (Dec. 4, 2017), this is the Initial Determination in the matter of *Certain Memory Modules and Components thereof*, Investigation No. 337-TA-1089.

For the reasons stated herein, the undersigned has determined that a violation of section 337 of the Tariff Act of 1930, as amended, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain memory modules and components thereof with respect to U.S. Patent No. 9,606,907. No violation has occurred with respect to U.S. Patent No. 9,535,623.

I. INTRODUCTION

A. Procedural History

On October 31, 2017, complainant Netlist, Inc. ("Netlist" or "Complainant") filed a complaint alleging violations of section 337 based upon the sale for importation, importation, or sale within the United States after importation of certain memory modules and components thereof. 82 Fed. Reg. 57290 (Dec. 4, 2017). On November 21, 2017, Netlist supplemented the complaint. *Id.*

On November 28, 2017, the Commission instituted this Investigation to determine:

> [W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain memory modules and components thereof by reason of infringement of one or more of claims 1–8, 10, 12, 14–22, 24–25, 27, 29–35, 38, 43–45, 47, 48, 50, 52, and 58 of the '907 patent and claims 1–5, 7–15, 17–25, 27, and 29 of the '623 patent; and whether an industry in the United States exists or is in the process of being established, as required by subsection (a)(2) of section 337;

Id. at 57290-1.

The named respondents are SK hynix, Inc. of Gyeoonggi-do, Republic of Korea; SK hynix America, Inc. of San Jose, California; and SK hynix memory solutions, Inc. of San Jose, California (collectively, "SK hynix" or "Respondents"). *Id.* at 57291. The Commission Investigative Staff ("Staff") is also a party to this Investigation. *Id.* On November 28, 2017, the undersigned assigned the investigation to Administrative Law Judge Thomas Pender. (EDIS Doc. ID 630098.)

On January 23, 2018, Netlist moved to amend the complaint and notice of investigation to assert and additional patent, U.S. Patent No. 9,858,218 which had issued on January 2, 2018. (Mot. No. 1089-003.) Netlist withdrew the motion on January 25, 2018 following a teleconference with the presiding ALJ. (EDIS Doc. ID 634845.) Additionally, at various times throughout the

investigation, Netlist moved to terminate certain collections of patent claims asserted against the Respondents. (*See* Order No. 12 (terminating claims 30, 31, 32, 33, 34, 35, and 38 of U.S. Patent No. 9,606,907 ("the '907 patent")); Order No. 19 (terminating claims 43, 44, 45, 47, 48, 50, 52, and 58 of the '907 patent); Order No. 27 (terminating 16, 17-22, 24-25, 27, and 29 of the '907 patent and claims 12, 13-15, 17-20, 21, 22-25, 27, and 29 of U.S. Patent No. 9,535,623 ("the '623 patent")).) Thus, the following claims remain asserted at the time of this initial determination: claims 1-8, 10, 12, 14, and 15 of the '907 patent; and claims 1-5 and 7-11 of the '623 patent.

On January 30, 2018, the presiding ALJ issued the procedural schedule (Order No. 7). On February 20, 2018, Respondents moved for summary determination of non-infringement on both of the '907 and '623 patents on the basis of claim preclusion and issue preclusion stemming from determinations made as part of prior investigation, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 ("the 1023 Investigation"). (Mot. No. 1089-006.)[1] The presiding ALJ granted-in-part the motion with Order No. 13 on April 12, 2018. Upon review, the Commission vacated Order No. 13 and remanded the investigation for further proceedings. (EDIS Doc. IDs 646160, 646161.) Accordingly, the presiding ALJ issued an initial determination extending the target date of the investigation and amending all remaining procedural schedule deadlines on June 14, 2018. (Order No. 14.) On August 24, 2018, and in response to briefing submitted by the parties, the presiding ALJ issued an order construing certain terms of the asserted claims. (Order No. 17.)

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[1] The Final Initial Determination of this investigation, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023, Initial Determination (Dec. 4, 2017) (public version) is referred to in this initial determination as "the 1023 ID."

On September 4, 2018, and due to the retirement of the prior ALJ, the investigation was reassigned to the undersigned. (EDIS Doc. ID 654640.) Additionally, and with respect to the procedural schedule, the government shutdown occurring between December of 2018 and January of 2019 necessitated a further extension of all deadlines and the target date in this investigation. At the completion of the shutdown, the undersigned issued Order No. 29 on January 29, 2019 which moved the start of the evidentiary hearing to March 11, 2019.

The evidentiary hearing was begun on March 11, 2019, however, for reasons of a family emergency, the undersigned cancelled the remainder of the hearing on March 12, 2019. Thereafter, on April 11, 2019, the undersigned issued a further, and final, extension of the target date (Order No. 48) and subsequently rescheduled the evidentiary hearing to the week of July 15-19, 2019 (Order No. 19). The evidentiary hearing recommenced July 15-19, 2019.

As of the date of this initial determination, two motions remain outstanding—Respondents' Motion to Strike Untimely Infringement Theory from Netlist's Reply Post-Hearing Brief (Mot. No. 1089-054) and Respondents' Motion for Leave to File a Reply in Support of [the prior motion] (Mot. No. 1089-055). Upon review of these pleadings, Netlist has not adequately discussed in its pre-hearing brief (*see* Opp. at 8 (citing CPB at 112-114)) the theory presented in its reply post-hearing brief; specifically, a theory the '907 patent claim term "second memory devices do not . . . receive any data associated with the memory . . . write command" can be satisfied simply by the memory devices operating in conjunction with a read command (*see* CRB at 3-4, 7, 12-13). This late theory is therefore in contravention of Ground Rule 9.2. Accordingly, Respondents' motion to strike (1089-054) is hereby granted; Respondents' motion for leave (1089-055) is denied.

B. The Parties

1. Complainant

Complainant Netlist, Inc. is a Delaware corporation with a principal place of business at 175 Technology Drive, Suite 150, Irvine, California. (CX-2001C at Q/A 49-50, 56.) Netlist is in the business of designing, developing, manufacturing, and supporting high-performance memory modules. (*Id.* at Q/A 51, 53-54.)

2. Respondents

SK hynix Inc. is a Korean corporation, having a principal place of business at 2091, Gyeonghung-daero, Bubal-eub, Icheon-si, Gyeonggi-do, Korea. (Respondents' Amended Resp. to Complaint at ¶ 27.) SK hynix Inc. is the parent corporation of Respondents SK hynix America Inc. and SK hynix memory solutions Inc. (*Id.*; RX-2002C at Q/A 37; RX-2001C at Q/A 41) SK hynix Inc. is a manufacturer and supplier of dynamic random-access memory ("DRAM") chips and memory modules, including the accused DDR4 LRDIMM and RDIMM products in this investigation. (*See* RX-2002C at Q/A 7.)

Respondent SK hynix America, Inc. is a California corporation, having a principal place of business at 3101 North 1st Street, San Jose, California. (Respondents' Amended Resp. to Complaint at ¶ 28.) SK hynix America, Inc. provides sales and technical support, assists with customer relationships in the United States for SK hynix Inc., and imports the accused products to this investigation into the United States. (*Id.*; RX-2002C at Q/A 37; JX-2030C at ¶ 2.)

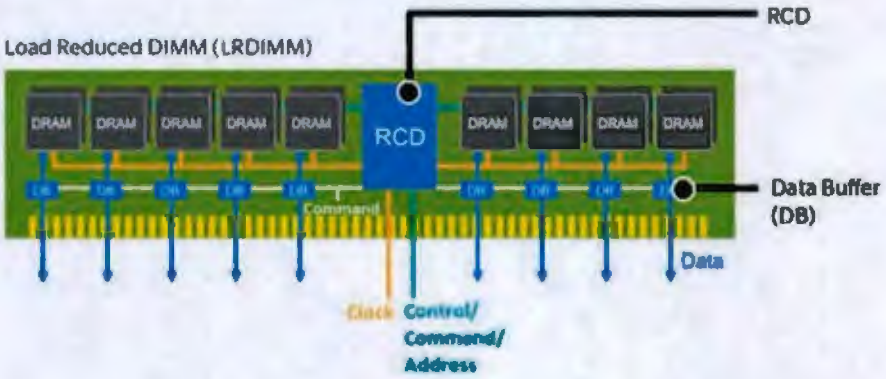
SK hynix memory solutions, Inc. has a principal place of business at 3103 North 1st Street, San Jose, California. (Respondents' Amended Resp. to Complaint at ¶ 29.) SK hynix memory solutions, Inc. is a wholly-owned subsidiary of SK hynix Inc. that performs research and

development and provides customers with controller hardware and flash management systems and firmware for devices. (*Id.*; RX-2001C at Q/A 41.)

C. Overview of the Technology and Relevant Products

The technology in this investigation relates to two types of memory modules: DDR4 Registered Dual In-Line Memory Modules ("RDIMMs") and DDR4 Load-Reduced Dual In-Line Memory Modules ("LRDIMMs"). (*See, e.g.*, CIB at 8-12, 14; RIB at 6.) Both RDIMMs and LRDIMMs are designed for use in servers to store data that must be readily available for certain software applications, and to allow quick and efficient retrieval of that data. (CIB at 8 (citing CX-2003C at Q/A 56, 59); RIB at 6.) The DDR4 designation refers to the particular generation of the DRAM chips on the memory module. DDR4 is the most recent generation of these DRAM chips, preceded by DDR3. (*See id.* at 9-12 (citing, *inter alia*, CX-2007C at Q/A 8-11).)

RDIMMs and LRDIMMS share several similar components, including a printed circuit board, DRAM chips, and a Register/ing Clock Driver ("RCD"). (*See id.* at 10-13 (citing, *inter alia*, Wedig, Tr. at 579:8-18).) LRDIMMS also contain Data Buffers ("DBs") on the printed circuit board. (*See id.* at 12 (citing, *inter alia*, CX-2001C at Q/A 83, 97; CX-0833 at *2).) Netlist provides the following demonstrative example LRDIMM:



(CIB at 13 (citing CDX-2004C).)

In this investigation, Netlist accuses Respondents of infringing U.S. Patent No. 9,606,907 ("the '907 patent") through its JEDEC-compliant LRDIMM products (CIB at 15), which Netlist lists by model number in the preface to its initial post-hearing brief (*id.* at xxvi-xvii), as reproduced below:

Accused LRDIMM Products	DENEB 8Gb DDR4 2rank x4 SDP 32GB LRDIMM (HMA84GL7AFR4N-UHT2; HMA84GL7AFR4N-UHTE; HMA84GL7AFR4N-VKT3; HMA84GL7AFR4N-VKTF; HMA84GL7AFR4N-XNT4; HMA84GL7AFR4N-XNT8; HMA84GL7AFR4N-XNTG); POLARIS 4Gb DDR4 4rank x4 DDP 32GB LRDIMM (HMA84GL7AMR4N-TFT2; HMA84GL7AMR4N-TFTE; HMA84GL7AMR4N-UHT2 HMA84GL7AMR4N-UHTE; HMA84GL7AMR4N-VKT3; HMA84GL7AMR4N-VKTF); POLARIS 4Gb DDR4 2rank x4 SDP 16GB LRDIMM (HMA42GL7AFR4NTFTE); DENEB 8Gb DDR4 4rank x4 DDP 64GB LRDIMM (HMAA8GL7AMR4N-UHT2; HMAA8GL7AMR4N-UHTE; HMAA8GL7AMR4N-VKT3; HMAA8GL7AMR4N-VKTF); POLARIS 8Gb DDR4 4rank x4 DDP 64GB LRDIMM (HMAA8GL7MMR4N-TFT1; HMAA8GL7MMR4N-TFTD; HMAA8GL7MMR4N-UHT2; HMAA8GL7MMR4N-UHTE); POLARIS 8Gb DDR4 2rank x4 SDP 32GB LRDIMM (HMA84GL7MFR4N-UHT2; HMA84GL7MFR4N-UHTE); POLARIS 8Gb DDR4 8rank x4 TSV 4H/4 128GB LRDIMM (HMABAGL7M4R4N-ULT2; HMABAGL7M4R4N-ULTE; HMABAGL7M4R4N-VNT3; HMABAGL7M4R4N-VNTF); HUMA 4Gb DDR4 4rank x4 DDP 32GB LRDIMM (HMA84GL7MMR4NTFT1; HMA84GL7MMR4N-TFTD); HUMA

	4Gb DDR4 2rank x4 SDP 16GB LRDIMM (HMA42GL7MFR4N-TFT1; HMA42GL7MFR4N-TFTD); ALIUS 8Gb DDR4 4rank x4 DDP 64GB LRDIMM (HMAA8GL7CPR4N-XNT4)

Netlist accuses Respondents of infringing U.S. Patent No. 9,535,623 ("the '623 patent") through its JEDEC-compliant LRDIMM products *and* its JEDEC-compliant RDIMM products (CIB at 15), the latter of which Netlist also lists by model number in the preface to its initial post-hearing brief (*id.* at xvii-xix), as reproduced below:

Accused RDIMM Products	DENEB 8Gb DDR4 1rank x8 SDP 8GB RDIMM (HMA81GR7AFR8N-UHT2; HMA81GR7AFR8N-UHTD; HMA81GR7AFR8N-VKT3; HMA81GR7AFR8N-VKTF; HMA81GR7AFR8N-VKTN; HMA81GR7AFR8N-XNT8; HMA81GR7AFR8N-XNTG); DENEB 8Gb DDR4 2rank x8 SDP 16GB RDIMM (HMA82GR7AFR8N-TFTD; HMA82GR7AFR8NUHT2; HMA82GR7AFR8N-UHTD; HMA82GR7AFR8N-UHTN; HMA82GR7AFR8N-VKT3; HMA82GR7AFR8N-VKTF; HMA82GR7AFR8N-XNT4; HMA82GR7AFR8N-XNT8; HMA82GR7AFR8N-XNTG); DENEB 8Gb DDR4 1rank x4 SDP 16GB RDIMM (HMA82GR7AFR4N-UHT2; HMA82GR7AFR4NUHTD; HMA82GR7AFR4N-VKBF; HMA82GR7AFR4N-VKT3; HMA82GR7AFR4N-VKTF; HMA82GR7AFR4N-VKTN; HMA82GR7AFR4N-XNT8; HMA82GR7AFR4N-XNTG); DENEB 8Gb DDR4 2rank x4 SDP 32GB RDIMM (HMA84GR7AFR4NTFTD; HMA84GR7AFR4N-UHT2; HMA84GR7AFR4N-UHTD; HMA84GR7AFR4N-VKT3; HMA84GR7AFR4N-VKTF; HMA84GR7AFR4N-UHC2; HMA84GR7AFR4N-UHCD; HMA84GR7AFR4N-VKTN; HMA84GR7AFR4N-XNT4; HMA84GR7AFR4N-XNT8; HMA84GR7AFR4N-XNTG); ALIUS 8Gb DDR4 2rank x4 SDP 32GB RDIMM (HMA84GR7BJR4N-UHC2; HMA84GR7BJR4N-UHCD); POLARIS 4Gb DDR4 2rank x4 DDP 16GB RDIMM (HMA82GR8AMR4N-TFT1; HMA82GR8AMR4NTFTD; HMA82GR8AMR4N-UHTD); POLARIS 4Gb DDR4 1rank x4 SDP 8GB RDIMM (HMA41GR7AFR4N-TFT1;HMA41GR7AFR4NTFTD; HMA41GR7AFR4N-UHT2; HMA41GR7AFR4N-UHTD; HMA41GR7AFR4N-VKT3; HMA41GR7AFR4N-VKTN); POLARIS 4Gb DDR4 2rank x8 SDP 8GB RDIMM (HMA41GR7AFR8N-TFT1; HMA41GR7AFR8N-TFTD; HMA41GR7AFR8N-UHT2; HMA41GR7AFR8N-UHTD; HMA41GR7AFR8N-VKT3; HMA41GR7AFR8N-VKTF); DENEB 4Gb DDR4 1rank x4 SDP 8GB RDIMM (HMA41GR7BJR4N-TFTD; HMA41GR7BJR4N-UHT2;

	HMA41GR7BJR4N-UHTD; HMA41GR7BJR4N-VKT3; HMA41GR7BJR4N-VKTF; HMA41GR7BJR4N-VKTN); DENEB 4Gb DDR4 2rank x8 SDP 8GB RDIMM (HMA41GR7BJR8N-VKT3); POLARIS 4Gb DDR4 2rank x4 SDP 16GB RDIMM (HMA42GR7AFR4N-TFT1; HMA42GR7AFR4N-TFTD; HMA42GR7AFR4N-UHT2; HMA42GR7AFR4N-UHTD; HMA42GR7AFR4N-VKT3; HMA42GR7AFR4N-VKTF; HMA42GR7AFR4N-VKTN); DENEB 4Gb DDR4 2rank x4 SDP 16GB RDIMM (HMA42GR7BJR4N-TFT2; HMA42GR7BJR4NTFTD; HMA42GR7BJR4N-UHT2; HMA42GR7BJR4N-UHTD; HMA42GR7BJR4N-VKT3; HMA42GR7BJR4N-VKTF); POLARIS 4Gb DDR4 1rank x8 SDP 4GB RDIMM (HMA451R7AFR8N-TFT1; HMA451R7AFR8N-TFTD; HMA451R7AFR8N-UHT2; HMA451R7AFR8N-UHTD; HMA451R7AFR8N-VKT3; HMA451R7AFR8N-VKTF); DENEB 8Gb DDR4 2rank x4 DDP 32GB RDIMM (HMAA4GR8AMR4N-UHT2; HMAA4GR8AMR4NUHTD); POLARIS 8Gb DDR4 2rank x4 DDP 32GB RDIMM (HMAA4GR8MMR4N-TFT1; HMAA4GR8MMR4N-TFTD); DENEB 8Gb DDR4 2S2R x4 TSV 2HI 64GB RDIMM (HMAA8GR7A2R4NVNT3; HMAA8GR7A2R4N-VNTF); DENEB 8Gb DDR4 2S4R x4 TSV 4HI 128GB RDIMM (HMABAGR7A4R4N-VNT3; HMABAGR7A4R4N-VNTF); POLARIS 8Gb DDR4 1rank x8 SDP 8GB RDIMM (HMA81GR7MFR8N-UHT2; HMA81GR7MFR8NUHTD); POLARIS 8Gb DDR4 2rank x8 SDP 16GB RDIMM (HMA82GR7MFR8N-UHT2; HMA82GR7MFR8N-UHTD; HMA82GR7MFR8N-VKT3); POLARIS 8Gb DDR4 1rank x4 SDP 16GB RDIMM (HMA82GR7MFR4N-TFTD; HMA82GR7MFR4NUHT2; HMA82GR7MFR4N-UHTD; HMA82GR7MFR4N-VKT3); POLARIS 8Gb DDR4 2rank x4 SDP 32GB RDIMM (HMA84GR7MFR4N-TFT1; HMA84GR7MFR4N-TFTD; HMA84GR7MFR4N-UHT2; HMA84GR7MFR4N-UHTD; HMA84GR7MFR4N-VKT3; HMA84GR7MFR4N-VKTF); HUMA 4Gb DDR4 2rank x4 DDP 16GB RDIMM (HMA82GR8MMR4NTFT1; HMA82GR8MMR4N-TFTD); HUMA 4Gb DDR4 1rank x4 SDP 8GB RDIMM (HMA41GR7MFR4N-TFT1; HMA41GR7MFR4N-TFTD); HUMA 4Gb DDR4 2rank x8 SDP 8GB RDIMM (HMA41GR7MFR8N-TFT1; HMA41GR7MFR8N-TFTD); HUMA 4Gb DDR4 2rank x4 SDP 16GB RDIMM (HMA42GR7MFR4N-TFHD; HMA42GR7MFR4N-TFT1; HMA42GR7MFR4N-TFTD); HUMA 4Gb DDR4 1rank x8 SDP 4GB RDIMM (HMA451R7MFR8N-TFT1; HMA451R7MFR8N-TFTD); DENEB 8Gb/4Gb DDR4 2rank x8 SDP 12GB RDIMM

	(HMA815R7AFR8N-VKT3; HMA815R7AFR8N-VKTF); ALIUS 8Gb DDR4 1rank x4 SDP 16GB RDIMM (HMA82GR7CJR4N-VKTN; HMA82GR7CJR4N-VKTF; HMA82GR7CJR4N-WMT4)

It should be understood that, when this initial determination uses the term "Accused Products" in the context of the '907 patent, it refers to the collective group of LRDIMM products identified above. When in the context of the '623 patent, or neither patent in particular, the term "Accused Products" refers to all LRDIMM and RDIMM products.

For the purposes of domestic industry in this investigation, Netlist identifies its "16 GB 2Rx4 DDR4 HV-LRDIMM" and "32GB 2Rx4 DDR4 HV-LRDIMM" products as practicing claims of both the '907 and '623 patents. (CIB at 14.) These two products are referred to together as the "Domestic Industry Products" in this initial determination.

D. Asserted Patents

1. U.S. Patent No. 9,606,907

U.S. Patent No. 9,606,907 is entitled "Memory Module with Distributed Data Buffers and Method of Operation." (JX-2001 (hereafter cited as '907 patent).) It issued on March 28, 2017 from an application filed on August 20, 2013. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA and Jayesh R. Bhakta inventors. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) The '907 patent generally relates to memory modules which include data buffer circuits that control, and potentially inhibit, data transmission between a system memory controller and memory devices located on the module. (*See id.* at 2:25-58, Figs. 4A, 4B.) As noted, Netlist asserts claims 1-8, 10, 12, 14, and 15 of the '907 patent in this investigation. Importantly, the '907 patent claims priority, at least, to U.S. Patent 8,516,185 ("the '185 patent") which was asserted as part of the 1023 Investigation.

2. U.S. Patent No. 9,535,623

U.S. Patent No. 9,535,623 is entitled "Memory Module Capable of Handshaking with a Memory Controller of a Host System." (JX-2002 (hereafter cited as '623 patent).) It issued on January 3, 2017, from an application filed June 1, 2016. (*Id.*) The patent lists Hyun Lee of Ladera Ranch, CA as the inventor. (*Id.*) Netlist, Inc. of Irvine, CA is listed as the assignee. (*Id.*) The '623 patent generally relates to memory modules which generate a signal reflecting a status of one or more training sequences it undergoes to prepare for normal operation, wherein that signal can then be transmitted to the system memory controller to communicate that status. (*See id.* at Abstract.) As noted, Netlist asserts claims 1-5 and 7-11 of the '623 patent in this investigation. Importantly, the '623 patent claims priority, at least, to U.S. Patent 8,489,837 ("the '837 patent") which was also asserted as part of the 1023 Investigation.

II. JURISDICTION & IMPORTATION

A. Subject Matter Jurisdiction

Section 337 confers subject matter jurisdiction on the Commission to investigate, and if appropriate, to provide a remedy for, unfair acts and unfair methods of competition in the importation, the sale for importation, or the sale after importation of articles into the United States. *See* 19 U.S.C. §§ 1337(a)(1)(B), (a)(2). Netlist filed a complaint alleging a violation of this subsection. Accordingly, the Commission has subject matter jurisdiction over this Investigation under section 337 of the Tariff Act of 1930. *See Amgen, Inc. v. U.S. Int'l. Trade Comm'n.*, 902 F.2d 1532, 1536 (Fed. Cir. 1990).

B. Personal Jurisdiction

Respondents have appeared and participated in this Investigation. The Commission therefore has personal jurisdiction over Respondents. *See, e.g., Certain Optical Disk Controller Chips &*

Chipsets & Prods. Containing Same, Including DVD Players & PC Optical Storage Devices, Inv. No. 337-TA-506, Initial Determination at 4-5 (May 16, 2005) (unreviewed in relevant part).

C. *In Rem* Jurisdiction

Respondents do not dispute that the Commission has *in rem* jurisdiction over the SK hynix accused products that have been imported into the United States. (RIB at 7.) In fact, Respondents admit that "SK hynix America Inc. imports the accused DDR4 LRDIMM and RDIMM memory modules into the United States." (*Id.*) Accordingly, the Commission has *in rem* jurisdiction over the Accused Products.

D. Importation

As noted above, Respondents do not dispute that they import the accused RDIMM and LRDIMM memory modules (*see* RIB at 7) and Netlist notes the parties have entered into a stipulation "admit[ing] that each Accused Product is sold by SK hynix Inc. to SK hynix America, Inc. outside the United States, and then imported into the United States by SK hynix America, Inc." (CIB at 20 (citing JX-2030C).) Accordingly, the importation requirement of section 337 is satisfied.

E. Standing

Netlist asserts that it has standing to bring this investigation based on its rights and interest in the asserted patents. (CIB at 20 (citing JX-2005; JX-2006; CX-2001C at Q/A 72-73).) The Staff agrees. (SIB at 21 (citing JX-2005; JX-2006).) Respondents do not appear to dispute standing in their briefing. The undersigned finds this evidence is sufficient to establish Netlist's standing to bring this suit.

III. RELEVANT LAW

A. Claim Construction

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *see also Markman*, 52 F.3d at 979. As the United States Court of Appeals for the Federal Circuit ("Federal Circuit") explained in *Phillips*, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in the art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims

themselves provide substantial guidance as to the meaning of particular claims terms." *Id.* at 1314; *see Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point[ ] out and distinctly claim[ ] the subject matter which the patentee regards as his invention.'"). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.*

The specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Id.* at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be . . . the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Id.* at 1317; *see Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the

invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* at 1317. "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, "if the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid." *Id.*

B. Infringement

In a section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *See Spansion, Inc. v. Int'l Trade Comm'n*, 629 F.3d 1331, 1349 (Fed. Cir. 2010). This standard "requires proving that infringement

was more likely than not to have occurred." *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n.15 (Fed. Cir. 2005).

Literal infringement is a question of fact. *See Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). Literal infringement requires the patentee to prove that the accused device contains each limitation of the asserted claim(s). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *See Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

C. Validity

A patent is presumed valid. 35 U.S.C. § 282; *Microsoft Corp. v. i4i Ltd. P'ship*, 131 S. Ct. 2238, 2242 (2011). A respondent who has raised patent invalidity as an affirmative defense has the burden of overcoming this presumption by clear and convincing evidence. *See Microsoft*, 131 S. Ct. at 2242. As with an infringement analysis, an analysis of invalidity involves two steps: determining the scope of the claim and comparing the properly construed claim with the prior art to determine whether the claimed invention is anticipated and/or rendered obvious.

1. Anticipation (35 U.S.C. § 102)

Under 35 U.S.C. § 102 (pre-AIA), a claim is anticipated and therefore invalid when "the four corners of a single, prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation." *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000), *cert. denied*, 532 U.S. 904 (2001). To be considered anticipatory, the prior art reference must be enabling and describe the applicant's claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000).

2. Obviousness (35 U.S.C. § 103)

Under 35 U.S.C. §103 (pre-AIA), a patent may be found invalid as obvious if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. §103(a). Because obviousness is determined at the time of invention, rather than the date of application or litigation, "[t]he great challenge of the obviousness judgment is proceeding without any hint of hindsight." *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1375 (Fed. Cir. 2011) ("*Star II*").

When a patent is challenged as obvious, the critical inquiry in determining the differences between the claimed invention and the prior art is whether there is an apparent reason to combine the known elements in the fashion claimed by the patent at issue. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417-418 (2007). The Federal Circuit has since held that when a patent is challenged as obvious, based on a combination of several prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007) (citations omitted).

Obviousness is a determination of law based on underlying determinations of fact. *Star II*, 655 F.3d at 1374. The factual determinations behind a finding of obviousness include: (1) the scope and content of the prior art, (2) the level and content of the prior art, (3) the differences between the claimed invention and the prior art, and (4) secondary considerations of non-obviousness. *KSR*, 550 U.S. at 399 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). These factual determinations are referred to collectively as the "*Graham* factors." Secondary

considerations of non-obviousness include commercial success, long felt but unresolved need, and the failure of others. *Id.* When present, secondary considerations "give light to the circumstances surrounding the origin of the subject matter sought to be patented," but they are not dispositive on the issue of obviousness. *Geo. M. Martin Co. v. Alliance Mach. Sys. Int'l.*, 618 F.3d 1294, 1304-06 (Fed. Cir. 2010). A court must consider all of the evidence from the *Graham* factors before reaching a decision on obviousness. For evidence of secondary considerations to be given substantial weight in the obviousness determination, its proponent must establish a nexus between the evidence and the merits of the claimed invention. *See W. Union Co. v. MoneyGram Payment Sys. Inc.*, 626 F.3d 1361, 1372-73 (Fed. Cir. 2010) (citing *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995)).

3. Written Description (35 U.S.C. § 112)

Under 35 U.S.C. §112 (pre-AIA) "The specification shall contain a written description of the invention . . . in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same . . . ." The hallmark of the written description requirement is the disclosure of the invention. *See Ariad Pharm., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). The test for determining the sufficiency of the written description in a patent requires "an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed." *Id.* Compliance with the written description requirement is a question of fact and "the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology." *Id.*

D. Domestic Industry

In a patent-based complaint, a violation of section 337 can be found "only if an industry in the United States, relating to the articles protected by the patent . . . concerned, exists or is in the process of being established." 19 U.S.C. § 1337(a)(2). Under Commission precedent, this "domestic industry requirement" of section 337 consists of an economic prong and a technical prong. *See Certain Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm'n Op. at 12-14, 2009 WL 5134139 (U.S.I.T.C. Dec. 2009). The complainant bears the burden of establishing that the domestic industry requirement is satisfied. *See Certain Set-Top Boxes and Components Thereof*, Inv. No. 337-TA-454, Final Initial Determination at 294, 2002 WL 31556392 (U.S.I.T.C. June 21, 2002) (unreviewed by Commission in relevant part).

1. Economic Prong

Section 337(a)(3) sets forth the following economic criteria for determining the existence of a domestic industry in such investigations:

> (3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned –
>
> (A) significant investment in plant and equipment;
> (B) significant employment of labor or capital; or
> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

Given that these criteria are listed in the disjunctive, satisfaction of any one of them will be sufficient to meet the economic prong of the domestic industry requirement. *See Certain Integrated Circuit Chipsets and Prods. Containing Same*, Inv. No. 337-TA-428, Order No. 10, Initial Determination (unreviewed) (May 4, 2000).

2. Technical Prong

The technical prong of the domestic industry requirement is satisfied when the complainant in a patent-based section 337 investigation establishes that it is practicing or exploiting the patents at issue. *See* 19 U.S.C. § 1337(a)(2), (3); *Certain Microsphere Adhesives, Process for Making Same and Prods. Containing Same, Including Self-Stick Repositionable Notes,* Inv. No. 337-TA-366, Comm'n Op. at 8, 1996 WL 1056095 (U.S.I.T.C. Jan. 16, 1996). "The test for satisfying the 'technical prong' of the industry requirement is essentially [the] same as that for infringement, *i.e.*, a comparison of domestic products to the asserted claims." *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). To prevail, the patentee must establish by a preponderance of the evidence that the domestic product practices one or more claims of the patent, either literally or under the doctrine of equivalents. *See Bayer*, 212 F.3d at 1247. It is sufficient to show that the products practice any claim of that patent, not necessarily an asserted claim of that patent. *See Certain Microsphere Adhesives*, Comm'n Op. at 7-16.

E. Claim Preclusion

"Under the doctrine of claim preclusion, 'a judgment 'on the merits' in a prior suit involving the same parties or their privies bars a second suit based on the same cause of action.'" *SimpleAir, Inc. v. Google LLC*, 884 F.3d 1160, 1165 (Fed. Cir. 2018) (citing *Lawlor v. Nat'l Screen Serv. Corp.*, 349 U.S. 322, 326 (1955)). A "cause of action is defined by the transactional facts from which it arises, and the extent of the factual overlap." *Senju Pharm. Co. v. Apotex, Inc.*, 746 F.3d 1344, 1349 (Fed. Cir. 2014) (citing *Acumed LLC v. Stryker Corp.*, 525 F.3d 1319, 1323-1324 (Fed. Cir. 2008)). For purposes of claim preclusion, the scope of a prior cause of action is determined "pragmatically, giving weight to such considerations as whether the facts are related in time, space, origin, or motivation, whether they form a convenient trial unit, and whether their

treatment as a unit conforms to the parties' expectations or business understanding or usage." *Acumed*, 525 F.3d at 1324 (internal citation omitted).

In the patent infringement context, "[c]laim preclusion will generally apply when a patentee seeks to assert the same patent against the same party and the same subject matter." *Senju Pharm. Co.*, 746 F.3d at 1349 (citing *Kearns v. Gen. Motors Corp.*, 94 F.3d 1553, 1557 (Fed. Cir. 1996)); *see Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1341 (Fed. Cir. 2012) (holding two claims which were "not materially different" do not create a new cause of action). "While 'ordinarily' different patents will raise different causes of action . . . that factor is not dispositive and does not substitute for the transactional approach consistently followed by the [Federal Circuit]." *SimpleAir*, 884 F.3d at 1166 (internal citations omitted). "Where different patents are asserted in a first and second suit, a judgment in the first suit will trigger claim preclusion only if the scope of the asserted patent claims in the two suits is essentially the same." *Id.* at 1167. "[T]he claim preclusion analysis requires comparing the patents' claims along with other relevant transactional facts," even though a terminal disclaimer "is a strong clue" that the subsequent patent lacks a patentable distinction over the former. *Id.* at 1168.

F. Issue Preclusion

Issue preclusion is also known as "collateral estoppel" and "like the related doctrine of *res judicata*, serves to 'relieve parties of the cost and vexation of multiple lawsuits, conserve judicial resources, and, by preventing inconsistent decisions, encourage reliance on adjudication.'" *United States v. Mendoza*, 464 U.S. 154, 158 (1984) (citing *Allen v. McCurry*, 449 U.S. 90, 94 (1980)). "Under the doctrine of issue preclusion, also called collateral estoppel, a judgment on the merits in a first suit precludes relitigation in a second suit of issues actually litigated and determined in

the first suit." *In re Freeman*, 30 F.3d 1459, 1465 (Fed. Cir. 1994). The Federal Circuit has explained:

> Indeed, for us not to adopt the same claim construction in a case such as this, in which the construction of the claim term in question was a necessary predicate to the determination of a prior litigation before this court and is evident from the face of the intrinsic record without resort to expert testimony, would run counter to the Supreme Court's guidance on stare decisis in *Markman*: "treating interpretive issues as purely legal will promote (though it will not guarantee) intrajurisdictional certainty through the application of stare decisis." *Markman*, 517 U.S. at 391, 116 S.Ct. 1384.

Miken Composites, L.L.C. v. Wilson Sporting Goods Co., 515 F.3d 1331, 1338, n.* (Fed. Cir. 2008). Accordingly, "where a determination of the scope of patent claims was made in a prior case, and the determination was essential to the judgment there on the issue of infringement, there is collateral estoppel in a later case on the scope of such claims, *i.e.*, the determined scope cannot be changed. *Molinaro v. Fannon/Courier Corp.*, 745 F.2d 651, 655 (Fed. Cir. 1984). Issue preclusion differs from claim preclusion in that "claim preclusion forecloses successive litigation of the same cause of action whether or not relitigation of the cause of action involves the same issues as the earlier suit." *SimpleAir*, 884 F.3d at 1165 (citing *New Hampshire v. Maine*, 532 U.S. 742, 748-9 (2001)).

With that said, "[t]ribunals have discretion to decide whether a particular case is appropriate for application of issue preclusion." *Certain 3G Mobile Handsets and Components Thereof*, Inv. No. 337-TA-613 (remand), Comm'n Op. at 26 (Sep. 21, 2015) ("*3G Mobile Handsets*") (citing *A.B. Dick Co. v. Burroughs Corp.*, 713 F.2d 700, 702 (Fed. Cir. 1983); *Certain Semiconductor Integrated Circuits Using Tungsten Metallization and Products Containing Same*, Inv. No. 337-TA-648, Comm'n Op. at 3 (Feb. 18, 2009) ("*Semiconductor Integrated Circuits*"). The Commission has identified a four factor test for the application of issue preclusion:

> Under Federal Circuit law, the doctrine of issue preclusion can be applied only if: (1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) the plaintiff had a full and fair opportunity to litigate the issue in the first action.

Semiconductor Integrated Circuits, Inv. No. 337-TA-648, Comm'n Op. at 2-3 (citing *In re Freeman*, 30 F.3d at 1465).

"[T]o apply issue preclusion to a claim interpretation issue decided in a prior infringement adjudication, 'the interpretation of the claim had to be the reason for the loss [in the prior case] on the issue of infringement.'" *In re Freeman*, 30 F.3d at 1466 (quoting *Jackson Jordan, Inc. v. Plasser American Corp.*, 747 F.2d 1567, 1577 (Fed. Cir. 1984)). "Only a final judgment holds sway in an analysis of whether issue preclusion applies, even if the final judgment is reached first in a later filed case." *3G Mobile Handsets*, Inv. No. 337-TA-613 (remand), Comm'n Op. at 29 (citing *Chicago, R.I. & P. Ry. V. Schendel*, 270 U.S. 611, 615-17 (1926)). With respect to identity of issues, the Federal Circuit has held "[c]omplete identity of [patent] claims is not required to satisfy the identity-of-issues requirement for claim preclusion." *Soverain Software LLC v. Victoria's Secret Direct Brand Mgmt., LLC*, 778 F.3d 1311, 1319 (Fed. Cir. 2015) (citing *Ohio Willow Wood Co. v. Alps S., LLC*, 735 F.3d 1333, 1342 (Fed. Circ. 2013)). Rather, "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342.

G. Unclean Hands

The doctrine of unclean hands comes from "the equitable maxim that 'he who comes into equity must come with clean hands.'" *Precision Instr. Mfg. Co. v. Auto. Maint. Mach. Co.*, 324 U.S. 806, 814 (1945). Unclean hands only applies "where some unconscionable act of one coming

for relief has immediate and necessary relation to the equity that he seeks in respect of the matter in litigation." *See Gilead Sciences, Inc. v. Merck & Co., Inc.*, 888 F.3d 1231, 1239 (Fed. Cir. 2018), *cert. denied*, 139 S. Ct. 797, 202 L. Ed. 2d 572 (2019) (quoting *Keystone Driller Co. v. Gen Excavator Co.*, 290 U.S. 240, 245 (1933)); *Aptix Corp. v. Quickturn Design Sys., Inc.*, 269 F.3d 1369, 1376 (Fed. Cir. 2001) (quoting same). "Moreover, a finding of unclean hands generally does not prejudice the offending party in subsequent cases, but only provides a bar to relief in the case at hand." *Aptix*, 269 F.3d at 1376. "[T]he 'immediate and necessary relation' standard, in its natural meaning, generally must be met if the conduct normally would enhance the claimant's position regarding legal rights that are important to the litigation if the impropriety is not discovered and corrected." *Gilead*, 888 F.3d at 1240.

IV. U.S. PATENT NO. 9,535,623

A. Overview

Netlist alleges infringement of claims 1-5 and 7-11 of the '623 patent. Claims 2-5 and 7-11 depend from independent claim 1. The asserted claims provide as follows:

> 1. [limitation 1a] A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
>
> [limitation 1b] a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode,
>
> [limitation 1c] wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal

to the memory controller of the host system via the open drain output while the memory module is in the second mode; and

[limitation 1d] a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller,

[limitation 1e] the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

2. The memory module of claim 1, further comprising:

a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed address and control signals to the plurality of synchronous dynamic random access memory elements.

3. The memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.

4. The memory module of claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

5. The memory module of claim 1, wherein the one or more training sequences are executed by the module controller in response to a command or a signal received from the memory controller of the host system.

. . . .

7. The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

> 8. The memory module of claim 7, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
>
> 9. The memory module of claim 7, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
>
> 10. The memory module of claim 7, wherein the notification circuit generates the notification signal using one or more OR logic elements.
>
> 11. The memory module of claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system.

('623 patent at cls. 1-5, 7-11.)

B. Level of Ordinary Skill in the Art

As part of the *Markman* process in this investigation, a prior presiding ALJ determined the level of ordinary skill in the art at the time of invention for the '623 patent is "a person with a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST." (Order No. 17 at 9.) The undersigned has considered the issues relevant to this initial determination in accordance with this definition. The parties each allege they have done the same in their analyses of the issues. (*See* CIB at 79; RIB at 59; SIB at 85.)

C. Claim Construction

Order No. 17 construed the following claim terms relevant to the issues in this initial determination:

Term	Construction
"notification signal indicating [at least one / a] status of [the] one or more training sequences" ('623 patent at cls. 1, 12, 21)	"notification signal" does not encompass polling and "indicating [at least one / a] status of [the] one or more training sequences" is not limited to indicating the completion of a sequence
"one or more training sequences" ('623 patent at cls. 1, 3, 5, 11, 12, 13, 21, 23, 29)	means "one or more operations related to synchronization of a receiver circuit to an incoming data signal"

(Order No. 17 at 137.)

Netlist and Respondents do not identify any discrete claim construction issues beyond those resolved as part of the *Markman* process. (*See* CIB at 79; CRB at 55; RIB at 59; RRB at 37-56; SIB at 85-87; SRB at 22-27.)

D. Infringement

1. Issue Preclusion

Apart from the merits of Netlist's claim of infringement under the '623 patent, Respondents contend "[i]ssue preclusion bars Netlist's claim that Alert_n provides status of any aspect of the accused CA Bus training" in light of determinations made in the prior 1023 Investigation regarding the '837 patent, of which the '623 patent is a continuation. (RIB at 77.) Respondents identify the relevant considerations as whether: "the issue in dispute was (1) 'necessarily decided in the previous proceeding' and is 'identical to the one which is sought to be relitigated'; (2) 'the first proceeding ended with a final judgment on the merits'; and (3) the party against whom issue preclusion is asserted was a 'party or in privity with a party' to the earlier proceeding." (*Id.* at 76 (citing *e.Digital Corp. v. Futurewei Techs., Inc.*, 772 F.3d 723, 726 (Fed. Cir. 2014)).) Respondents explain "Netlist only disputes the first element [of the issue preclusion test] because the 1023 Investigation resulted in a final decision that the same products accused in this

Investigation do not infringe any asserted 837 patent claim, a decision Netlist did not appeal." (*Id.* at 77.) It is important to note at this time that the Commission determined not to review this determination in the 1023 ID, thereby adopting it. *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023, Comm'n Notice (Jan. 16, 2018); *Certain Two-Way Radio Equipment and Systems, Related Software and Components Thereof*, Inv. No. 337-TA-1053, Comm'n Op. at 8 n.4 (Dec. 18, 2018) (public version); 19 C.F.R. § 210.42(h)(2).

More specifically, Respondents advance two grounds of issue preclusion that would necessitate a finding of non-infringement of the '623 patent. First, Respondents reference that portion of the 1023 ID which found non-infringement of the '837 patent over the claim limitation "notification signal indicating . . . at least one status of the at least one initialization sequence." (*Id.* at 77.) Respondents explain:

> The CALJ found the "'ALERT_n signal' generated from the memory module does not indicate a status of the 'Clock-to-CA training mode....'" *Id.* The CALJ reasoned that ALERT_n signals are merely "aggregated data points (*i.e.*, 'LOW' or 'HIGH') that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence." *Id.* at .0102-.0103. "Put differently, these feedback signals [Alert_n] passing through the memory module ***do not amount to a 'status'*** until the memory controller utilizes them to make a status determination." *Id.* at .0103 (emphasis added).

(*Id.* at 77-78 (citing JX-2031C at *102-103).)[2] Respondents add that this issue was fully and fairly litigated between the parties (*id.* at 78 (citations omitted)) and that Netlist uses the same infringement theory now as in the 1023 Investigation—"that ALERT_n indicates the status of

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[2] The 1023 ID is sometimes cited by the parties as JX-2031C, or occasionally by Netlist as CX-2366C.

some aspect of CA Bus training" (*id.* at 78-79 (citing CX-2004C at Q/A 321, 344; Mangione-Smith, Tr. at 310:5-19, 313:10-314:3)). Respondents argue "[b]ut the reasoned and un-contested holdings of the CALJ are that the ALERT_n signals 'do not amount to a 'status'...,' but are just 'aggregated data points (*i.e.*, 'LOW' or 'HIGH') that are feedback signals....'" (*id.* at 79 (citing JX-2031C at *102-103)) such that issue preclusion bars the repeated contention (*id.* (citing *Mycogen Plant Sci., Inc. v. Monsanto Co.*, 252 F.3d 1306, 1310 (Fed. Cir. 2001), *vacated on other grounds*, 535 U.S. 1109 (2002))).

Respondents offer several additional points in anticipation of Netlist's rebuttal. One, Respondents contend that it makes no difference that the '837 patent required a "status" of an "initialization sequence," whereas the '623 patent requires a "status" of a "training sequence," because "the Commission has already held that Alert_n provides no status because Alert_n is data that only the memory controller can use to later to determine status of its CA Bus training. . . . Netlist cannot reargue that Alert_n somehow is status." (*Id.*) Two, according to Respondents, if there is a difference it is immaterial as the 1023 ID previously held that a "training sequence" is included within "initialization sequence." (*See id.* at 79-80 (citing JX-2031C at *98); *see also* RRB at 54 (arguing that the terms need not be "coterminous").) Three, the 1023 ID's finding was not limited to a determination that Alert_n simply did not provide completion status—it determined "ALERT_n signal does not and cannot indicated 'status' at all . . . ." (RIB at 80-81 (citing JX-2031C at *102-103).) The Staff agrees with Respondents' first issue preclusion theory. (*See* SIB at 84.)

Respondents' second ground of issue preclusion concerns the 1023 ID's determination that, in Respondents' words, "the accused RCD does not 'cause' the module to enter CA Bus training." (RIB at 82.) Specifically, according to Respondents, "the Commission found that the memory

controller, not the memory module's RCD, 'caused' the module to enter the CA Bus training mode" through the following passage:

> The RCD of the accused devices does not "cause" the accused products (*i.e.*, memory modules) to enter the "Clock-to-CA" training mode. Rather, the "memory controller" of the accused products causes entry into the accused . . . mode.

(*Id.* (citing JX-2031C at *96, 97).) Respondents continue, "[i]n this Investigation, Netlist contends that the same JEDEC compliant RCD causes the module to enter CA Bus training mode" (*id.* (citing CX-2004C at Q/A 302)) even though "the 837 patent and the 623 patent claim a memory module that cause[s] itself to enter the accused mode" (*id.* at 82-83 (citing '623 patent at cl. 1; '837 patent at cl. 1)). Respondents add, this too was "vigorously contested in the 1023 Investigation." (*Id.* at 83.) The Staff appears to agree with Respondents' second issue preclusion theory. (*See* SIB at 90.) Additionally, on this second ground specifically, Respondents view Netlist as having waived any opposition thereto. (RRB at 55 (citing CPB at 426, 549-550).)

In opposition, and with respect to Respondents' first ground, Netlist states "the 1023 ID did not find that the Accused Products are incapable of indicating a 'status' of anything." (CIB at 93; CRB at 67-68 (citing JX-2031C at *97-98, 102-103; RX-3548C; RX-3783C at *17-18).) Rather, according to Netlist:

> The 1023 ID recognized that "initialization" and "training" are different for the reason set forth in the patent's specification: initialization can include one or more training sequences, but the training sequences are not themselves initialization. *See* Order No. 17 at 137-139; JX-2002 at 6:53-58; RX-3548C at RX-3548C.00027-RX-3548C.00028. In fact, the 1023 ID highlighted the material difference in scope between these terms by analogizing the training sequences to "the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake," which are component parts of—but not themselves—the cake (*i.e.*, the initialization sequence). JX-2031C at JX-2031C.0105; RX-3548C at RX-3548C.00027-.00028.

(CRB at 67-68.) In its reply brief, Netlist also claims Respondents have mischaracterized Netlist's infringement theory in this investigation (*id.* at 66-67) and their second ground of issue preclusion is a mere repetition of their non-infringement position (*id.* at 68).[3]

Here, the undersigned finds issue preclusion prevents consideration of whether, in this investigation, the Accused Products infringe the "notification signal indicating at least one status of one or more training sequences" and "wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system." As noted above, there are four factors to consider before determining an issue in an investigation is precluded: "(1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) the plaintiff had a full and fair opportunity to litigate the issue in the first action." *Semiconductor Integrated Circuits*, Inv. No. 337-TA-648, Comm'n Op. at 2-3 (Feb. 18, 2009).

With respect to "wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system," the undersigned first observes that Netlist effectively offers no opposition to this ground. (CIB at

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[3] The undersigned does observe, however, that Netlist argues in its reply brief (in an infringement section) that Respondents mistakenly "require[] the claim limitation 'configured to cause' from the '837 Patent to be read as the exact equivalent of the claim limitation 'configured to cause . . . in response to a command from the memory controller of the host system' from the '623 Patent." (CRB at 56 (emphasis in original).) To the extent Netlist intends this paragraph to be a rebuttal to Respondents' presentation of issue preclusion, the undersigned finds it is not persuasive and is misplaced because the precluded issue would be whether the module controller "cause[]s the memory module to enter [a second mode / the initialization mode];" and not whether that second/initialization mode is caused because of some identical requisite condition or command.

93; CRB at 68.) There is no dispute to Respondents' claim that the current Accused Products are the same as those at issue in that prior investigation. (RIB at 4.) There can be no dispute that Netlist had a full and fair opportunity in that investigation to litigate whether those products infringed the '837 patent claim limitation "a controller circuit configured to cause the memory module to enter the initialization mode" nor that resolution of that issue was essential to the final judgment in that investigation. (1023 ID at 91-93, 95 ("the evidence of record demonstrates that the RCD of the accused devices does not 'cause' the accused memory modules to enter the 'Clock-to-CA' training mode; rather that occurs by way of the operation of the 'memory controller.'").)

Regarding the remaining factor, "the issue is identical to one decided in the first action," the Federal Circuit has held "[c]omplete identity of [patent] claims is not required to satisfy the identity-of-issues requirement for claim preclusion." *Soverain Software*, 778 F.3d at 1319 (citing *Ohio Willow Wood*, 735 F.3d at 1342). Rather, "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342.

On this last point, the undersigned finds that the limitation of the '837 patent, "a controller circuit configured to cause the memory module to enter the initialization mode" is not materially different from "wherein the module controller is configured to cause the memory module to enter a second mode" in the '623 patent. Claim 1 of the '623 patent recites how the memory module undergoes "training sequences" when in the "second mode" ('623 patent at cl. 1) and the shared specification between the two patents teaches that the "training sequence" is a type or part of "initialization mode" or "initialization sequence":

> As discussed, the memory module **10** is configured to operate in at least two modes comprising an initialization mode during which the memory module **10** executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller **14**. In some embodiments, the controller circuit **18** is configured to cause the memory module **10** to enter the initialization mode. For example, the controller circuit **18** may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller **14** or is otherwise received from the host computer system **16** (e.g., upon receipt of a reset signal).

(*Id.* at 6:50-65.)

Thus, the undersigned finds that it is clear that there is no material difference between "a controller circuit configured to cause the memory module to enter the initialization mode" and "wherein the module controller is configured to cause the memory module to enter a second mode." Issue preclusion, therefore, prevents reconsideration of infringement of this limitation such that there can be no infringement by the Accused Products of claim 1 of the '623 patent or any other asserted claim (all of which depend therefrom).

With respect to "notification signal indicating at least one status of one or more training sequences," the undersigned finds there is likewise no material difference between it and "notification signal . . . indicating at least one status of the at least one initialization sequence" from the '837 patent. Both limitations critically use the same term "status," which the Federal Circuit has instructed should be given the same meaning. *Omega Eng'g Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003) (citing *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)).

There is also little reason to consider "initialization sequence" and "training sequence" to have materially different meanings under *Ohio Willow Wood*. 735 F.3d at 1342. The 1023 ID went so far as to characterize any argument on the relationship between the two as "semantic." (1023 ID at 90.) Order No. 17 in this Investigation stated that the shared specification of the '837 and '623 patents is completely devoid of any technical explanation of what these sequences are apart from repeated references to "training sequences" as a type or subset of "initialization sequences." (*See* Order No. 17 at 132.) These references are as follows:

> Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period . . . .

('623 patent at 4:40-43; '837 patent at 3:36-39);

> In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14.

('623 patent at 6:53-58; '837 patent at 5:46-51);

> [I]n response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences).
>
> . . . .
>
> [I]n response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences).

('623 patent at 7:5-14; '837 patent at 5:65-6:7). Thus, while "initialization sequence" was not explicitly construed in Order No. 17 or in the 1023 Investigation,[4] whatever its meaning it must encompass "training sequences" per the language of the shared specification. This makes it

[4] Order No. 17 did not construe "initialization" as it is not a claim term of the '623 patent. The 1023 ID also did not construe "initialization" apart from finding the accused "'Clock-to-CA' training" was such. (1023 ID at 90-91.)

difficult to view "a notification signal indicating at least one status of one or more training sequences" as presenting a fresh question once it has been determined there is no "notification signal . . . indicating at least one status of the at least one initialization sequence" in any accused product.

Netlist's observation that the two are "not coterminous" (CIB at 93) does not disturb this outcome. Again, the test is not exact identity but rather "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342. That court explained:

> As reflected in the claim language above, these patents use slightly different language to describe substantially the same invention. For example, where the '237 patent recites a "tube sock-shaped covering," an "amputation stump being a residual limb," and "fabric in the shape of a tube sock," the '182 patent analogously recites the same claim scope in the form of a "cushion liner for enclosing an amputation stump, said liner comprising a fabric covering having an open end for introduction of said stump and a closed end opposite said open end." Thus, the mere use of different words in these portions of the claims does not create a new issue of invalidity.

Id. at 1342-43. Indeed, much like the patentee in *Ohio Willow Wood*, Netlist's argument is deficiently limited to declaring "initialization" and "training" as different because "initialization can include one or more training sequences, but the training sequences are not themselves initialization" (CRB at 67) without explaining why this is significant:

> It is undisputed that the adjudicated claims of the '182 patent only require a "polymeric" gel whereas the unadjudicated claims of the '237 patent specifically require a "block copolymer" gel. OWW argues that this difference in claim scope precludes summary judgment. But OWW has not adequately supported this contention because it has not provided any explanation regarding *how* the "block copolymer" limitation is patentably significant in view of the obviousness determination regarding the claims of the '182 patent.

> Since OWW failed to explain how the "block copolymer" limitation changes the invalidity analysis, OWW has not met its burden of opposing summary judgment based on this distinction.

735 F.3d at 1343. In fact, the terms "polymeric" and "block copolymer" in *Ohio Willow Wood* have the same relationship as "initialization sequence" and "training sequence," wherein the latter is a subset of the former.

Additionally, it is important to address Netlist's claim that the 1023 ID actually "highlighted the material difference in scope between these terms." (CRB at 67-68.) To be clear, Netlist states:

> In fact, as already discussed, the 1023 ID highlighted the material difference in scope between these terms by analogizing the training sequences to "the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake," which are component parts of—but not themselves—the cake (*i.e.*, the initialization sequence). JX-2031C at JX-2031C.0105; RX-3548C at RX-3548C.00027-.00028.

(*Id.*) First and foremost, this is a mischaracterization of the 1023 ID. In the 1023 ID, the undersigned explained how the "notification signal" was not a "status" with the following analogy:

> By way of analogy, placing all of the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake in a shopping bag (*i.e.*, the memory module) at the grocery store does not transform them into a cake; that only occurs when they are blended and transferred into the oven and baked (*i.e.*, the memory controller).

(1023 ID at 96.) Clearly, in this analogy it is the ALERT_n signals which are the ingredients and do not become a status (cake) until they are received and processed (baked) by the external system memory controller (oven)—and not training sequences as the ingredients of an initialization sequence.

Second, even if the 1023 ID had analogized "training sequences" to be an ingredient of "initialization sequences," this only serves to repeat that principle which the shared specification already discloses—an initialization sequence can comprise one or more training sequences. ('837 patent at 5:64-67, 6:4-7; '623 patent at 7:4-7, 7:11-14.) This is not an explanation of why a switch from "initialization sequence" to "training sequence" materially alters the question of infringement.

Lastly, even if "initialization sequence" and "training sequence" had radically different meanings (*e.g.*, non-overlapping), replacing the former with the latter has only a minimal effect on the claimed invention. The technical character of these sequences does not have any bearing on any other recited feature. For example, "initialization sequence" is recited in claim 1 of the '837 patent as something the memory module performs and to which the notification signal corresponds, with no other feature or component affected:

1. A memory module comprising:

> at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module *executes at least one initialization sequence* and an operational mode;
>
> a controller circuit configured to cause the memory module to enter the initialization mode; and
>
> a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller *indicating at least one status of the at least one initialization sequence*; and
>
> wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

('837 patent at cl. 1 (emphasis added).) Claims 2, 3, 6, 7, 10, 14, and 17 all use "initialization sequence" in the same isolated way.

The '623 patent claims likewise use "training sequences" as a process the memory module must perform but the substance of that process does not affect any other feature:

> 1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
>
> a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating *a notification signal indicating at least one status of one or more training sequences* while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
>
> a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

('623 patent at cl. 1 (emphasis added).) Claims 3, 5, 11-13, 21, 23, and 29, again, all use "training sequence" without regard to what that sequence actually entails.

This finding is buttressed by Order No. 17 which analyzed how "initialization" and "training" are used across the '837 and '623 patents and concluded they are effectively interchangeable as far as the invention was concerned. The Order stated:

> For this limitation, I find an overall lack of intrinsic evidence to explain the meaning of "training sequences." Neither it nor "initialization sequence" are given any technical definition in the '623 patent specification apart from referring to "initialization sequence (*e.g.*, comprising one or more training sequences)" ('623 patent at 6:55-57), or "initialization sequence (*e.g.*, one or more training sequences)" (*id.* at 7:7-8). This is acknowledged by all parties. (CIMB at 59; RIMB at 9-10; SRMB at 43.)
>
> The '623 patent also introduces a "training *mode*" in its claims to characterize the second mode of the memory module which is not the normal operational mode. ('623 patent at cls. 4, 14, 22.) This is interesting because the specification never uses this term, opting instead for "initialization mode," which it uses twenty-four times to refer to the same mode—that which is not the normal operational mode. ('623 patent at 5:13-26, 6:50-65, 7:34-47, 8:30-33, 8:46-53, 8:54-9:16, 9:55-61, 10:7-11, 12:6-23, 12:33-37, 12:41-43, 12:57-63, 12:66-13:5, 13:30-36.) No prior family members use "training mode" in their specifications or claims either. (*See generally* '837 patent; '116 patent.) I find this sudden and complete switch suggests interchangeability between "initialization" and "training" as far as the invention of the '623 patent is concerned. In total, the intrinsic evidence communicates that "training" and "initialization" are, broadly, those processes and operations the memory module undergoes when it is not in normal operational mode to prepare for operational mode.

(Order No. 17 at 132.)

The undersigned agrees with these observations of Order No. 17 and hereby determines that the meanings of "initialization sequence" and "training sequence" simply have minimal importance to the inventions of the '837 and '623 patents and minimal impact on the infringement analyses associated therewith such that the test under *Ohio Willow Wood* is satisfied. As there is no dispute as to the other three factors (actually litigated, essential to prior judgment, full and fair

opportunity) (*see* CIB at 93; CRB at 66-68), the undersigned finds issue preclusion prevents reconsideration of infringement of this limitation such that there can be no infringement by the Accused Products of claim 1 of the '623 patent or any other asserted claim of that patent (all of which depend therefrom).

2. Independent Claim 1

Should the Commission not agree issue preclusion applies, the merits of Netlist's claim of infringement under the '623 patent are discussed below, and the undersigned finds that the Accused Products do not literally infringe claim 1 of the '623 patent.

a) Undisputed Limitations

To facilitate the infringement discussion, Netlist has assigned identifiers to each limitation of independent claim 1 of the '623 patent. (*See* CIB at xxii-xxiii.) With reference to these identifiers, Netlist contends that there is no dispute over the infringement of limitations 1a, 1b, and 1d by the Accused Products. (CIB at 79, 80, 92.) Netlist cites to the written testimony of its expert, Dr. Mangione-Smith, to fulfill its obligation in establishing the Accused Products include these limitations. (CIB at 79 (citing CX-2004C at Q/A 256-285, 705-771, 847, 849-859, 926), 80 (citing CX-2004C at Q/A 286-297, 705-765, 772-778, 847, 849-855, 860-865, 926), 92 (citing CX-2004C at Q/A 344-360).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 60-75; RRB at 37-53; SIB at 87-93; SRB at 22-26.) The undersigned notes here that, again, Netlist omits discussion of limitation 1e of the '623 patent, but appears to treat it alongside limitation 1d through citation to expert testimony which covers both limitations.

(*Compare* CIB at xxi *with* CIB at 92; CX-2004C at Q/A 344-360 (covering limitations 1d and 1e).)[5]

In view of the testimony of Dr. Mangione-Smith that the Accused Products include these limitations, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these features of independent claim 1. (*See* CX-2004C at Q/A 256-285, 705-771, 847, 849-859, 926, 286-297, 705-765, 772-778, 847, 849-855, 860-865, 926, 344-360.)

Infringement of limitation 1c is disputed in-part. This limitation reads:

> wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode;

('907 patent at cl. 1.) Within this limitation, Netlist identifies only "the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system" and "the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode" as in dispute between the parties. (*See* CIB at 80, 83.) Accordingly, these portions are discussed further below. With respect to the remaining portion, Netlist cites to the written testimony of Dr. Mangione-Smith to fulfill its obligation in establishing it is present in the Accused Products. (CIB at 92 (citing CX-2004C at Q/A 298-347).) Respondents and Staff do not

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[5] The undersigned notes that the numbering of Q344-347 is used twice in CX-2004C. The noted citation refers to the second usage of Q344-347.

appear to dispute this evidence or Netlist's contention. (RIB at 59-75; RRB at 37-53; SIB at 87-93; SRB at 22-26.)

In view of the testimony of Dr. Mangione-Smith that the Accused Products include these portions, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these features of independent claim 1. (*See* CX-2004C at Q/A 298-347.)

b) Disputed Limitations

As noted above, there is a dispute as to whether the Accused Products meet two portions of limitation 1c of independent claim 1 of the '623 patent. As discussed below in more detail, the undersigned finds that the Accused Products do not include "wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system" or "the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode."

> (1) "wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system"

For the "cause the memory module to enter a second mode" limitation, Netlist claims "[t]he JEDEC-compliant RCDs in the Accused Products include an RC0C training control word register, the value of which determines the operating mode of the memory module (*e.g.*, Clock-to-CA Training Mode)." (CIB at 80 (citing CX-2004C at Q/A 302).) Netlist continues:

> For the memory module to enter Clock-to-CA Training Mode (the claimed "second mode"), the RCD first receives a 13-bit "control word" from the memory controller (the claimed "command"). *Id.* at Q/A 303-304; Tr. (Wedig) at 609:24-610:1. This 13-bit control word is an instruction to the RCD, which the RCD decodes using its

> own internal logic. *Id.* at Q/A 305; Tr. (Mangione-Smith) at 360:25-361:9; Tr. (Wedig) at 610:1-611:19. Then, using its own internal logic, the RCD writes 4-bits to its RC0C register. CX-2004C (Mangione-Smith) at Q/A 306-307; Tr. (Mangione-Smith) at 361:10-16; Tr. (Wedig) at 610:1-611:19. Writing x000 places the module in a normal operating mode; writing x001 places the module in the Clock-to-Ca Training Mode. CX-2004C (Mangione-Smith) at Q/A 302.

(*Id.* at 80-81.) Netlist adds, "the mode of operation of the memory module does not, and cannot, change until the RCD receives the 13-bit control word—an instruction or command—from the memory controller, decodes that word suing its own internal logic, and then write the 4-bit training control word into its internal RC0C register." (*Id.* at 81 (citing CX-2004C at Q/A 307-311; Mangione-Smith, Tr. at 361:17-20, 362:20-363:2; Wedig, Tr. at 612:1-22).) Netlist states clearly, "the memory controller cannot and does not program the RC0C register; instead, the RCD on the Accused Products does this" and "[t]he mode of operation of the memory module does not, and cannot, change until the RCD receives the 13-bit control word—an instruction or command—from the memory controller, decodes that word using its own internal logic, and then writes the 4-bit training control word into its internal RC0C register." (CRB at 58-59 (citations omitted).)

Netlist asserts that Respondents' opposition to this "cause" limitation is rooted in "a mistaken belief that the unconstrued claim term 'cause' can only mean 'original cause,' 'deciding factor,' or 'decide.'" (CIB at 82 (citing Wedig, Tr. at 605:20-606:7; CX-2004C at Q/A 317-320; 969-974); CRB at 57-58.) Netlist cites several dictionaries to show this is an incorrect interpretation of the plain and ordinary meaning (CIB at 82 (citations omitted)), and views Respondents' expert, Dr. Wedig, as "admit[ting] the Accused Products, not the memory controller, 'choose' (*i.e.*, decide) to operate in Clock-to-CA Training Mode" (*id.* (citing Wedig, Tr. at 581:11-14)). Netlist then suggests that "cause" in the '837 patent from the 1023 Investigation should be read differently than "cause" in the '623 patent, because the relevant limitation in the '623 patent

includes the following additional underlined language—"the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system." (*See id.* at 82-83 (citing '623 patent at cl. 1; Mangione-Smith, Tr. at 359:13-23; Wedig, Tr. at 605:4-12; 597:10-598:20); CRB at 56-57.) On this point in particular, Netlist argues "[i]n the '623 Patent, the module controller cannot 'cause' until it receives the command to do so. . . . In the '837 Patent, there was no such predicate action required, and thus the module controller had to 'cause' on its own." (CRB at 60.)

In opposition, and as discussed above, Respondents view the 1023 Investigation as conclusively establishing that the module controller does not "cause" itself to enter CA Bus training mode, as it is actually the memory controller which causes this. (RIB at 60; *see id.* at 65-66 (citing JX-2031C at *99; RX-1587C at Q/A 20[]4-20[]5); RRB at 45-46.) Apart from the 1023 Investigation, and on the nature of Alert_n's use in the system, Respondents explain:

> The host's memory controller causes itself to enter the CA Bus training and the JEDEC standard provides the memory controller can then cause the RCD to participate in the memory controller's training when the memory controller programs the control word into the "RC0C" register in the module's RCD. CX-0417 (or RX-2148) at Table 22; CX-2220 (or RX-0320) at Table 27; RX-3870C at Q/A 217. The memory controller first enters CA Bus training and then causes the memory module to both enter, and exit, the CA Bus training mode. *Id.* In particular, once the memory controller is in its CA Bus training mode, the memory controller takes control over the memory module by setting the control word to x001 and transmitting it to the RCD. *Id.*; *see also* CX-0417 (or RX-2148) at Table 35; CX-2220 (or RX-0320) at Table 44. If the memory controller did not send this control word for CA Bus training, the memory module would not enter the CA Bus training mode.

(*Id.* at 66.) Respondents emphasize how Dr. Mangione-Smith in the 1023 Investigation testified it is this control word which causes the memory module to enter the initialization (*i.e.*, training or second) mode. (*Id.* (citing CX-0005 at Q/A 1334; Mangione-Smith, Tr. at 308:15; JX-2031C at *99).) Respondents add that, to the extent it is attempted, Netlist has waived any argument that

"cause" should receive different meanings between the '837 and '623 patents (RIB at 67-68; RRB at 47-48) and that such argument is otherwise contrary to law and the intrinsic evidence (*id.* at 68-70 (citing, *inter alia*, *Aventis Pharma.*, 675 F.3d at 1330; RX-3870C at Q/A 221-232); RRB at 48-49). In their reply brief, Respondents dispute that Dr. Wedig "admitted the accused products satisfy the cause limitation because they can choose to operate in the accused mode." (RRB at 49 (citing CIB at 82; Wedig, Tr. at 581:11-14).) Respondents claim this testimony was simply an observation that "the accused products can be configured/chose [sic] to implement CA Bus training or not to do it all." (*Id.* (citing CX-0890 at *9).) The Staff appears to agree with Respondents' position on this limitation. (*See* SIB at 88-90.)

Here, and apart from the identity of issue between this limitation and "a controller circuit configured to cause the memory module to enter the initialization mode" of the '837 patent resulting in issue preclusion as discussed and determined above, it is notable that the Commission has itself determined, through its non-review of the relevant portions of the 1023 ID, that it is the memory controller of the Accused Products which "causes" the memory module to enter the "second mode." (1023 ID at 92; *Two-Way* Radio, Inv. No. 337-TA-1053, Comm'n Op. at 8 n.4; 19 C.F.R. § 210.42(h)(2).) More specifically, the Commission determined "the 'memory controller' controls when to enter/exist the accused 'initialization mode' with control words and sets the registers in the memory module." (1023 ID at 92.) In doing so, the Commission rejected Netlist's position that it is the memory module's RCD which causes entrance to the initialization mode. (*Id.* at 91.)

The present record confirms this is the operation of the Accused Products. The parties agree that to initiate Clock-to-CA training (*i.e.*, CA Bus training), the memory controller sends a 13-bit training control word to the RCD, which is decoded by the RCD, and using its own logic

writes a 4-bit training word into its RC0C register; wherein that 4-bit training word is what triggers Clock-to-CA training by the module. (CRB at 58-59; RIB at 57, 66.)

The evidence would show, however, that that 4-bit control word is nothing more than the final 4 bits of the 13-bit control word coming from system memory controller. This is shown in the JEDEC specification (CX-0417) by the following tables' identification of "DA[3:0]":

Table 22 — Control Word Decoding

Control word	Address Bit													Meaning
	12[1]	11	10	9	8	7	6	5	4	3	2	1	0	
RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Global Features Control Word
RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Clock Driver Enable Control Word
RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Timing and IBT Control Word
RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				CA and CS Signals Driver Characteristics Control Word
RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				ODT and CKE Signals DriverCharacteristics Control Word
RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Clock Driver Characteristics Control Word
RC06	0	0	0	0	0	0	1	1	0	command3:0]				Command Space Control Word
RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use
RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Input Output Configuration Control Word
RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Power Saving Settings Control Word
RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				RDIMM Operating Speed
RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Operating Voltage VDD and VREF Source Control Word
RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Training Control Word
RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				DIMM Configuration Control Word
RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Parity Control Word
RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Command Latency Adder Control Word
RC1x	0	0	0	0	1	setting[7:0]								Internal Vref Control Word
RC2x	0	0	0	1	0	setting[7:0]								I^2C Bus Control Word

Table 35 — RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

(CX-0417 at -68347, Table 22 (excerpted and annotated), -68352, Table 35 (annotated).) If the memory controller's DA[3:0] bits are x000, the memory module will be in "normal operating

mode" (in which read/write operations occur); and if those bits are x001, the memory module be in "Clock-to-CA training mode" (the "second mode"). (*Id.* at -68352, Table 35.) Thus, the memory controller has direct control over, and thus causes, when the memory module enters the second mode.

This is interpretation of "cause" is supported by the '623 patent's teaching of embodiments where the memory controller controls when the memory module enters or exits modes:

> The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14.

('623 patent at 6:55-58);

> In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16.

(*id.* at 8:25-29);

> [E]xecution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode.

(*id.* at 8:46-49).

Again, there is no dispute that the memory controller determines when the Accused Products enter the "second mode." Accordingly, the undersigned finds Netlist has not shown the Accused Products include this limitation of independent claim 1.

> (2) "the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode"

For the "a notification signal indicating at least one status of one or more training sequences" limitation, Netlist argues "the function of the RCD's ALERT_n signal and pin during a single training sequence within the larger Clock-to-CA Training Mode satisfies this element.

(CIB at 83 (citing CX-2004C at Q/A 322).) Netlist explains "the entire Clock-to-CA Training Mode assists the memory controller to align its incoming command, address, and control signals optimally to the clock signal to ensure reliability when reading data from and writing data to memory modules." (*Id.* (citing CX-2004C at Q/A 323).) Netlist further explains how this is accomplished through communication of series of ones zeros and a clock signal from the memory controller to the RCD circuit, wherein the RCD samples the series according to the clock signal, and "logically 'ORs' the sampled signals" to generate a single-bit output of zero or one. (*Id.* at 84 (citations omitted).) Netlist describes this as an "eye opening operation" and how that single-bit output is communicated back to the memory controller "via the open drain output ALERT_n." (*Id.* (citing (CX-2004C at Q/A 288, 330-331, 345).) Importantly, Netlist describes the foregoing as "the claimed training sequence." (*Id.* (citing CX-2004C at Q/A 332, 344).)

Returning to that single-bit ALERT_n output, Netlist argues its value "indicates to the memory controller whether (1) the memory module was able to successfully sample or read all of the enabled Dn inputs as zero (*i.e.*, ALERT_n = low or 0), or (2) the memory module failed to correctly sample or read all of the enabled Dn inputs as zero (*i.e.*, ALERT_n = high or 1)." (*Id.* (citing CX-2004C at Q/A 331, 333, 344; CX-047 at *54-55); *see* CRB at 61.) According to Netlist, if the ALERT_n = 0 that is an "indication" that the memory controller and RCD circuit are "synchronized," whereas ALERT_n = 1 "indicates" they are "unsynchronized." (CIB at 84-85 (citing CX-2004C at Q/A 331, 333, 344).)

Netlist views Respondents' opposition to this limitation as consisting of four arguments that have no merit. First, Netlist contends there is no requirement in the claim for "handshaking, handing off control, or executing independent operations" as part of the "notification signal"; and even if there were, "the memory controller passes off the 'eye opening' operations (the training

sequences) to the memory module." (*Id.* at 85-86 (citing CX-2004C at Q/A 939-946; CX-0417 at *54-55); *see* CRB at 63.) Second, Netlist argues the ALERT_n signal is not a "polled" signal (which would not fall under the claim according to Order No. 17), a finding otherwise conclusively established by the 1023 ID (CIB at 87 (citing CX-2366C at *102-103); CRB at 63-64), but also because "[t]here [is] no request or query from the memory controller to the memory module during an eye opening operation" (CIB at 88 (citing CX-2004C at Q/A 951-956; RX-3870C at Q/A 158; Wedig, Tr. at 591:8-20, 613:9-614:12)).

Third, Netlist disputes that the RCD needs to "know" what the status is in order to indicate it. (CIB at 88 (citing CX-2004C at Q/A 957-962); *see* CRB at 63.) Netlist views "[t]he relevant inquiry [as] whether the memory controller knows what status the RCD is going to send. The answer is 'no.'" (CIB at 88 (citing Wedig, Tr. at 617:5-9).) Relatedly, Netlist disputes that ALERT_n is a mere "loop back of the signal sent of the single, enabled Dn line" and argues it can be sent in reference to multiple Dn signals at the same time. (*Id.* at 89 (citing CX-0417 at *54-55; RX-3870C at Q/A 115; Wedig, Tr. at 613:10-19).) Netlist further contends Respondents' expert, Dr. Wedig, misrepresents the JEDEC standards under which the Accused Products operate as allowing for initiation of the training sequence via a series of all zeros as opposed to all ones. (*Id.* (citing RX-3870C at Q/A 125-129, 179-196; CX-0417 at *54-55; Wedig, Tr. at 619:5-14).) Netlist explains how, in its view, Respondents' improper interpretation of the standard would defeat the entire purpose of Clock-to-CA training. (*Id.* at 89-90 (citing, *inter alia*, CX-2004C at Q/A 336-343; Wedig, Tr. at 616:7-23; Mangione-Smith, Tr. at 365:3-15).)

Fourth, Netlist argues the Clock-to-CA Training Mode is indeed a "training sequence" as the term was construed by Order No. 17—"synchronization of a receiver circuit to an incoming data signal." (*Id.* at 91 (citing CX-2004C at Q/A 963-966; CX-0417 at *54-55; Wedig, Tr. at

595:13-596:11).) Netlist disputes that the mode does not somehow involve data signals or receivers, as the series of ones and zeros on the Dn lines are "hits of data" (*id.* (citing Wedig, Tr. at 613:8-614:12)) and the memory module is a "receiving component[]" (*id.*; CRB at 64).

In its reply brief, Netlist repeats its position discussed above that the 1023 Investigation "did not find that the Accused Products are incapable of indicating a 'status' of anything. Instead the ALERT_n signal provides information related to discrete eye opening(s)—the one or more training sequences in this Investigation—but not information relating to the entirety of Clock-to-CA Training Mode, *i.e.*, an 'initialization sequence.'" (CRB at 60 (citing JX-2031C at *102).) Similarly, Netlist claims "training sequence" and "initialization sequence" are "two very different things." (*Id.*)

Netlist also contends any argument that ALERT_n = 0 may nonetheless result in system failure if the Dn samplings were taken in non-optimal eye opening regions is untimely under Ground Rule 9.2 (CRB at 61) and technically incorrect as well (*id.* at 62). On this, Netlist argues:

> But Netlist does not allege, and the JEDEC specification certainly does not state, that the training stops after a single eye opening sequence that results in successful communication as Respondents argument would require to be accurate. *Id.*; CX-0417 at CX-0417.00054-55.Instead, each individual training sequence provides the status (success or failure) for that specific sampling of Dn inputs and clock position. *Id.* As the CALJ found in the 1023 ID, for the purposes of the entire initialization sequence, the memory controller then takes the result of many of these individual training sequences to determine where the eye opening starts and ends. JX-2031C at JX-2031C.0102-03. In the case of a zero returned in a "metastable region," the zero still indicates that the particular clock position resulted in successful read of the Dn inputs (*see* CIPHB at 82-85). The fact that the metastable is not an ideal location for normal operation is beside the point.

(CRB at 62.)

In opposition, Respondents describe the CA Bus training mode (*i.e.* Clock-to-CA training) as something the memory controller controls on its own—"it controls its own training of its own

signals and clock rather than handing off training to the memory module." (RIB at 59 (citing RX-3870C at Q/A 39-42, 145-148).) Again, as discussed above, Respondents view the 1023 Investigation as conclusively establishing that Alert_n "is incapable of indicating status of the training; it simply provides information that the memory controller, along with the other information only the controller possesses, uses to determine status." (*Id.* at 60; *see id.* at 60-61 (citing JX-2031 at *102-103; RX-3870C at Q/A 165-166, 286-287; Wedig, Tr. at 627:2-18, 633:20, 631:5-362:12 [sic]); RRB at 38-39 ("the Commission already ruled Alert_n does not provide the status of the 'eye-opening' operations, whether they are equated to initialization or training sequences.").) Apart from the 1023 Investigation, and on the nature of Alert_n's use in the system, Respondents explain their view that:

> To determine status, the memory controller must (along with other actions): (1) compare the returned ALERT_n pin value with the Dn values that the memory controller sent, (2) use this comparison along with previous comparisons and any phase shifts of the memory controller's Dn signals to determine the position of the beginning, middle or endpoint of an eye opening, and (3) use this information along with any prior identification of the other endpoint of an "eye opening" to determine whether a sampled signal is the start or the end of an "eye opening." RX-3870C at Q/A 170-172, 197-198. In doing so, the memory controller keeps track of the Dn values sent by the memory controller along with the phase difference between the Dn and the clock at each iteration. *Id.* All of this information is known only to the memory controller and only the memory controller is able to determine whether the RCD's sample, the Alert_n value, is within or outside the eye, in the metastable region, and ultimately whether the clock and Dn signals are successfully synchronized such that the sampling was done correctly. *See id.*; CX-0417 (RX-2148), JEDEC RCD01 Specification at SKH_JEDEC_0068334-35; CX-2220 (RX-0320), JEDEC RCD02 Specification at SKH_JEDEC_0068144-46; RX-1587C at Q/A 102-130, 235-249.

(*Id.* at 61-62.) Respondents proffer that all experts agree a 1 or 0 value for Alert_n "does not indicate whether the RCD sampled the Dn signals successfully inside or outside the eye such that the clock and Dn signals are synchronized." (*Id.* at 62-63 (citations omitted); *see generally id.* at

63-65; RRB at 39-45.) Respondents also discuss how the RCD standard can call for the training of an individual Dn signals, as opposed to several collectively, and this shows the memory module "is merely a slave that samples and returns back the incoming Dn signal(s)." (RRB at 42 (citing RX-3870C at Q/A 194-195; Mangione-Smith, Tr. at 329:1-24); *see generally* RIB at 58 (citing CX-0417 at 44; CX-2220 at 45; RX-3870C at Q/A 112, 115, 116; RX-4089C through RX-4100C).)

Respondents further argue there is no "notification signal" either, as this is "a specific type of handshaking signal [and] the Accused Products do not handoff training and thus do not require any handshake signal, just like the prior art the 623 patent disparages." (RIB at 60; *see id.* at 70-71 (citing RX-3870C at Q/A 140-141, 152, 282-285; Wedig, Tr. at 621:14-25); RRB at 50-51.) Respondents also look to the '623 patent specification as supporting a distinction between handshaking and complete control by a system memory controller. (RIB at 71 (citing '623 patent at 3:55-67; RX-3870C at Q/A 39-40, 42-43, 145-148; RX-1587C at Q/A 141; JX-0029C at 328:19-332:10).) In sum, Respondents claim:

> The memory controller has full control over CA Bus training because it effectively provides, schedules, and knows exactly when it will receive the feedback signals (Alert_n) from the memory module, *i.e.*, three clock cycles after sending the Dn signals, and makes all phase shift adjustments between the clock and Dn signals. CX-0417 (or RX-2148) at 44; CX-2220 (or RX-0320) at 44; RX-3870C at Q/A 282-285. In fact, the memory controller's clock signal instructs the memory module when to read (*i.e.*, samples) the memory controller's Dn signals (*i.e.*, the rising edge of the clock signal) being trained. CX-0417 (or RX-2148) at 44-45 (SKH_JEDEC_0068334-35); CX-2220 (or RX-0320) at 44-46 (SKH_JEDEC_0068144-46). IDT, who manufactures the accused RCD, testified that tbe RCD is merely a slave that does not execute any training. *See, e.g.*, JX-2022C at 69-70, 72. The CA Bus training is performed primarily, if not entirely, by the memory controller. RX-3870C at Q/A 147. That is because the memory controller is intimately conducting the training. *See* JX-2033C at 401:12-402:20 (Mangione-Smith); RX-3870C at Q/A 149-154.

(*Id.* at 71-72.) Nonetheless, Respondents continue, if Alert_n is viewed as handshaking, it is "at best a polled, not a notification, signal" which is not covered by the limitation as construed by Order No. 17. (*Id.* at 60; *see id.* at 72-74 (citing, *inter alia*, RX-3870C at Q/A 156-164, 280-290; RX-2460 at 64:22-65:2; Wedig, Tr. at 625:23-626:12; Mangione-Smith, Tr. at 347:4-6; CX-0417 at 44; CX-2220 at 44); RRB at 51-53.) The Staff appears to agree with this assessment. (*See* SIB at 87-88.)

Lastly, Respondents challenge the notion that CA Bus training meets "synchronization of a receiver circuit to an incoming data signal" (Order No. 17's construction of "training sequence") because "CA Bus training trains control, command and address signals, not data signals." (*Id.* at 60; *see id.* at 74-75 (citing, *inter alia*, CX-2004C at Q/A 55-57, 323; RX-3870C at Q/A 212; CX-0417 at 44; CX-2220 at 44; RX-1587C at Q/A 226; JX-2033C at 405:13-20, 407:4-13); RRB at 53.)

Here, and apart from the identity of issue between this limitation and "notification signal indicating . . . at least one status of the at least one initialization sequence" of the '837 patent resulting in issue preclusion, the Commission has already determined, through non-review of the 1023 ID, that the ALERT_n signal contained in the Accused Products "does not indicate a status of the 'Clock-to-CA' training mode[] and, instead, that only the memory controller provides status information regarding the initialization sequence [(*i.e.* the 'second mode')]." (1023 ID at 95.) More specifically, the Commission determined "the information provided by the 'ALERT_n signal' [] is aggregated data points (*i.e.*, 'LOW' or 'HIGH') that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence." (*Id.* at 95-96.) In doing so, the Commission refuted Netlist's theory "that 'ALERT_n

signal' of the accused products 'indicates to the memory controller (1) when the 'eye opening' has started, (2) when Clock-to-CA training is seeking the ending boundary of the 'eye opening,' and (3) when the ending boundary of the 'eye opening' has been found.'" (*Id.* at 94.)

The present record confirms this is the nature of the ALERT_n signal in the Accused Products and supports the same finding that ALERT_n is not a "status" of a "training sequence." The JEDEC specification Netlist relies on to show the operation of the Accused Products details the manner in which ALERT_n is generated and then used by the system memory controller. (CX-0417 at *54-55; *see* CX-0417 at -68334-68335.) For the avoidance of any confusion, the relevant portion of the specification is reproduced below:

2.12 CA Bus Training Modes

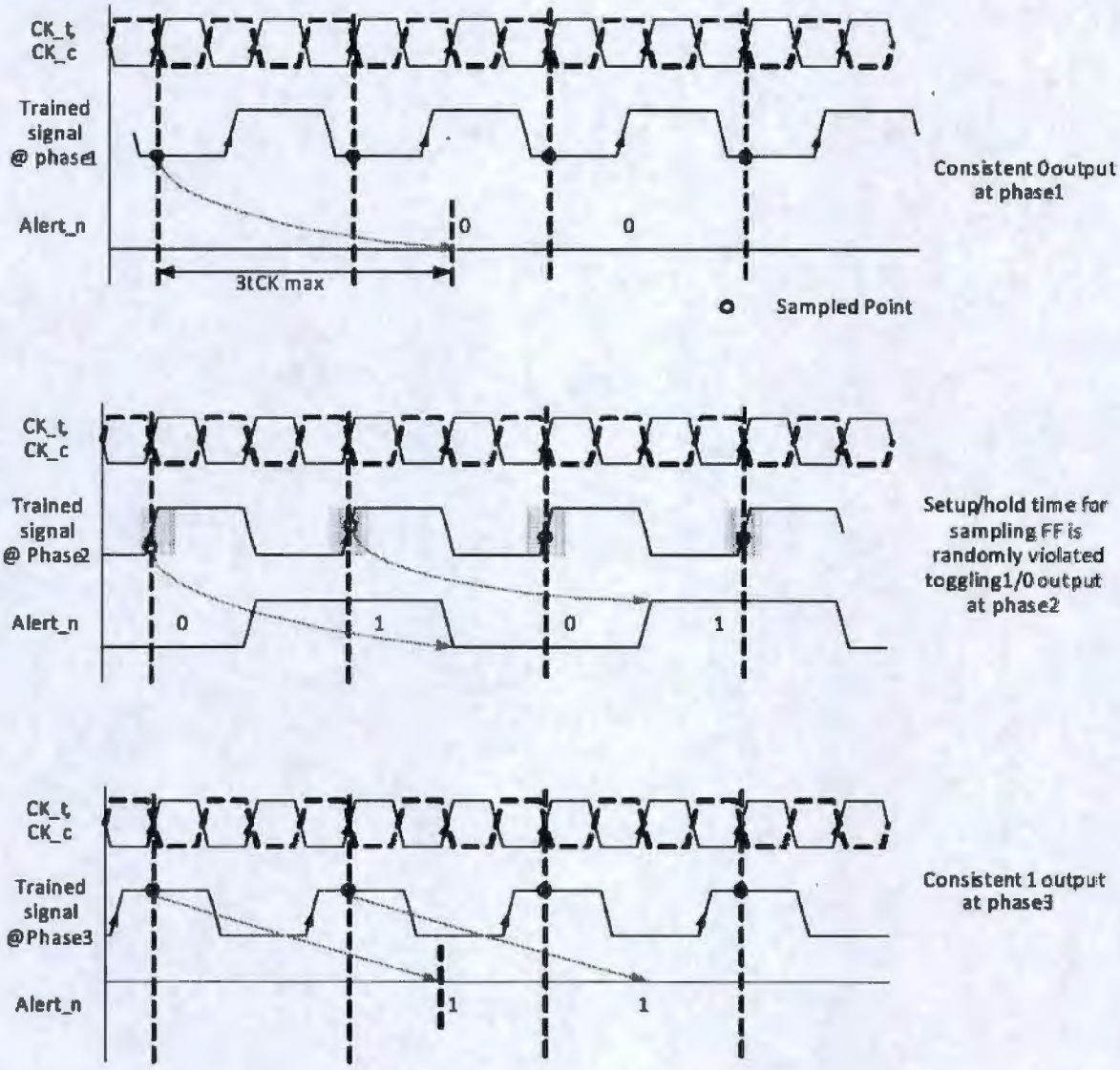
The DDR4RCD01 supports several training modes (selected in Table 35, "RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD01 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD01 to adjust the CK_t-CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS-DQS_n to CK_t-CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD01 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD01 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

2.12 CA Bus Training Modes (cont'd)



(CX-0417 at -68334-68335.)

As described and shown, the Clock-to-CA training involves several steps. At all points in the process, the memory controller writes consecutive 1s and 0s to the sampled Dn input line (*i.e.*, alternating 1 and 0 to align with sampling at every other clock cycle (*see* CX-0417 at -68352, Table 35 ("1. In these training modes, the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).")). The inputs are sampled by the memory module (read as 1 or 0) and fed into a OR function whose output

is ALERT_n. If all samples are read as 0, then ALERT_n is LOW (*i.e.*, 0). If at least one sample is read as a 1, then ALERT_n is HIGH (*i.e.*, 1).

The process begins with the phase of the clock signal (or the inputs) being "pull[ed]" or shifted by the memory controller until ALERT_n registers LOW (*i.e.*, every sample is read as a 0). This moment is used as a "start position" or starting point for determination of the eye opening location, in that the start position is considered a first boundary of that eye opening. (CX-0417 at Section 2.12, first waveform image.) The process is continued by the memory controller further pulling or shifting the phase of the clock signal (or the inputs) until ALERT_n registers HIGH (*i.e.*, at least one sample is read as a 1) *for a continuous three alternating clock cycles*. This moment is used as the "end position" or ending point of the eye opening, in that the end position is considered the opposite boundary of that eye opening. (CX-0417 at Section 2.12, third waveform image.) Then, importantly, the memory controller makes a final pull or shift so as to place the clock cycle edge in between the two boundaries—ideally centered between the two so as "to achieve equal amounts of setup and hold time relative to the clock edge" (*i.e.*, to provide the cleanest, most reliable, eye opening reading). Notably, the middle waveform image presented above displays the moment where ALERT_n has begun returning a HIGH value to the memory controller but that HIGH value is not maintained long enough (*i.e.*, three alternating clock cycles) so as to mean the end boundary of the eye opening has been located.

In this way, it is clear that the HIGH or LOW values for ALERT_n, generated by the memory module and transmitted back to the memory controller, do not represent anything more than an indication of whether or not *all* input signals were sampled as 0. The signal is, as the 1023 ID determined (1023 ID at 95-96), a type of feedback signal that reflects the content of the signals it received. It does not reflect the state (*i.e.*, "status") of Clock-to-CA training.

The undersigned acknowledges, however, that Netlist's theory of infringement is not that ALERT_n indicates a status of the entire Clock-to-CA training process. Rather, that theory specifically alleges the claimed "training sequence" is just one, as characterized by Netlist, "eye opening operation." (CIB at 84.) Further, Netlist identifies two specific "statuses" indicated by ALERT_n, where its LOW value (*i.e.* 0) would indicate a "status" of synchronization between the memory controller and module controller, and its HIGH value (*i.e.*, 1) indicates a "status" of non-synchronization. (*Id.*) To be clear, Netlist contends:

> Focusing on the behavior of just one "eye opening" operation (the accused training sequence), the memory controller first sends, over the course of two clock cycles, a set of ones, then a set of zeros, over the enabled Dn inputs to the RCD. CX-0417, at CX-0417.00054-00055; CX-2004C (Mangione-Smith) at Q/A 327-328. With each set of signals the RCD also receives a clock signal. *Id.* The RCD then samples the enabled Dn inputs every other clock cycle according to the clock signal received from the memory controller. CX-0417, at CX-0417.00054-00055; CX-2004C (Mangione-Smith) at Q/A 329, 344. The RCD then logically "ORs" the sampled signals, and generates a single-bit output of zero or a one. CX-2004C (Mangione-Smith) at Q/A 330, 344. The single bit result of the logical OR operation is sent to the memory controller via the open drain output ALERT_n. CX-2004C (Mangione-Smith) at Q/A 288, 330-331, 345. This process is visually depicted in CDX-2004C.052, and is called a single "eye opening operation." This is the claimed training sequence. CX-2004C (Mangione-Smith) at Q/A 332, 344.
>
> . . . .
>
> The resultant value of ALERT_n after a single "eye opening" operation (the claimed training sequence) indicates to the memory controller whether (1) the memory module was able to successfully sample or read all of the enabled Dn inputs as zero (*i.e.*, ALERT_n = low or 0), or (2) the memory module failed to correctly sample or read all of the enabled Dn inputs as zero (*i.e.*, ALERT_n = high or 1). CX-0417.00054-00055; CX-2004C (Mangione-Smith) at Q/A 331, 333, 344. *Successful sampling (Alert_n = 0) is an indication of the memory module and memory controller being "synchronized."* CX-2004C (Mangione-Smith) at Q/A 331, 333, 344. *On the other hand, unsuccessful sampling (Alert_n = 1) indicates that the memory module and memory controller are "unsynchronized." Id.* Thus, the module controller of the Accused Products (the RCD)

> generates (via a logical OR operation of multiple sampled Dn signals) a notification signal (the ALERT_n signal) indicating a status (success or failure) of the one or more one or more training sequences (one or more eye opening operations) to the memory controller. This claim element is infringed.

(CIB at 84-85 (emphasis added).)

The record does not support Netlist's contention. If ALERT_n = 0 is "an indication of the memory module and memory controller being 'synchronized,'" then upon receiving a LOW ALERT_n value, Clock-to-CA training would cease and the memory module could switch to normal operating mode. The training does not cease, however. As described in the JEDEC specification, after receiving a LOW ALERT_n value, the memory controller continues to pull or shift the phase of either the Dn signals or the clock signal for some amount of time until ALERT_n maintains a HIGH value for "three cycles after the last command." (CX-0417 at -68334.) Necessarily, at points during this transition the ALERT_n signal is continuing to return LOW values to the memory controller; and even then, synchronization between the memory module and memory controller is only achieved after the full Clock-to-CA process is performed. Then, after that, the memory controller pulls or shifts the clock signal (or Dn signal) a final time so as to place the clock cycle edge (the moment Dn samples are taken) between the two eye opening boundaries—a technique used to maximize the reliability of the memory module's readings of incoming data signals. It is necessarily true that ALERT_n returns LOW values during this shift as well. After the clock edge is so placed, this would be the moment the memory module and memory controller would be considered synchronized. Thus, the evidence does not support Netlist's claim that ALERT_n = 0 indicates a "status" of synchronization between memory module and memory controller.

Further, even if ALERT_n indicated synchronization between those two components, that synchronization is not so much a "status" of the "training sequence" as opposed to the status which

the training is invoked to achieve. (*See* CX-0417 at -68334 ("The DDR4RCD01 supports several training modes . . . in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal . . . .").)

Additionally, the undersigned finds Netlist's decision to include ALERT_n as both part of its defined "training sequence" (*see* CIB 84 ("[t]he single bit result of the logical OR operation is sent to the memory controller via the open drain output ALERT_n. . . . This process . . . is called a single 'eye opening operation.'")) and also as the "notification signal" meant to indicate a "status" of that training sequence (*id.* at 84-85 ("Successful sampling (Alert_n = 0) is an indication of the memory module and memory controller being 'synchronized.'")) to be generally inconsistent with the spirit of the invention of the '623 patent which treats these signals as separate. For example, the principle aim of the '623 patent is fairly summarized as:

> Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory sub system controller.

('623 patent at 4:48-56; *see* '623 patent at 7:41-47 ("notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences . . . .").) Without reading this feature into the claims, it is nonetheless difficult to see how a notification signal could signal completion after training has ended if it was itself part of that training as ALERT_n is. As to the actual claim language at issue, "the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode" ('623 patent at cl. 1), this too suggests a division between the notification signal and the

signals which actually achieve that initialization or training. Indeed, there is no embodiment in the '623 patent where a signal that is part of the training or initialization sequence also serves to indicate a status of that sequence. (*See generally id.*)

Accordingly, the undersigned finds Netlist has not shown the Accused Products include this limitation of independent claim 1.

3. Dependent claims 2-5 and 7-11

With respect to dependent claims 2-5 and 7-11, Netlist contends that there is no dispute over the infringement of these claims by the Accused Products, apart from their dependence on independent claim 1. (CIB at 92.) Netlist cites to the written testimony of Dr. Mangione-Smith to fulfill its obligation in establishing the Accused Products infringe these claims. (CIB at 92 (citing CX-2004C at Q/A 357-421, 705-765, 790-847, 849-855, 880-926).)

It appears Respondents indeed do not contest infringement of claims 2, 3, 5, and 7-11 apart from their dependence on claim 1, but do contest infringement of claim 4 on independent grounds. (RIB at 75-76; RRB at 53.) Claim 4 recites, "[t]he memory module of claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module." ('623 patent at cl. 4.) Specifically, Respondents argue the CA Bus training mode within the Accused Products is properly characterized as a training mode of the system controller, not the memory module, in light of the memory controller "adjust[ing] the memory controller's clock phase to the memory controller's Dn input timing to adjust timing on the memory controller's command and address signals on the memory controller's bus." (*Id.* at 75 (citing CX-0417 at 44; RX-2148 at 44; CX-2220 at 44; RX-0320 at 44).) Thus, according to Respondents, "nothing in the memory module is trained, and no internal clocks to the memory module are modified as a result of CA Bus training." (*Id.* (citing *inter alia* RX-3870C at Q/A 237-

238); *see id.* at 76 (citing Order 17 at 132).) The Staff appears to agree with this assessment of claim 4. (SIB at 94.)

In its reply brief, Netlist characterizes Respondents' position as "not credible, at least because their own expert consistently testified that the JEDEC RCD Specification only detailed the operation of the RCD component and not the memory controller." (CRB at 64-65 (citing RX-3870C at Q/A 110).) Netlist adds, "[t]he '623 patent does not require the 'training mode' to train a particular component, it merely requires that the memory module is in a training mode." (*Id.* at 65 (citing CX-2004C at Q/A 977; '623 patent at cl. 1; CX-2060C at *137-139).) Put another way, Netlist states, "training occurs in Clock-to-CA Training Mode, a training mode into which the memory module is placed. Claim 4 is infringed." (*Id.*)

In view of the testimony of Dr. Mangione-Smith that the Accused Products infringe claims 2, 3, 5, and 7-11, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products do not infringe claims 2, 3, 5 and 7-11 of the '623 patent based on their dependence on claim 1, but otherwise the limitations of these dependent claims are met in the Accused Products. (*See* CX-2004C at Q/A 357-375, 383-421, 705-765, 790-847, 849-855, 880-926.)[6]

As to dependent claim 4, the undersigned finds the Accused Products would infringe this claim as well if not for its dependence on claim 1. The JEDEC specification discussed above in connection with claim 1 shows clearly that the Clock-to-CA training process involves both the memory controller and the module controller on the memory module. (CX-0417 at -68334-68335.) Without the input of ALERT_n from the module controller, Clock-to-CA training could not be accomplished. The

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[6] The undersigned notes that the numbering of Q357-360 is used twice in CX-2004C. The noted citation refers to the second usage of Q357-360.

specification also outlines, as discussed above, how the memory module enters into a distinct training mode from the loading of its RC0C register with x001 bits. (CX-0417 at -68347, Table 22, -68352, Table 35.) Thus, the memory module does enter into a second mode, which is one of training, and the claim is met.

E. Domestic Industry – Technical Prong

Netlist asserts that its Domestic Industry Products practice claims 1-5 and 7-11 of the '623 patent. (CIB at 5, 93 (citing CX-2004C at Q/A 482-658).) Netlist explains "[t]he relevant analysis is substantially the same as the infringement analysis: the Netlist HybriDIMM is JEDEC compliant" and "[n]either Respondents nor Staff advance any theory regarding technical domestic industry outside of their non-infringement theories." (CIB at 93 (citing CX-2366C at *107; RX-3870C at Q/A 267; RPB at 374-376; SPB at 181).) Thus, Netlist asserts that the practice of claims 1-5 and 7-11 of the '623 patent by the Domestic Industry Products rises and falls with infringement of the same claims by the Accused Products. Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 76; RRB at 53; SIB at 95; SRB at 22-26.)

Accordingly, and given the above determinations on infringement, the undersigned finds the Domestic Industry Products do not practice claims 1-5 and 7-11 of the '623 patent.

F. Validity

As reflected in Respondents' briefing, the validity of the asserted claims of the '623 patent is no longer at issue in this investigation based on Order No. 51. (RIB at 76; RRB at 54; *see* SIB at 95.)

V. U.S. PATENT NO. 9,606,907

A. Overview

Netlist alleges infringement of claims 1-8, 10, 12, 14, and 15 of the '907 patent. Claims 2-8, 10, 12, 14, and 15 depend from independent claim 1. The asserted claims provide as follows:

> 1. [limitation 1a] A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
>
> [limitation 1b] a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
>
> [limitation 1c] a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
>
> [limitation 1d] M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,
>
> [limitation 1e] the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines,
>
> [limitation 1f] wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as

memory device load associated with the respective one or more of the second memory devices from the memory controller; and

[limitation 1g] a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines,

[limitation 1h] wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

2. The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.

3. The memory module of claim 1, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the M sets of n data lines to the memory controller.

4. The memory module of claim 3, wherein the first module control signals include chip select signals, wherein the first memory deviees and the second memory devices receive different chip select signals from the module control circuit.

5. The memory module of claim 1, wherein the each respective buffer circuit is configured to present a load to the respective one or more of the first memory devices that is the same as a load the memory controller would present.

6. The memory module of claim 1, wherein the each respective buffer circuit has a first data width of n bits, and wherein each of the

plurality of memory devices has a second data width different from the first data width.

7. The memory module of claim 1, wherein the second module control signals indicate a direction of data flow through the buffer circuits.

8. The memory module of claim 1, wherein the module control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter.

. . . .

10. The memory module of claim 1, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.

. . . .

12. The memory module of claim 1, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.

. . . .

14. The memory module of claim 1, wherein the first memory read or write command is a memory write command, and wherein the each respective buffer circuit includes tristate buffers controlled by the logic to transmit the respective n-bit section of the each N-bit wide data signal associated with the memory write command to the respective one or more of the first memory devices.

15. The memory module of claim 1, wherein the M buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide.

('907 patent at cls. 1-8, 10, 12, 14, 15.)

B. Level of Ordinary Skill in the Art

As part of the *Markman* process in this investigation, a prior presiding ALJ determined the level of ordinary skill in the art at the time of invention for the '907 patent is "a person having an

electrical or computer engineering background, and specifically, a Bachelor's degree in electrical engineering, computer engineering, or in a related filed and at least one—preferably two—years of work experience relating to memory systems." (Order No. 17 at 9.) The undersigned has considered the issues relevant to this initial determination in accordance with this definition. The parties each allege they have done the same in their analyses of the issues. (*See* CIB at 23; RIB at 15; SIB at 52.)

C. Claim Construction

Order No. 17 construed the following claim terms relevant to the issues in this initial determination:

Term	Construction
"output or receive ... data" / "do not output or receive any data" ('907 patent at cls. 1, 16, 43, 58)	means "transmit or acquire / do not transmit or acquire" and does not require a "fork in the road"
"[M buffer circuits / each respective buffer circuit] being [operatively] coupled to . . . [a] respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines" ('907 patent at cls. 1, 16)	means the first and second memory devices are both connected to the buffer circuit through the same set of *n* (as a number of) module data lines
"the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines" ('907 patent at cl. 1)	does not mean "*selectively* allowing communication" or a "fork in the road"

"produc[e/ing]" ('907 patent at cls. 1, 16, 43, 58)	means "create, *i.e.*, bring into existence"
"wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more [of the first memory devices / memory devices in the subset of the memory devices] [as well as / and] memory device load associated with the [respective] one or more of the [second / other] memory devices from the memory controller" ('907 patent at cls. 1, 16, 43, 58)	as in claims 1 and 16, means "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the respective one or more of the second memory devices from the memory controller" as in claim 43, means "wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices from the memory controller and to isolate memory device load associated with the one or more of the other memory devices from the memory controller" as in claim 58, means "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the one or more of the second memory devices from the memory controller"

(Order No. 17 at 135-136.)

Netlist and Respondents do not identify any discrete claim construction issues beyond those resolved as part of the *Markman* process with Order No. 17. (*See* CIB at 23-25; CRB at 5-6; RIB at 7-15; RRB at 1-4.) The Staff, on the other hand, raises several preliminary claim construction considerations, including: (1) the proper interpretation of Order No. 17's construction of "receive / do not receive"; (2) a perceived "late claim construction argument" from Netlist regarding the same limitation; and (3) a non-infringement argument from Respondents on a PCB

claim limitation. (*See* SMB at 26-36.) The undersigned considers these issues identified by the Staff within the infringement discussion below.

D. Infringement

1. Claim Preclusion

Apart from the merits of Netlist's claim of infringement under the '907 patent, Respondents contend the doctrine of claim preclusion bars the claim altogether. (*See* RIB at 51.) Respondents identify the doctrine as "bar[ring] a party from asserting a cause of action following a 'final judgment on the merits in a prior suit' involving 'the same parties or their privies' and the 'same cause of action'" (*id.* (citing *SimpleAir, Inc. v. Google LLC*, 884 F.3d 1160, 1165 (Fed. Cir. 2018))) and frame the only dispute as whether there is the "same cause of action" here as in the 1023 Investigation (*id.*).

As to whether this investigation consists of the same cause of action, Respondents assert that the "claim language does not have to be identical in order for claim preclusion to apply" but only "'patentably indistinct.'" (*Id.* (citing *SimpleAir*, 884 F.3d at 1167).) Respondents view the obviousness-type double patenting rejection based on the '185 patent, and issued against the '907 patent during prosecution, as a "strong clue" that claim preclusion applies (*id.* at 51-52 (citing *SimpleAir*, 884 F.3d at 1168)), in addition to their expert, Dr. Subramanian's, opinion that the '907 patent claims are obvious over the '185 patent (*see id.* at 52-53 (citations omitted)). Respondents do acknowledge, however, that "the 907 claims are lengthier than the 185 claims" but argue that does not make them patentably distinct because the additional elements only recite well known elements from the prior art. (*Id.* at 53-54 (citations omitted).) Respondents add a contention that Netlist could have asserted the '907 patent in the 1023 Investigation, as a factor supporting the fairness of barring its assertion now. (*Id.* at 54 (citing *SimpleAir*, 884 F.3d at 1169).)

In their reply brief, Respondents accuse Netlist and the Staff of dismissing claim preclusion without addressing *SimpleAir* which, according to Respondents, "created a new test for claim preclusion." (RRB at 36.)

In its opposition, Netlist highlights what it views as a "stark difference in the patent claims here—straight line, not fork in the road" as constituting different transactional facts so as to prevent the application of claim preclusion. (CIB at 78 (citing 1023 ID at 112-125; Order No. 17).) In its reply brief, Netlist argues more specifically:

> Claim preclusion cannot apply here for several reasons. First, Respondents have not cured the deficiencies identified in the ALJ's order denying their motion for summary determination on the basis of claim preclusion. Second, after-acquired causes of action cannot be claim precluded, and the '907 patent did not exist before the 1023 Investigation. Third, cases cannot be precluded if they are based on different transactional facts—and the difference in the patent claims here, conclusively resolved by ALJ Pender's claim construction order, create different transactional facts gutting the defense.

(CRB at 53.) With respect to the timing between the 1023 Investigation and the '907 patent, Netlist explains "[t]he '907 patent issued on March 28, 2017—just days before the close of expert discovery in the 1023 Investigation, and less than a month before pre hearing briefs were due." (*Id.* at 53-54.) Netlist argues it would therefore not have been "feasible" to add it to that prior investigation. (*Id.* at 53.) Finally, Netlist argues the claims of the two patents are materially different and Respondents' attempt to conflate the two based on their specifications is in error. (*Id.* at 54.) The Staff agrees with Netlist, adding that Order No. 17 settled the question of whether the claims of the '907 patent and earlier '185 patent are patentably indistinct—and concluded they were not. (SIB at 82 (citing Order No. 17 at 25).)

Here, the undersigned finds Respondents have not shown the asserted claims of the '907 patent are patentably indistinct from the '185 patent claims addressed in the 1023 Investigation. Indeed, Respondents fail to identify and compare the actual language of the two groups of claims

to show their scopes are indistinct, opting instead to emphasize how obvious or broad the '907 patent claims are in light of the '185 patent. (*See* RIB at 51-54; RRB at 36-37 ("[e]ven if a later claim has a 'stark difference' compared to the earlier claim, the later claim can still be obvious in light of the earlier claim. . . . and thus claim preclusion applies.").) Even though the Federal Circuit has instructed that "a terminal disclaimer is a strong clue that a patent examiner and, by concession, the applicant, thought the claims in the continuation lacked a patentable distinction over the parent," *SimpleAir*, 884 F.3d at 1168, the court immediately emphasized that actual claim language must be compared:

> But as our precedent indicates, that strong clue does not give rise to a presumption that a patent subject to a terminal disclaimer is patentably indistinct from its parent patents. It follows that a court may not presume that assertions of a parent patent and a terminally-disclaimed continuation patent against the same product constitute the same cause of action. Rather, the claim preclusion analysis requires comparing the patents' claims along with other relevant transactional facts.

id.;

> Thus, whether the '838 and '048 continuation patents present the same cause of action as previously litigated depends on the scope of their claims, not on their dates of issuance.

id. at 1169.

If that language is considered, at least two differences in scope are revealed. For example, and as extensively explored in Order No. 17, independent claim 1 of the '907 patent completely fails to require selective electrical isolation between memory devices which was a critical limitation of the '185 patent claims for the 1023 Investigation. (Order No. 17 at 32-33, 37, 64-65.) Claim 1 of the '907 patent also requires first module control signals communicated from a module control circuit to memory devices which cause those memory devices to, for example, "receive" or "not receive" data/data signals; and dependent claim 2 requires the number of those

control signals to increase as compared to what had been received by that module control circuit. (*See* '907 patent at cls. 1, 2.) There is no corresponding limitation recited in the '185 patent claims. (*See* '185 patent at cls. 1-9; *but see* '185 patent at cl. 13 (only reciting "transmitting the first set of module control signals to the plurality of sets of memory devices").) It is therefore impossible to conclude the scopes of these sets of asserted claims are indistinct.

Accordingly, Respondents have not shown claim preclusion should apply to bar Netlist's infringement claims under the '907 patent.

2. Independent Claim 1

As discussed further below, the undersigned finds that the Accused Products infringe claim 1 of the '907 patent.

a) Undisputed Limitations

To facilitate the infringement discussion, Netlist has assigned identifiers to each limitation of independent claim 1 of the '907 patent. (*See* CIB at xx-xxi.) With reference to these identifiers, Netlist contends that there is no dispute over the infringement of limitations 1a and 1d (nor 1e or 1f, as explained in footnote below) by the Accused Products. (CIB at 26, 49.)[7] Netlist cites to the written testimony of its expert, Dr. Levitt, to fulfill its obligation in establishing the Accused Products include these limitations. (CIB at 26 (citing CX-2003C at Q/A 307-346), 49 (citing CX-2003C at Q/A 432-459).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 16-29; RRB at 5-21; SIB at 52; SRB at 6-16.)

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[7] The undersigned notes that, at this point, Netlist's brief stops following the claim limitation identifier scheme it presented in the brief's preface (*compare* CIB at xx *with* CIB at 49), and switches to the differing scheme used in Dr. Levitt's witness statement (*compare* CIB at 49 *with* CX-2003C at Q432). Nevertheless, the undersigned detects no dispute over claim limitations 1e and 1f from Respondents or Staff.

In view of the testimony of Dr. Levitt that the Accused Products include these limitations, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these limitations of independent claim 1. (*See* CX-2003C at Q/A 307-346, 432-459.)

Infringement of limitation 1b is disputed in-part. This limitation reads:

> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

('907 patent at cl. 1.) Within this limitation, Netlist identifies only "produce first module control signals and second module control signals in response to the set of input address and control signals" as in dispute between the parties. (*See* CIB at 26.) Accordingly, this portion is discussed further below. With respect to the remaining portions, Netlist cites to the written testimony of Dr. Levitt to fulfill its obligation in establishing they are present in the Accused Products. (CIB at 26 (citing CX-2003C at Q/A 347-374).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 16-29; RRB at 5-21; SIB at 52; SRB at 6-16.)

In view of the testimony of Dr. Levitt that the Accused Products include these portions, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these features of independent claim 1. (*See* CX-2003C at Q/A 347-374.)

Infringement of limitation 1c is disputed in-part. This limitation reads:

> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

('907 patent at cl. 1.) Within this limitation, Netlist identifies only "second memory devices do not receive any data" as in dispute between the parties. (*See* CIB at 30.) Accordingly, this portion is discussed further below. With respect to the remaining portions, Netlist cites to the written testimony of Dr. Levitt to fulfill its obligation in establishing they are present in the Accused Products. (CIB at 30 (citing CX-2003C at Q/A 375-431).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 16-29, RRB at 5-21, SIB at 52; SRB at 6-16.)

In view of the testimony of Dr. Levitt that the Accused Products include these portions, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these features of independent claim 1. (*See* CX-2003C at Q/A 375-431.)

With respect to limitations 1g and 1h Netlist apparently discusses both in a combined section under a heading identified as limitation 1e. (*Compare* CIB at xx *with* CIB at 49-53.) As discussed above in footnote, this appears to be the result of a switch in claim limitation identifiers between Netlist's brief and its Dr. Levitt's witness statement. Nevertheless, of this grouping, Netlist identifies only a portion of limitation 1h as in dispute (CIB at 49-50 (identifying "wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices")), which appears as follows:

> wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and *wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices*,

('907 patent at cl. 1 (emphasis added).) Accordingly, this disputed portion is discussed further below. With respect to the remaining portions of limitations 1g and 1h, Netlist cites to the written

testimony of Dr. Levitt to fulfill its obligation in establishing they are present in the Accused Products. (CIB at 49-50 (citing CX-2003C at Q/A 460-483).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 16-29, RRB at 5-21, SIB at 52; SRB at 6-16.)

In view of the testimony of Dr. Levitt that the Accused Products include these portions, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the Accused Products include these features and limitations of independent claim 1. (*See* CX-2003C at Q/A 460-483.)

b) Disputed Limitations

As noted above, there is a dispute as to whether the Accused Products meet various portions of limitations 1b, 1c, and combined 1e-1h of independent claim 1 of the '907 patent. As discussed below in more detail, the undersigned finds that the Accused Products do include these limitations.

> (1) "produce first module control signals and second module control signals in response to the first set of input address and control signals"

For this limitation, Netlist contends "the Accused LRDIMM Products include a JEDEC-compliant RCD component that is configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines." (CIB at 26 (citing CX-2003C at Q/A 349, 350, 352).) Netlist further contends the claimed "first module control signals" include, as an example, "QA and QB versions of signals CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, and C0-C2." (*Id.* at 27 (citing, *inter alia*, CX-2003C at Q/A 358; CX-0417 at *63, 12-14, 48).) Netlist argues this occurs during an "Encoded QuadCS Mode" where two chip select signals are received by the RCD, which operates on them to output four chip select signals. (*Id.* (citing CX-2003C at Q/A 360-361; CX-0417 at

*63).) Netlist argues this also occurs in an "output inversion" operation, where address signals received by the RCD are forwarded on to an "A-side" of the memory module, but also inverted before sending on to the "B-side" of the module. (*See id.* (citing CX-2003C at Q/A 363; CX-0417 at *48).) Netlist states "[t]his too demonstrates that the RCD 'produces first module control signals.'" (*Id.*) As to the claimed "second module control signals," Netlist argues these are met by "post-register" signals BCOM, BODT, BCKE, and BCK created by the RCD circuit on the memory module which are then sent to and control how the DBs (data buffers) operate. (*See id.* at 28 (citing, *inter alia*, CX-2003C at Q/A 366-370; CX-0417 at *23, 24, 26, 28, 63).) The Staff appears to agree with Netlist on this limitation. (*See* SIB at 53-56.)

Netlist disputes what it views Respondents' opposition to be, namely that "this claim element requires using both address and other control signals as inputs to produce all new control signals." (*Id.* at 28 (citing RX-3869C at Q/A 116-137).) Netlist argues this opposition is in error based on findings on the meaning of "produce" in Order No. 17 (*id.* at 29) and the claim's plain language use of "set" (*id.* at 29-30) which simply means one set of address and control signals is turned into two sets of output control signals (*id.* at 29-30; *see* CRB at 11-12).

Respondents indeed describe their opposition to this limitation as "[t]he accused products do not use *both* address *and* control signals to produce a new output signal—that fact is undisputed." (RIB at 23-24 (emphasis in original).) Respondents acknowledge Order No. 17 construed "produce" but claims it did not construe "in response to the set of input address **and** control signals." (*Id.* at 24 (emphasis in original).) Respondents view Netlist's interpretation as "rendering the word 'and' [emphasized by Respondents above] superfluous." (*Id.*; *see* RRB at 17-18.) Respondents state "[a]ny construction that would cover module control signals produced in response to either input address signals alone or control signals alone would improperly render

limitations of the claim meaningless." (RIB at 24 (citing *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010)).) Respondents claim the '907 patent specification only describes the use of both address and control signals to produce "the module control signals." (*See id.* at 24-25 (citing RX-3869C at Q/A 116; '907 patent at 10:39-44, 17:57-18:16, 18:28-59; RX-0163 at Figs. 1A, Table 1); RRB at 18-19.) Respondents further claim the prosecution history of a patent, similar to another incorporated by reference into the '907 patent specification, confirms "set of" cannot mean address or control signals but must mean address *and* control signals. (*See* RIB at 25 (citations omitted).)

Under this interpretation, Respondents argue Netlist's identified "second module control signals" (BCOM, BODT, BCKE, and BCK) are unrelated and therefore not produced in response to any address signals. (*See id.* at 26 (citing RX-3869C at Q/A 121-126).) Similarly, for Netlist's identified "first module control signals," Respondents argue a first group are not produced in response to address signals (*id.* at 27 (citing RX-3869C at Q/A 128); RRB at 19) while the remaining signals are not produced in response to any control signals (RIB at 27 (citing RX-3869C at Q/A 128)). Respondents summarize "[i]n both cases, the output is produced in response to *either* control signals *or* address signals, but not both as required by the claim language." (*Id.* at 37-38 (citing RX-3869C at Q/A 127-137) (emphasis in original).) Respondents also note that Netlist's reliance on "Encoded QuadCS Mode" for the "first module control signals" can only apply to those accused products with four ranks of memory, and not those with two or eight (RIB at 27 n.7 (citing RX-3869C at Q/A 130; CX-2003C at Q/A 15; RRB at 19) and "output inversion" does not actually constitute "produc[ing]" signals (RRB at 19 (citing RX-3869C at Q/A 131-132)).

Here, Respondents' primary non-infringement position is based on reading "to produce first module control signals and second module control signals in response to the set of input

address and control signals" as requiring the "first module control signals" and "second module control signals" each be produced in response to each type of input signal (address and control). The undersigned finds the limitation should not be read so narrowly. The claim language reads:

> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

('907 patent at cl. 1.) A plain reading of this language conveys that an unspecified number of signals are received by a module control circuit, some of which would be characterized as "address" signals and some as "control" signals, and the module control circuit uses those signals to produce a further unspecified number of "first module control signals" and similarly unspecified "second module control signals." The limitation's use of "set" consolidates the input address and control signals such that a response to any one of those signals is a response to the set. This is strongly supported by the '907 patent's disclosure that, according to its own usage, there is no real difference between a "control" signal and an "address" signal:

> Furthermore, especially when registered DIMMs (RDIMMs) are used, the increase in the number of the memory devices translates to an increase in the distributed RC load on the data paths, but not on the control paths (e.g., address paths), thereby introducing uneven signal propagation delay between the data signal paths and control signal paths. *As used herein, the terms "control lines" and "control paths" include address lines or paths and command lines or paths, and the term "control signals" includes address signals and command signals.*

('907 patent at 4:29-38 (emphasis added));

> The control circuit **430, 430'** of certain embodiments is configurable to be operatively coupled to control lines **440, 440'** to receive control signals (e.g., bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller **420, 420'**.

(*id.* at 10:24-29);

> The latency may be used by the memory module to control operation of the data transmission circuits **416**. During the latency, address and control signals pass from the memory controller **420** to the control circuit **430** which produces controls sent to the control logic circuitry **502** (e.g., via lines **432**) which then controls operation of the components of the data transmission circuits **416**.

(*id.* at 15:57-64). Respondents' citations to the '907 patent specification and other sources, discussed below, do not give reason to depart from this plain meaning.

First, Respondents point to intrinsic evidence from the '386 patent (incorporated by reference into the '907 patent) showing how chip-select signals (*i.e.*, "first module control signals") are produced in response to both types of input signals (*see* RRB at 18-19 (citing '386 patent at Fig. 1A, Table 1, 7:45-8:14)), with the following demonstrative:

FIG. 1A

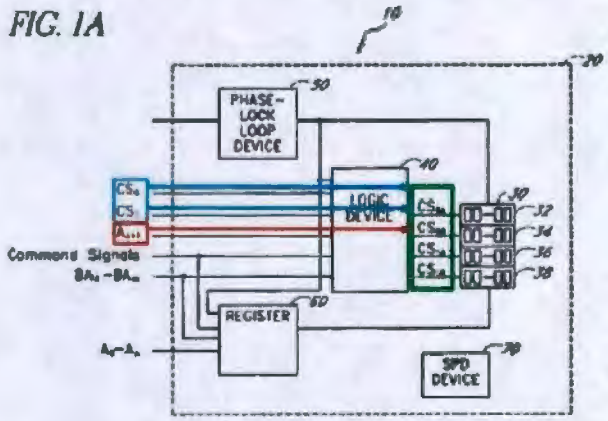

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

(RRB at 18 (showing '386 patent at Fig. 1A, 7:45-8:14) (annotated).) Yet this would appear to be an artificial distinction as the '386 patent also treats address signals as a type of control signal:

> As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element **40** receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element **40** generates a set of

> output control signals which includes address signals and command signals.

('386 patent at 6:63-7:5.)[8] Further, the same figure shows additional "bank address signals (BA_0-BA_m)" supplied to the logic device 40 (*i.e.*, "module control circuit" in the '907 patent claims) which are not used to produce CS_{0A} through CS_{1B} (*i.e.*, "first module control signals" in the '907 patent claims). ('386 patent at Fig. 1, 7:45-8:14.) Thus, this example actually shows less than all types of the "input address and control signals" being used to "produce first module control signals."

Respondents also point to the '907 patent specification and argue it "states that the module control circuit can 'produce additional chip-select signals or output enable signals based on address decoding,' which uses both address and control signals as inputs, as [again] described in the 386 patent incorporated by reference." (RIB at 24-25 (citing ""907 patent at 10:39-44; '386 patent at Fig. 1A, Table 1).) Yet the full '907 patent passage actually states "may produce":

> Additionally, the control circuit **430, 430'** supplies control signals for the data transmission circuits **416, 416'** (e.g., via lines **432, 432'**), as described more fully below. The control signals indicate, for example, the direction of data flow, that is, to or from the memory devices **412, 412'**. The control circuit **430, 430'** *may produce additional* chip-select signals or output enable signals based on address decoding. Examples of circuits which can serve as the control circuit **430, 430'** are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein.

('907 patent at 10:34-44 (emphasis added).) Contrary to Respondents urging, the undersigned views this passage, and its use of "*may produce additional* . . . signals" to imply the existence of an embodiment where chip-select signals (*i.e.*, "first module control signals") and output enable

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[8] Notably, this Figure and Table from the '386 patent also mentions "command signals," yet these too are considered a type of control signal—by both the '386 patent ('386 patent at 6:63-7:5) and '907 patent ('907 patent at 4:36-37 ("the term 'control signals' includes address signals and command signals.")).

signals (*i.e.*, "second module control signals") are not based on address decoding—otherwise the phrase "may produce additional" would not have been used.

In another example, Respondents argue "[t]he 907 patent repeatedly explains 'the control circuit 430 evaluates the address and control signals' to produce the second module control signals for the data buffer circuits during a read or write operation." (RIB at 25 (citing '907 patent at 17:57-18:16, 18:28-59).) The undersigned again does not agree. While each cited passage does include Respondents' quotation, they do not reflect Respondents' subsequent paraphrasing of "to produce . . . ." Instead, they simply mention the module controller 430 evaluates those signals "to determine that data is to be [written to/read from] memory devices . . . in the [first/second] group":

> The control circuit **430** evaluates the address and control signals **440** to determine that data is to be written to memory devices **412A**, **412C** in the first group.

('907 patent at 17:60-63);

> The control circuit **430** evaluates the address and control signals **440** to determine that data is to be written to memory devices **412**B, **412**D in the second group.

(*id.* at 18:6-9);

> The control circuit **430** evaluates the address and control signals **440** to determine that data is to be read from memory devices **412**A, **412**C in the first group.

(*id.* at 18:31-34);

> The control circuit **430** evaluates the address and control signals **440** to determine that data is to be read from memory devices **412**B, **412**D in the second group.

(*id.* at 18:47-50). There is no mention here on the nature of the signals passed to the data transmission (*i.e.* buffer) circuits as being based on one or both types (to the extent there is a meaningful difference) of input signal.

Finally, Respondents refer to statements made during prosecution of a certain "912 patent"—a patent continuing from the '386 patent but not itself incorporated by or related to the '907 patent—over claims reciting generating a "set" of output signals in response to a "set" of input signals, wherein that set of input signals needed to include at least one chip-select signal and at least one bank address signal. (RIB at 25 (citing JX-2003 at *331-335).) According to Respondents, Netlist argued that the limitation would not be met if bank address signals were not used to generate any of the output control signals (*see id.*) with an implication that these statements somehow mandate their interpretation of the '907 patent claim limitation at issue. Respondents' briefing, however, does not present any law supporting the use of prosecution activity from an unrelated patent to limit claim terms in a challenged patent, even when that unrelated patent happens to be a continuation of a third patent the challenged patent incorporates by reference. (*See* RIB at 25.)

With the proper claim scope in mind, and with respect to "first module control signals," there appears to be no dispute to Netlist's claim that, in at least some Accused Products, the RCD operates in an "Encoded QuadCS Mode" where "the RCD receives two chip select signals at its input on the DCS[1:0] pins, decodes them, and then creates two new signals to output four chip select signals: QACS[3:0]_n and QBCS[3:0]." (CIB at 27 (citing CX-2003C at Q/A 360-361; CX-0417 at *63); *see* RIB at 27; RRB at 19).) There also appears to be no dispute that in a process called "output inversion," the "RCD first receives an address signal, and sends the address, in an unmodified form, to the memory devices on the A-side of a memory module. . . . Then, the RCD inverts the address – meaning the bit values of the address are set to their logical inverse – and sends that signal to memory devices on the B-side of the memory module." (CIB at 27 (citing CX-2003C at Q/A 363); RIB at 27; RRB at 19).) The undersigned finds either of these processes

meets the limitation requiring "first module control signals" produced in response to the "set of input address and control signals." Order No. 17 construed "produce" as "create, *i.e.*, bring into existence." (Order No. 17 at 135.) It appears from this description, not contested by Respondents, that the inverted signal does not exist until the RCD creates it—*i.e.*, the inverted signal is a product of the RCD and thus "produced" by the RCD. To the extent Respondents argue that "Encoded QuadCS Mode" only exists in a subset of the Accused Products (*see* RIB at 27 n.7), there appears to be no such restriction on the "output inversion" process Netlist identifies.

As to the "second module control signals," and with proper claim scope in mind, there appears to be no remaining dispute to Netlist's claim that "the RCD is configured to produce, in response to the set of input address and control signals, a second set of control signals, such as BCOM, BODT, BCKE, and BCK, which are sent from the RCD to the data buffers." (CIB at 28 (citing CX-2003C at Q/A 366-374; CX-0417 at *63); RIB at 26; RRB at 19 (arguing only that none of these signals depend on address signals as inputs).) The undersigned finds this meets the limitation requiring "second module control signals" produced in response to the "set of input address and control signals."

Accordingly, the undersigned finds the Accused Products do include this feature of independent claim 1.

(2) "second memory devices do not receive any data"

At the outset, the undersigned notes that this limitation is subject to extensive briefing by the parties and the dispute involves both the meaning of Order No. 17's construction of "receive" and the nature of the Accused Products' operation.

In its opening brief, and with respect to the meaning of "receive," Netlist contends Order No. 17 has already rejected the idea that a circuit element "receives" a signal when that signal

simply reaches one of the element's inputs. (CIB at 30-31 (citing Order no. 17 at 32).) Rather, Netlist contends "receive" "refers to the first stage of a write operation to a memory devices in the selected rank, *i.e.*, acquiring data." (*Id.* at 31 (citation omitted) (emphasis in original); CRB at 5, 19 (arguing Dr. Subramanian confirmed that the first stage of a write operation necessitates amplifying data and sending it to be latched").) Netlist also contends, however, that "'receiving' data occurs when different memories receive different chip selects and a single rank accepts data during the first stage of a write operation which is evidence by a latch." (CIB at 31 (emphases in original); CRB at 6 ("[T]he only question that needs to be answered when applying the claim terms to the accused products is: do the second memory devices 'latch'?"), 8 (asserting "acquire" means "(1) latch or (2) amplify data and send to a latch"), 18-19 ("Netlist has always maintained that [acquire] requires the demonstration of a 'latch.'").) Netlist represents that Order No. 17 construed "receive" as "acquire" "in agreement with Netlist"; and also that Dr. Subramanian "interprets 'acquire' to mean 'the first stage of a write operation to a memory device in a selected rank.'" (CIB at 32 (citing RX-3869C at Q/A 71-72); CRB at 9 ("And, at the end of the day, the point remains: all parties agree that the 'first stage of a write operation' is what 'acquire' means").) Netlist continues:

> Importantly, Dr. Subramanian testified at the hearing in this case and at the hearing in the 1023 Investigation that the "latch in the DRAM device" is the "first stage" of "what accepts the data." JX-2034C (Subramanian) at 653:8-10; Tr. (Subramanian) at 694:23-695:2. Dr. Subramanian gave this testimony as he was describing the operation of a targeted (*i.e.*, selected) memory device performing a "normal write operation." Tr. (Subramanian) at 693:3-695:2. The only logical inference from this is that the "latch" is the first stage of the write operation—as he testified even in the 1023 Investigation. JX-2034C (Subramanian) at 653:8-10. This makes the infringement analysis straight forward: if a selected memory device "latches" data, it has "acquired" data. In contrast, if a non-selected memory device does not "latch" data, it has not "acquired" data. This is both

> Netlist's infringement theory and exactly how the Accused LRDIMM Products operate.

(CIB at 32.) Netlist re-summarizes, at a self-characterized "memory system level—which is the proper level of skill of a POSITA" (*id.* at 35), the operation of the Accused Products as:

> For example, during a write command, the first memory devices will receive as inputs from the RCD a low value on their respective CS pins. CX-2003C (Levitt) at Q/A 385, 388; CX-0889 at CX-0899.00032. The second memory devices will receive a high value on their respective CS pins, which causes the second memory devices to be de-selected. This precludes the second memory devices from acquiring or writing data as part of the write command. CX-2003C (Levitt) at Q/A 385, 388; CX-0889 at CX-0899.00032. The JEDEC RCD specification expressly states that only one rank at a time is selected to perform a particular memory operation. CX-0417 at CX-0417.00020 in Figure 3, Note 1. CX-2003C (Levitt) at Q/A 383. This is visually depicted in CDX-2003.052. Logic dictates that a memory device that is targeted, selected, or activated to perform a write operation, does, in fact, perform the first stage of a write operation. Conversely, a memory device that is not targeted, selected, or activated to perform a write operation, does not perform the first stage of a write operation. Accordingly, the Accused LRDIMM Products satisfy the "in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command" portion of this claim element.

(*Id.* at 35-36; *see also id.* at 41-44 (describing, in particular, amplification of data signals in selected memory devices)).

Responding to Respondents' opposition, Netlist argues that terminating a data signal is not the same as acquiring data, and, similarly, termination of that signal followed by [redacted] is also not acquiring data. (*Id.* at 33 (referring to RX-3869C at Q/A 56, 72); *see id.* at 45-49 (describing, in particular, ODT functionality as known by a POSITA and not understood to "receive" or "acquire" data); CRB at 8, 14, 16.) With particular respect to Respondents' corresponding argument that the RCVRS

circuity in second memory devices is always active and therefore is acquiring data, Netlist explains:

> The only operation the RCVRS circuitry performs (and the only operation it is capable of performing) in the second memory devices is [redacted]

(CRB at 17.) Netlist further claims "[i]t is undisputed that [redacted] . . . Dr. Subramanian admitted that, in these second memory devices, [redacted] (*Id.* (citing Subramanian, Tr. at 695:3-20; 695:21-696:18; 697:12-22; 697:6-11; 697:23-698:16; 700:19-701:5; 701:6-19).)

Netlist views the Staff as promoting an additional, but equally incorrect, interpretation of "acquire" that requires common acquiring circuitry between selected and unselected memory devices but where that use of that circuitry is precluded in unselected memory devices. (*See* CIB at 33 (citing SPB at 99-100).) Netlist argues the practical operation of the Accused Products does not support Staff's application of its interpretation either, because:

[redacted]

(*Id.* at 34 (emphases in original); *see generally* CRB at 22-28 ("The evidence unequivocally demonstrates, and all experts agree, [redacted].) With

respect to the Staff's assertion that no connection has been made between the "first module control signals" and "receive/do not receive limitation," Netlist disputes this and cites Dr. Levitt's testimony. (CRB at 24-25 (citing, *inter alia*, CX-2003C at Q/A 360-363, 349, 382, 385, 388, 409-411).)

Turning back to Respondents' theory, Netlist argues Respondents have improperly ignored the claims' "express distinction" between the terms "data" and "data signal." (CIB at 34 (citing *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1333 n.3 (Fed. Cir. 2006)); *see* CRB at 6, 19.) Netlist views Dr. Subramanian as acknowledging this when he described how "a 'data signal' is what 'carries' 'data,' and that a 'data signal' is just a representation of 'data.'" (CIB at 34 (citing [RX]-3869C at Q/A 96; Subramanian, Tr. at 677:2-18); CRB at 6 ("Thus, legally and factually the claims [sic] terms have different meanings.").) Netlist then claims a certain "train analogy" employed by Dr. Subramanian during the 1023 Investigation to explain the Accused Products' operation actually supports infringement in this investigation. (*See generally id.* at 36-39; CRB at 14-15.) Netlist also argues transistor-level analysis of the memory devices to determine if they "receive" or do not "receive" data under the claim is unnecessary because the definition of a POSITA for the '907 patent is concerned only with "how JEDEC-compliant memory devices operate; not their internal design and construction." (CIB at 39-40 (citing Levitt, Tr. at 444:18-446:24, 450:2-22, 451:13-453:3, 464:11-25, 465:10-466:18).) Netlist observes "[t]ellingly, Respondents and Staff have failed to perform the same level of analysis when presenting invalidity contentions." (*Id.* at 40; *see* CRB at 26-28.)

In opposition, Respondents essentially argue that despite the Accused Products use of JEDEC-standard chip-select signals, all of the memory devices in the memory module "*always*"

"receive" or "acquire" data under the meaning of those terms in the '907 patent during a write command. (*See* RIB at 17-18 (emphasis in original).) Respondents continue, however, to state:

> There is an important technical reason why both ranks in the accused products acquire the same data even though one rank will ignore the data while the other rank writes the data to memory. *See* RX-3869C at Q/A 38. This functionality prevents the data from "reflecting" off the second rank back on to the data bus, which would cause interference. *See id.* (discussing use of "on-die termination" (ODT) circuits inside each memory device to prevent reflections of data signals); Levitt, Tr. 388:22–389:8 ("ODT plays an important role."). Thus, in the accused products, the alleged "second" memory devices are not just sitting passively, doing nothing, during a write operation directed to the alleged "first" memory devices. *See* RX-3869C at Q/A 52.

(*Id.* at 18.) Respondents argue the second, non-selected memory devices, "actively acquire and terminate the data being sent on the shared data bus so that it does not reflect back and interfere with the data transmission." (*Id.* at 19 (citing RX-3869C at Q/A 52).) Respondents add:

> In addition, the system memory controller specifically sends control signals (such as CKE) to the "second" memory device so that its "receiver" circuitry (called RCVR) [redacted] This also precludes infringement.

(*Id.*; *see* RRB at 10-11.) In their reply brief, Respondents seek to clarify that they do not claim "terminating" is the same as "acquiring," but that "if the memory device is not the target of the write operation . . . , then after the data is 'acquired' it will be 'terminated' by the ODT circuitry and [redacted] (RRB at 13 (citing RX-3869C at Q/A 55, 70).) Respondents continue, citing Dr. Subramanian, [redacted] . . . The same is true with respect to 'terminating' [redacted] you cannot do either until you have first acquired the data." (*Id.* at 13.)

Respondents also describe what they view as Netlist's changing of its infringement theories throughout the investigation "as [it] kept discovering that each theory does not read on the accused products." (*See* RIB at 19-21 (citing RX-3869C at Q/A 40-48, 93).) Respondents explain how, in the third and final theory, it is Netlist's position that "'data' only exists (and therefore is 'acquired') after the data signal has been 'latched' deep inside the memory device, Levitt, Tr. 409:17-20, which Dr. Levitt further alleges, without evidence, never happens in the second memory devices of the accused products, *see* RX-3869C at Q/A /A 74-76, 92-93." (*Id.* at 20-21.) Respondents contend this theory fails for at least six reasons: (1) Order No. 17 specifically rejected "latch" as the meaning of "receive" (RIB at 21; RRB at 5-7); "data" and "data signal" are, in fact, interchangeable according to the intrinsic evidence, Order No. 17, and various experts' usages of the terms (RIB at 21-22; RRB at 7-10); (3) [redacted] (RIB at 22); (4) no expert analysis of how first memory devices supposedly receive "data signals" in response to "first module control signals" under the claim (RIB at 22-23; RRB at 15); (5) Dr. Levitt generally should be accorded no weight for lack of credibility in light of changing theories (RIB at 23); and (6) that Dr. Levitt's admission that data can be received without latching (RIB at 23; RRB at 5 (citing, *inter alia*, Levitt, Tr. at 395:19-22)).

Relatedly, Respondents claim chip-select signals are an insufficient tool to determine whether memory devices "receive" or "do not receive" because they "merely tell[] a memory device whether to write the data [to] its internal memory array, not whether to 'receive' and 'acquire' the data in the first place." (RRB at 15 (citing RX-3869C at Q/A 86; Subramanian, Tr. at 743:18-744:5).) Respondents also claim Netlist discusses Dr. Subramanian's train analogy from the 1023 Investigation in an incomplete fashion. (*See id.* at 16-17.)

The Staff agrees with Respondents that the limitation is not met. (SIB at 36; SRB at 7.) The Staff argues latching cannot be the meaning of "receive" under Order No. 17 as it is indisputably not the first stage of a write operation; and thus, Netlist's theory depending on latching cannot succeed. (SIB at 37; *see id.* at 38-39 (citing Levitt, Tr. at 447:19-22; CX-2057); *id.* at 39 n.32 (citing Levitt, Tr. at 447:12-18); SRB at 12-14.) Even if latching is used as "receive," the Staff contends the limitation is not met for lack of a connection between latching and the "first module control signals" in which the "receiv[ing]" must be in response to. (SIB at 40; SRB at 9-10.) Specifically, the Staff observes Netlist identifying two different lists of signals for each limitation with an implication that this is problematic. (*See* SIB at 40-41 (citing CX-2003C at Q/A 358, 382); SRB at 10.) The Staff further argues how an [redacted] (SIB at 42.)

Additionally, the Staff argues "the evidence shows that the transmission from the memory controller is [redacted] Accordingly, the evidence does not show that the first memory device 'receives' while the second memory devices 'do not receive' as construed." (SIB at 36; SRB at 15.) Specifically, the Staff argues "the evidence shows that in both the first and second memory devices, [redacted] (*Id.* at 39 (citing CX-2003C at Q/A 409; CPB at 116-117), 58 (citing RX-3869C at Q/A 72), 58 n. 45 (citing RX-3869C at Q/A 68, 69); SRB at 16 (citing Subramanian, Tr. at 697:12-19).)

Overall, the Staff contends a generic showing of performance or non-performance by a memory device is not sufficient to show the limitation is met under Order No. 17. (SIB at 42-44

(citing Order No. 17 at 38, 34, 20); *id.* at 56-57 (citing CX-2003C at Q/A 382, 385); *see generally* SRB at 7-11 (Netlist's conclusory statement that a non-selected memory devices does not perform the first stage of [a] write operation is not supported.").) The Staff also contends Netlist's reliance on JEDEC specifications is inadequate given that these specifications "do not dictate the internal operations/processing of signals by individual memory devices, and merely disclose that a memory device 'latches' data for a write operation." (*Id.* at 44 (citing Levitt, Tr. at 445-449).) The Staff summarizes, "the claim limitation as construed is not satisfied by the mere 'normal and intended use' of memory devices . . . ." (*Id.* at 57.)

Here, the undersigned finds the limitation is met by the Accused Products. As a preliminary matter, the undersigned finds it is not proper to assign different meanings to the terms "data" and "data signal" in the '907 patent claims even though they are technically different words used within the same claim. For context, the limitation reads:

> [T]he first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

('907 patent at cl. 1.) The parties focus on the "do not . . . receive any data" portion of this limitation but the undersigned does not observe any party addressing the "do not output . . . any data" portion. Indeed, it follows, and no party has asserted otherwise, that it is "data signals" which are output by memory devices, and not "data". Contrary to Netlist's suggestion, the undersigned does not read *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d at 1324, 1333 n.3 (Fed. Cir. 2006) ("*Applied Med.*") as requiring different meanings for these terms, as the case which *Applied Med.* draws upon for support clearly states different meanings are only presumed, and then, only in the absence of evidence to the contrary:

> It is certainly established that claims are to be construed to "preserve the patent's internal coherence." *Markman*, 517 U.S. at 390, 116

> S.Ct. 1384. In addition, "[i]n the absence of any evidence to the contrary, we must presume that the use of . . . different terms in the claims connotes different meanings." *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed.Cir.2000). In other words, the use of two terms in a claim requires that they connote different meanings, not that they necessarily refer to two different structures. *Id.* The prosecution history, specification, comparison with other claims in the patent, and other evidence may require that two terms in a claim refer to different structures, *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-19 (Fed.Cir.2005) (en banc), but preserving claim integrity does not.

Applied Med., 448 F.3d at 1333 n.3; *see Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010) (citing *CAE Screenplates*, 224 F.3d at 1317).

Here, the undersigned finds the '907 patent provides evidence to the contrary; specifically, usage of "data" and "data signals" that suggests interchangeability. (*See, e.g.*, '907 patent at cls. 1, 15, 43, 2:59-3:20.) In particular, within claim 1 itself, as excerpted above, is language requiring that during a read operation, a first memory device outputs a "data signal" while a second memory device does not output "data." (*Id.* at cl. 1.) The undersigned does not understand from the record that a memory device is actually capable of outputting "data" in contrast to a "data signal." (*See* CX-2003C at Q/A 70 ("In the second stage of the read operation, the memory chip transmits data from the data I/O by converting the digital data into an analog waveform and driving that data signal representing the data values on to the connected data lines . . ."), 393; CX-0257 at -39747.) Netlist's argument on the importance of when a "data signal" supposedly changes to "data" during a write operation (*see, e.g.*, CIB at 42 (referring to "data" as "digital, binary form" and only existing after the RCVRS block)) necessarily assumes the opposite—that memory devices do output "data" as opposed to "data signals"—which is incorrect. It is therefore reasonable to treat "data" and "data signal" as used in "the first memory devices output or receive each N-bit wide data signal

associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command" the same.

With this understanding, the parties' primary dispute becomes whether memory devices alleged to be the "second memory devices" meet the "do not receive" limitation during a write operation. The record shows that they do.

The parties are effectively in agreement that Order No. 17 construed "receive" as "acquire" and that "acquire" was understood in that order as meaning "the first stage of a write operation." (CIB at 31; RIB at 7, 11; SIB at 37, 41; Order No. 17 at 20.) The parties' experts are in agreement that, during a write operation, the incoming data signal lands on the input pins of all Accused Product memory devices regardless of whether they are selected (*i.e.*, targeted) or not—specifically, the input pin of a RCVRS circuit. (RX-3869C at Q/A 35, 68, 70; *see* CX-2003C at Q/A 388, 405.)

It is at this point the record shows [redacted]" (RX-3869C at

Q/A 70.) Dr. Levitt characterizes this circumstance as [redacted]

(CX-2003C at Q/A 410.)

The undersigned finds that [redacted] Therefore, the second un-selected memory device has not "acquired" or "received" the signal. Rather, as Dr. Subramanian described it in the 1023 Investigation, the incoming data signal is "ignored." (*See, e.g.*, CX-2068C at Q/A 85-90 ("The chip select signal CS1A_n is not activated so the memory chips D18 and D23 in the second rank ignore and do not process the data"), 180; RX-3869C at Q/A 56, 86.) Consideration of the on or off state of the RCVRS amplifier circuit as indicative of whether a memory device received or did not receive a data signal is consistent with the '907 patent's discussion of chip-select signals as selecting or "activat[ing]" memory devices during operation. ('907 patent at 1:51-58 ("During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals.").) The undersigned finds Dr. Subramanian's characterization of the [redacted] and not consistent with the '907 patent.

Setting aside the RCVRS circuit, however, the parties' experts are also in agreement that, during a write operation, the incoming data signal lands not only on the input pin of the RCVRS circuit, but also on the input pin of an on-die termination ("ODT") circuit located in parallel to the RCVRS circuit. (CX-2003C at Q/A 419; RX-3869C at Q/A 53-54.) This parallel relationship is shown in CX-0889:

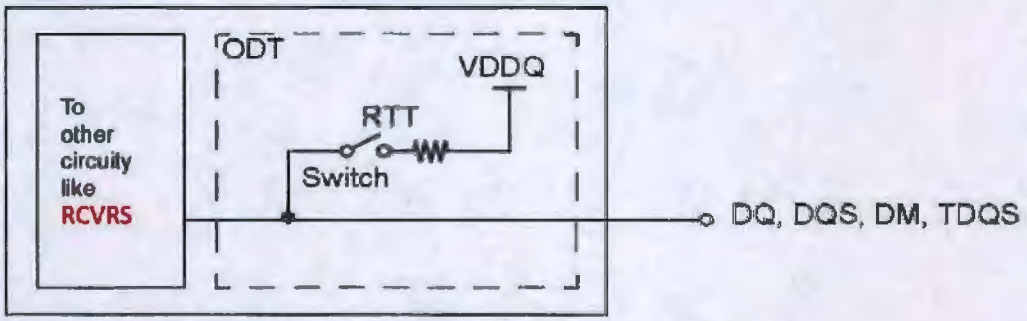


Figure 157 — Functional Representation of ODT

(CX-0889 at -57021 (annotated); *see* CX-0889 at -57022 at Fig. 158.) Netlist describes the ODT as "ensuring that the data signal that has entered the non-selected memory device during a write operation as a result of being made available on the shared data line is terminated. This is to ensure that the data signal does not reflect back onto the shared data line." (CX-2003C at Q/A 420.)

Dr. Subramanian similarly describes the action of the ODT as "inside each memory device to prevent reflections of data signals." (RX-3869C at Q/A 38.) Dr. Subramanian also acknowledges how memory device usage of ODT is disclosed in the '386 patent (RX-0163) incorporated by reference into the '907 patent (RX-3869C at Q/A 38) and ODT was introduced into JEDEC-standardization of memory devices with the DDR2 standard (*id.* at Q/A 53-54). Contrary to Dr. Levitt, however, Dr. Subramanian claims the signal-terminating action of ODT actually constitutes "receiving" or "acquiring" the data signal such that memory devices, regardless of whether they are selected (*i.e.*, "first memory devices") or un-selected (*i.e.*, "second

memory devices"), never stop "receiving" or "acquiring" the data signal in violation of the "do not receive" claim limitation. (*See* RX-3869C at Q/A 52.) To be exact, Dr. Subramanian testified:

> Q. Please summarize how the use of ODT functionality in the JEDEC standards confirms your opinion that the alleged "second memory devices" will acquire the same data sent to the alleged "first memory devices"?
>
> A. The ODT circuit causes the "second" memory devices to "receive" (*i.e.*, acquire) the data as construed by ALJ Pender even if the chip-select signal causes that memory device to ignore the received data and not write it to memory. For example, "receiving" as a result of ODT functionality "is something the memory devices do rather than a result of some other external act." Order No. 17 (RX-2437) at .00032. Indeed, those data signals are terminated on the die of the memory device (hence the name On Die Termination). Dr. Levitt agrees with me in Q/A 420 of CX-2003C that "[t]his is to ensure that the data signal does not reflect back onto the shared data line, which would potentially harm the integrity of the signal intended for the selected memory devices." In other words, if the ODT circuits were disabled (*i.e.*, a Hi-Z state), the data signals would "bounce off" from the ODT circuits (to use ALJ Pender's analogy) and could cause reflections on the data bus. *Id.* at .00042 ("[A] better analogy might be a dart (data) thrown at a dart board (memory device) which will either stick (memory device configured to receive) or bounce off and fall dead (memory device configured to not receive)."). With the proper ODT control, the data is "acquired" as the signal carrying that data is terminated on the die of the alleged "second" memory device. *Id.* (in ALJ Pender's analogy, the dart sticks to the board). That is, the ODT signal from the system memory controller that is sent to the ODT circuitry (as well as the clock enable (CKE) signal that is sent to the CKE circuitry) configures the alleged "second" memory device to acquire the data in the Accused SK hynix LRDIMM Products.

(RX-3869C at Q/A 56.) Dr. Subramanian cites details of ODT functionality by reference to a technical report "written by a student of my colleagues Elad Alon and Vladimir Stojanovich" which states:

> At the high frequencies of operation of DDR4, the transmission lines in the communication channel cannot be treated as lumped components. Their electrical properties and length have an impact on the signal. One of the major concerns is the signal reflection due to impedance mismatch at the source and load (Feng et al. 2013).To

> minimize these reflections and their adverse impact on the signal quality, appropriate termination impedances are required. ODT entails that these impedances be present on the die itself, and not connected externally to the chip. The exact value of these impedances depends on the operating conditions such as supply voltage and temperature and therefore, need to be dynamically varied. To achieve this, ZQ calibration is performed.

(*Id.* at Q/A 59 (citing RX-4052) (emphases removed).) Dr. Subramanian describes this function as "acquiring" the data signal in many places in his testimony. (*See, e.g.*, RX-3869C at Q/A 52, 55, 56, 57, 58, 60, 62, 64, 70, 72, 81, 84, 105, 108, 109, 111, 113).)

The undersigned is not persuaded the termination function provided by ODT constitutes "receiving" or "acquiring" a data signal under the '907 patent. Dr. Subramanian is conclusory on this point, offering no explanation as to how ODT's termination is a form of reception or acquisition or how it resembles, for example, the first stage of a write operation. (*See* RX-3869C at Q/A 81 ("A Skilled Artisan, however, would have understood that one of the memory operations which is relevant to 'receiving' data is receiving the data signal by the On-Die Termination (in short, 'ODT') circuit."); *see also* RX-3869C at Q/A 52, 55, 56, 57, 58, 60, 62, 64, 70, 72, 84, 105, 108, 109, 111, 113); Subramanian, Tr. at 709:6-717:22, 741:12-742:4, 744:24-749:7.) To the contrary, the termination of the data signal by ODT appears equivalent in relevant effect to [redacted] In both cases, the data signal is terminated and its substance (*i.e.*, sequence of 1s and 0s) is lost and/or ignored. The signal is not "received" or "acquired." it is extinguished.

Additionally, [redacted] ODT does nothing with and is not altered in any way by the substance of the data signal. Dr. Subramanian testified (adopting the content of RX-4052)) that ODT's operating parameters are changed but in ways unrelated to the data signal—"[ODT's impedance values] depend[] on the operating conditions such as supply voltage and temperature and therefore, need to be dynamically varied."

(RX-4052 at -665825; *see* CX-0889 at -57021-3.) It is therefore difficult, again, to see how the data signal is "received" or "acquired" by ODT as it is, for example, in the first stage of a write operation. Indeed, if one takes up Respondents' suggestion to consider ODT's action in terms of "data" instead of "data signal" (*see* RRB at 7 ("the patent and the parties have used the terms 'data' and 'data signals' interchangeably, meaning the RCVRS and ODT acquire the 'data' at the same time they acquire the 'data signals.'")), it becomes even more difficult to see how the ODT "receives" this information as opposed to ignoring or destroying it.

Accordingly, the undersigned does not find that non-selected memory devices nonetheless "receive" data signals in the Accused Products so as to prevent infringement of this limitation. It is important to note that while Netlist promotes a theory of "receive / do not receive" involving latching, that theory is based on a now-rejected distinction between "data" and "data signal" as used in the '907 patent claims. Further, Dr. Levitt testified that "receive" can occur without latching (Levitt, Tr. at 395:19-22) and as explained above, the undersigned agrees.

Respondents and the Staff appear to offer an additional reason why the limitation is not met. Respondents claim Netlist has provided an insufficient showing of "how the 'first' memory devices receive the 'data signal' . . . *in response* to the first module control signals." (RIB at 23 (emphasis added); RRB at 14-15; *see* SIB at 41-42.) This argument rests upon two incorrect presumptions, however. The first is that second memory devices never "do not receive" data signals (*see* RRB at 14-15 ("[t]hat is incorrect, because all memory devices 'receive' and 'acquire' the data . . . .")); and the second is that Netlist's sole infringement theory is that "receive" only means "latching" (*see id.* at 15 ("Netlist's only theory of infringement . . . . there is no evidence that either the JEDEC standard or the accused products require data to be 'latched' (or not) 'in response to' the chip select signal.")). Neither of these are correct. As discussed above, the

undersigned does not agree that second memory devices are always "receiving" data signals; and Netlist's initial post-hearing brief shows an infringement theory presented in a form of alternatives, where "receive" or "acquire" is accomplished either by latching or [redacted] before sending to the latch. (*See, e.g.*, CIB at 42-43.)

Returning to the record, there appears to be no dispute that [redacted] (CX-2003C at Q/A 385 (citing CX-0889 at -56906), 387, 388, 401 (citing CX-2053); *see* RX-3869C at Q/A 64, 68, 70 (citing RX-3904C).) To the extent there remains a dispute, the undersigned finds this act meets the limitation "in response to the first module control signals, the first memory devices output or receive . . . while the second memory devices do not output or receive . . . ."

Accordingly, the undersigned finds the Accused Products do include this feature of independent claim 1.

> (3) "wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices"

For this limitation, Netlist contends "the evidence shows that each of the nine data buffers is disposed on the PCB in a position 'corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices . . .'" (CIB at 50 (citing, *inter alia*, CX-2003C at Q/A 480).) Netlist views Figures 3A, 3C, and 3D of the '907 patent as showing the meaning of this limitation and matching the layout of the Accused Products where "[e]ach data buffer . . . is specifically located close to, or in a corresponding position respective to, the SDRAM components to which it is connected." (*See id.* at 50-51 (citing CX-2003C at Q/A 480-482; CX-0377 at *14; CX-2602 at *4; CX-0059 at *3; JX-0020C at 98:2-10,

156:13-157:5, 158:18-159:20, 161:22-162:10).) Netlist argues there is no merit to Respondents' contention that "corresponding to" must mean "aligned with" or without any offset. (*See id.* at 51-53.) The Staff agrees with Netlist and argues "the intrinsic evidence supports interpreting the limitation as requiring that each buffer circuit be generally located either aligned or offset with its respective memory devices." (SIB at 61.)

In opposition, Respondents argue:

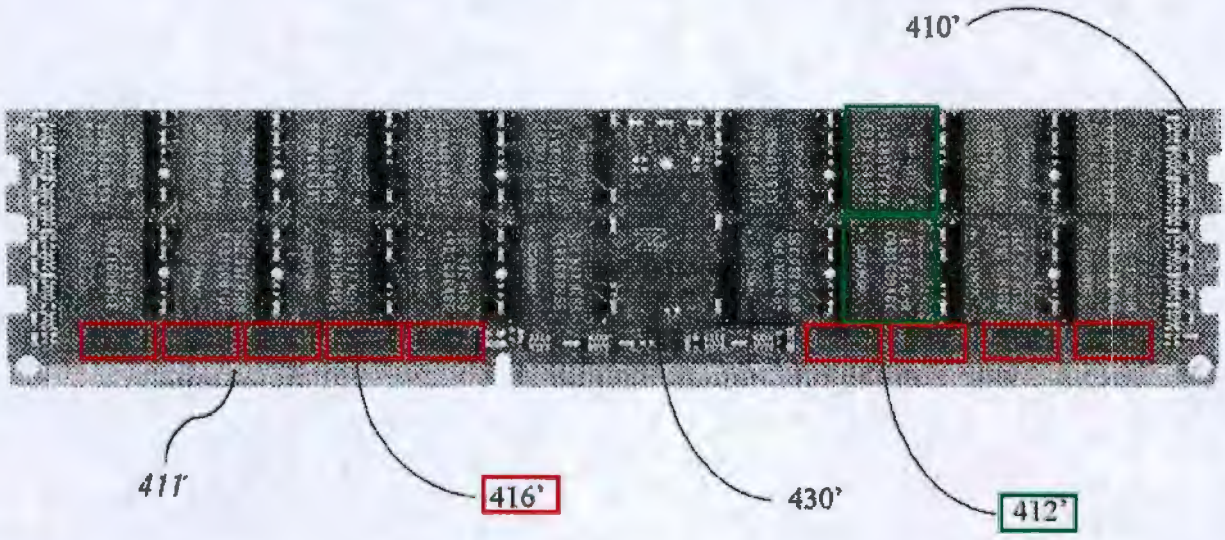
> The data buffers (DBs) in the Accused SK hynix LRDIMM Products (*i.e.*, the accused "buffer circuits") are not positioned such that each buffer "corresponds with" the position of the memory devices to which it is coupled. *See* RX-3869C at Q/A 140–42. Instead, some of the accused DBs correspond to the position of memory devices to which the DB is not coupled (*see, e.g.*, red DB in the demonstrative shown here) and others are between the memory devices (*see, e.g.*, green DB). *See* RX-3869C at Q/A 141–42; *see also* CX-2613.002 (photo of accused product annotated here). Thus, Netlist has failed to show that the accused DBs meet the "corresponding positions" requirement of claim 1 and all asserted dependent claims.

(RIB at 28-29.) Respondents primarily rely on Figure 3C of the '907 patent to show the meaning of "corresponding to." (*Id.* at 28 (citing RX-3869C at Q/A 139).) In their reply brief, Respondents argue "correspond to" cannot refer to similar horizontal ordering of buffers and memory devices as contended by the Staff (RRB at 20 (citing SIB at 35)) or physical close-ness as contended by Netlist (*id.* (citing CIB at 50-51)) and there is no reason to understand Figure 3D of the '907 patent as reflecting this limitation (*see id.* at 20-21).

Here, the undersigned finds the Accused Products meet the limitation. The '907 patent states:

> FIGS. 3C and 3D illustrate the positioning of the data transmission circuits **416'** in accordance with certain embodiments described herein. In certain embodiments, the position of at least one of the data transmission circuits **416'** is *generally aligned* with one or more of the memory devices **412'** to which the data transmission circuit **416'** is operatively coupled.

('907 patent at 12:55-61 (emphasis added).) Admittedly, Figure 3C shows data transmission circuits 416' (*i.e.*, data buffers) as perfectly aligned with the memory devices 412' to which they are connected, but this figure is clearly a conceptual illustration of layout. Figure 3D, on the other hand, is a photograph of an actual memory module and while it shows transmission circuits as offset from the memory devices, the patent discloses this figure as showing "general[] align[ment]." ('907 patent at 12:55-61.) It is undisputed that the Accused Products also employ an offset yet general alignment of data buffers and their respective memory devices such that it is clear, in a plain and ordinary sense, which memory devices each data buffer "corresponds to":



('907 patent at Fig. 3D (annotated));

(RIB at 28; *see* CIB at CX-0377 at *67).)

Accordingly, the undersigned finds the Accused Products do include this feature of independent claim 1.

3. Dependent Claims 2-8, 10, 12, 14, and 15

With respect to dependent claims 2-8, 10, 12, 14, and 15, Netlist contends that there is no dispute over the infringement of these claims by the Accused Products, apart from their dependence on independent claim 1. (CIB at 54.) Netlist cites to the written testimony of Dr. Levitt to fulfill its obligation in establishing the Accused Products infringe these claims. (*Id.* (citing CX-2003C at Q/A 484-557).) Respondents and Staff do not appear to dispute this evidence or Netlist's contention. (RIB at 29; RRB at 5-21; SIB at 36-44; SRB at 6-16.)

In view of the testimony of Dr. Levitt that the Accused Products infringe these claims, there being no clear disagreement by Respondents and Staff as to that fact, and the above determination that independent claim 1 is infringed, the undersigned finds that the Accused Products infringe claims 2-8, 10, 12, 14, and 15 of the '907 patent. (*See* CX-2003C at Q/A 484-557.)

E. Domestic Industry – Technical Prong

Netlist asserts that its Domestic Industry Products practice claims 1-8, 10, 12, 14, and 15 of the '907 patent. (CIB at 5; *see* CIB at 54.) In its opening brief, Netlist explains "Netlist's FPGA HybriDIMM includes a JEDEC-compliant LRDIMM portion that operates identically to JEDEC-compliant LRDIMMs like the Accused LRDIMM Products" and "Respondents and Dr. Subramanian only allege that Netlist's FPGA HybriDIMM does not satisfy the technical prong of the ITC's statutory domestic industry requirement for the same reasons they allege the Accused LRDIMM Products do not infringe." (CIB at 54 (citing [1023 ID] at 43; RX-3869C at Q/A 161; CX-2003C at Q/A 276-288, 598-610).) Thus, Netlist asserts that the practice of claims 1, 2-8, 10,

12, 14, and 15 of the '907 patent by the Domestic Industry Products rises and falls with infringement of the same claims by the Accused Products.

Respondents and the Staff similarly contend that "Netlist's HybriDIMM products fail to satisfy the technical prong of the domestic industry requirement for at least the same reasons that the accused LRDIMM products do not infringe." (RIB at 29; SIB at 64.) Respondents add, however, that even under Netlist's "received" as "latched" theory, there exists an overall failure of proof to show "[the Domestic Industry Products'] second memory devices do not latch any data." (RIB at 29-30 (citing CX-2003C at Q/A 689-690; Levitt, Tr. at 431:2-432:9); RRB at 21-22.) As far as Netlist's reliance on the JEDEC specification to show this, Respondents argue "[t]here is nothing in the JEDEC standards that prevents a non-targeted memory device from latching the data." (*Id.* at 30.) The Staff largely concurs with this assessment, stating, "analysis of 'do not . . . receive' limitation in the DI products required evidence specific to its memory devices – Samsung memory devices. Here, the evidence is insufficient to establish that the DI products satisfy this limitation." (SIB at 65 (citing Levitt, Tr. at 431:21-432:9); *see* SRB at 17-21 (citing *inter alia* *Fujitsu Ltd. v. Netgear, Inc.*, 620 F.3d 1321, 1327 (Fed. Cir. 2010)).)

In its reply brief, Netlist contends Respondents never raised a failure of proof on technical domestic industry "but now piggy back on, this argument [from the Staff]." (CRB at 29.) Netlist takes the position the argument is waived under Ground Rules 9.1, 13.1, and 13.3. (*Id.*) On its merits, however, Netlist argues "the scope of the claims, as informed by the level of skill of a POSITA, does not require any transistor-level analysis" defeats Staff's claim. (*Id.* (citing Levitt, Tr. at 450:2-22, 451:13-453:3, 444:18-446:24, 464:11-25, 465:10-466:18).) Netlist adds that the evidence shows "the DRAM devices are indisputably JEDEC-compliant." (*Id.* at 30 (citing RX-3869C at Q/A 163).)

Here, as an initial matter, the undersigned finds Respondents have waived a challenge to the sufficiency of Netlist's showing the "receive / do not receive" claim limitation as this was not included in their pre-hearing brief. (*See* RPB at 145-151.) Thus, only the Staff's evidentiary challenge is considered and, upon review, the undersigned is not persuaded that satisfaction of the "receive / do not receive" limitation can only be shown with evidence specific to the internal operation of the Samsung memory devices contained in the Domestic Industry Products. The test for technical prong of domestic industry is the same as that for infringement—a preponderance of the evidence standard. *See Crocs, Inc. v. Int'l Trade Comm'n*, 598 F.3d 1294, 1307 (Fed. Cir. 2010); *Cross Med. Prods., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1310 (Fed. Cir. 2005). This standard has been interpreted as a "more likely than not" test which can be satisfied with circumstantial evidence of infringement. *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1318 (Fed. Cir. 2009) (citing *Moleculon Research Corp., v. CBS, Inc.*, 793 F.2d 1261 (Fed. Cir. 1986)). Thus, the undersigned cannot agree that the JEDEC specifications' failure to "govern memory device design" (SRB at 19) or to "mandate the circuitry of the memory devices" (*id.* at 20) necessarily means Netlist cannot show practice of this limitation; and, upon consideration of the evidence that Netlist has presented, the undersigned finds a preponderance of the evidence shows the "receive / do not receive" claim limitation is practiced.

With Respondents' argument on insufficient evidence removed, Netlist and Respondents are otherwise in agreement that Netlist's practice of the limitation rises and falls with infringement by the Accused Products. (CIB at 54; RIB at 29; RRB at 21-22.) As discussed above, the Accused Products have been shown to infringe as the evidence does not support a finding that ODT circuitry or [redacted] (*i.e.*, the two technical grounds on which Respondents dispute infringement) qualify as reception or acquisition of a data

signal. Further, Dr. Levitt presented unrebutted evidence that the Samsung memory devices used in the Domestic Industry Products are JEDEC-compliant (CX-2003C at Q/A 276-288 (citing, *inter alia*, CX-0060C at -58099)) and that this standard involves the use of chip-select signals sent to these memory devices to control whether or not they participate in read or write operations (*id.* at Q/A 652-661 (citing, *inter alia*, CX-0889 at -56906)). Given the lack of argument or evidence from the Staff to the contrary (*see* SIB at 64-65; SRB at 17-21), the undersigned finds that unselected (*i.e.*, inactivated) memory devices instructed not to perform a write operation would correspondingly not perform the first stage of that write operation—*i.e.*, "receive" or "acquire" the data signal. This conclusion is commensurate with that intrinsic evidence relied on by Order No. 17 in construing the "receive / do not receive" claim limitation. (*See* Order No. 17 at 26-28, 33-34.)

Accordingly, and given the above determinations on infringement, the undersigned finds a preponderance of the evidence shows that the Domestic Industry Products practice claims 1, 2-8, 10, 12, 14, and 15 of the '907 patent.

F. Validity

1. Estoppel under 35 U.S.C. § 315(e)(2)

As noted in the above procedural history of this investigation, Respondents have filed numerous petitions for *inter partes* review on the validity of the asserted claims of the '907 patent. At the time of this initial determination, two of those petitions, IPR2018-00362 and IPR2018-00363 (consolidated into IPR2018-00362 (RX-2599 at *5041)), have resulted in a final written decision from the USPTO Patent Trial and Appeals Board, which the parties acknowledge. (CIB at 55; RIB at 5; SIB at 10.) This circumstance implicates 35 U.S.C. § 315(e)(2), which reads as follows:

> (e)Estoppel.—
>
> > (2)Civil actions and other proceedings.—
> >
> > The petitioner in an inter partes review of a claim in a patent under this chapter that results in a final written decision under section 318(a), or the real party in interest or privy of the petitioner, may not assert either in a civil action arising in whole or in part under section 1338 of title 28 or in a proceeding before the International Trade Commission under section 337 of the Tariff Act of 1930 that the claim is invalid on any ground that the petitioner raised or reasonably could have raised during that inter partes review.

35 U.S.C. § 315(e)(2).

Netlist contends Respondents are estopped from presenting obviousness invalidity theories based on prior art references U.S. Patent No. 7,024,518 ("Halbert") and U.S. Pub. No. 2009/0248969 ("Wu"). (*See* CIB at 54-55.) Netlist summarizes:

> As the CALJ correctly stated in Order No. 51, the statutory mandate of U.S.C. § 315(e)(2) is clear: any petitioner who obtains a Final Written Decision ("FWD") from the Patent Trial and Appeals Board ("PTAB") is precluded from advancing any invalidity grounds in the ITC that it raised or reasonably could have raised, before the PTAB. Order No. 51 at 6-8; U.S.C. § 315(e)(2). Respondents obtained a FWD on the asserted '907 patent, and are precluded from advancing invalidity grounds in this Investigation that they raised, or reasonably could have raised, in their IPR petition. *SK hynix, Inc.* v. *Netlist, Inc.*, IPR2018-00362, Paper No. 29 (P.T.A.B. June 27, 2019) ("362 IPR"); U.S.C. § 315(e)(2).

(*Id.* at 54-55.)

Netlist cites one form of "reasonably could have raised" as any patent or publication that a petitioner actually knew about or that a skilled searcher could have been expected to discover. (*See id.* at 56 (citing *Palomar Techs., Inc. v. MRSI Sys., LLC*, 373 F. Supp. 3d 322, 331 (D. Mass. 2019) (emphasis added)).) Netlist notes that the PTAB itself, "conducting a nearly identical estoppel analysis, [] estopped and terminated SK hynix's IPR proceeding based on Halbert and Amidi grounds following the FWD in the Ellsberry IPR." (*Id.* (citing IPR2018-0036[4], Paper 32

at 5-13).) Netlist argues the Federal Circuit holding in *Shaw Indus. Grp., Inc. v. Automated Creel Sys., Inc.*, 817 F.3d 1293 (Fed. Cir. 2016), cited by Respondents to avoid estoppel, is limited to a circumstance of IPR grounds not-instituted by the PTAB, and otherwise cannot occur again in light of the Supreme Court's decision in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1354 (2018). (*Id.* at 56-57.) In other words, according to Netlist, "federal district courts and the PTAB cabined Shaw to its peculiar facts." (*Id.* at 57 (citations omitted).)

Turning back to the Halbert and Wu references, Netlist argues both reasonably could have been raised in IPR2018-00362—Respondents' *inter partes* review proceeding against the '907 patent which resulted in a final decision. (*Id.* at 58-59.) Netlist observes Halbert was asserted in that very IPR (*id.* (citing *SK hynix, Inc.* v. *Netlist, Inc.*, IPR2018-00362, Paper No. 29 at 8-9)) and Wu was raised during the '907 patent's prosecution (*id.* at 58-59 (citing RPB at 177)). Regarding Wu specifically, Netlist contends that any argument from Respondents regarding an uncertainty over Wu's prior art status is belied by their use of Wu in this investigation. (*Id.* at 59.)

In its reply brief, Netlist addresses Respondents priority-date argument as to the Wu reference. (CRB at 34.) It summarily states:

> In this Investigation and in its IPR petitions, Respondents consistently applied July 16, 2009 as the priority date for the actual issued claims of the '907 patent, and based on that date, they consistently contended that Wu is prior art to the '907 patent. *See* IPR 2018-00362, Paper 1 (Petition) at 4 (assuming that "the claims of the 907 patent are entitled to a priority date of July 16, 2009"); Respondents' Disclosure of Invalidity Contentions at 18, n. 5 ("Netlist's corrected disclosure of priority dates…states that the "earliest" priority date for each asserted claim of the '907 patent is July 16, 2009"); Respondents' Invalidity Contentions at 18 ("Wu '969 is prior art to the '907 patent.") (emphasis added).
>
> There is no question that Respondents reasonably could have raised Wu during the IPR proceedings. As a result, they are estopped from continuing to advance the reference here.

(*Id.*) As to Halbert, Netlist disputes that the Staff "opened the door" to these invalidity grounds with its own discussion of Halbert such that Respondents are allowed to argue the same. (CRB at 39-40.) For support, Netlist looks to caselaw which limits the "open door" only to rebuttal evidence from an opponent to "rebut any false impression that might have resulted from the earlier admission." (CRB at 39-40 (citing, *inter alia*, *United States v. Whitworth*, 856 F.2d 1268, 1285 (9th Cir. 1988)).) Netlist asserts Respondents are not an opponent of the Staff and, even if they were, 35 U.S.C. § 315 prevents them "by law from offering any evidence or argument going to the invalidity of the '907 patent on this ground." (*Id.* at 40.) Netlist notes, even then, Respondents go well beyond commenting on the Staff's contentions. (*Id.* (citing RPB at 36-42; SPB at 67-75).)

In opposition, Respondents address estoppel of the Wu reference first. Respondents explain that during prosecution of the '907 patent, the applicant (*i.e.*, Netlist) filed inventor declarations on conception in order to "swear behind" Wu, which had previously been applied to reject the claims by the Examiner; and that the Examiner accepted those declarations such that "Wu is no longer considered prior art." (RIB at 31 (citing RX-2006C at Q/A 117, 118; RX-3627 at *173-188, 316-320).) Respondents reason they therefore "could not have reasonably raised Wu as prior art in its IPRs." (*Id.* (citing 35 U.S.C. § 325(d)).) Aware that they now assert Wu as prior art to the '907 patent, Respondents explain:

> The reason Wu is an invalidity reference here is because after Respondents filed their IPRs, Netlist made the strategic decision to not claim an earlier priority date that would have removed Wu as prior art in this Investigation, without ever conceding it could be considered prior art in the Patent Office. Thus Respondents could not have reasonably raised Wu in their IPR petitions, and estoppel does not apply.

(*Id.* at 31-32.)

With respect to the Halbert and Amidi invalidity ground (hereafter, referred to as "Halbert/Amidi" or "Halbert/Amidi combination"), Respondents' initial brief does not address the

merits of why they believe estoppel does not apply to this reference because, in their view, "it is undisputed that estoppel under § 315 does not apply to Staff, and thus Staff 'opened the door' for the parties to address invalidity in light of Halbert and Amidi." (RIB at 36-37.)

With respect to both of Wu or Halbert/Amidi, Respondents' reply brief cites *Shaw* as foreclosing estoppel through its holding that "Section 315(e)(2) estops an IPR petitioner from asserting grounds that were raised or that could have been raised after institution—*i.e.*, during the actual IPR." (RRB at 22 (citing *Shaw*, 817 F.3d at 1300).) Respondents thus reason "[n]either Wu nor Halbert was included in the 362 IPR petition, and they were unrelated to the grounds included in that petition, which focused on Ellsberry. They therefore could not have been raised 'during that' IPR (*i.e.*, after institution, according to *Shaw*)." (*Id.* at 23.)

For its part, the Staff does not address estoppel as it concerns Respondents, only arguing that its own invalidity contention based on the Halbert reference is not affected by 35 U.S.C. § 315. (SIB at 10 n.15, 65 n.48; SRB at 22 ("Accordingly, to the extent the claims are interpreted broadly, the Staff's evidence shows that the claims of the '907 patent are invalid as obvious").)

Here, the undersigned finds 35 U.S.C. § 315(e)(2) prevents Respondents from "assert[ing]" that the asserted claims of the '907 patent are invalid on the grounds of: (1) obviousness over Wu under 35 U.S.C. § 103; and (2) obviousness over Halbert and Amidi under 35 U.S.C. § 103. With respect to Wu, it is clear Respondents reasonably could have raised this reference in their petition which precipitated the USPTO to institute IPR2018-00362; that petition existing in the record as CX-2684. It is more likely than not that Respondents knew of this reference, as it is cited on the face of the '907 patent. (*See* '907 patent at Page 2.) Additionally, Respondents' contention that Netlist's successful "swearing-behind" prevented Wu from being raised is untenable in light of the following statement included at the beginning of Respondents' IPR petition:

> A. Effective Filing Date of the 907 Patent
>
> The application that resulted in the 907 Patent is a continuation of an application filed on April 15, 2010, now Patent No. 8,516,185 ("the 185 Patent") (Ex.1017), which is a "continuation-in-part" of an application filed on July 16, 2009, now Patent No. 8,417,870 (Ex.1015). Because each of the prior art references identified in this Petition predates July 16, 2009, Petitioner assumes for this Petition only that the claims of the 907 Patent are entitled to a priority date of July 16, 2009. Ex.1003¶¶43-46.

(CX-2684 at -625915.) This statement demonstrates Respondents' petition was not conditioned on what the Examiner accepted as the effective date of invention during the '907 patent's prosecution. There is thus no merit to Respondents' claim that Wu only appears now in this investigation because "Netlist made the strategic decision to not claim an earlier priority date that would have removed Wu as prior art." (RIB at 31.) Clearly, it was not an earlier-than-July 16, 2009 priority date consideration that kept Wu out of Respondents' IPR petition.

With respect to the Halber/Amidi combination, the undersigned first disagrees with Respondents that, should 35 U.S.C. § 315(e)(2) apply to them, they are somehow permitted to piggyback off the Staff's independent assertion of obviousness on these references. The statute estops a petitioner from "assert[ing] . . . that the claim is invalid [on the specified grounds]." *See* 35 U.S.C. § 315(e)(2). Captioning such an assertion as a response to another party's contention is still an assertion of invalidity which the statute does not permit.

Further, 35 U.S.C. § 315(e)(2) does apply to the Halbert/Amidi combination. Unlike Wu, it is particularly difficult to see how this combination would not fall under the "reasonably could have raised" rubric given that Respondents did file an additional *inter partes* review petition based on this ground shortly after the IPR2018-00362 petition. (CX-2695 at 1, 82; CX-2707 at 36.) The undersigned finds the existence of this petition shows it is more likely than not that Halbert/Amidi could have been raised in the *inter partes* review petition of IPR2018-00362. Respondents do not

dispute their ability to have done this (RRB at 22-23) and actually acknowledge their success in having used Halbert and Amidi to successfully invalidate the claims of the parent to the '907 patent—the '185 patent (*see* RIB at 37).

With respect to the *Shaw* decision and its effect upon both Wu and Halbert/Amidi, the undersigned agrees with the reasoning of several district courts and the PTAB itself that *Shaw*'s holding can only apply to the circumstances that were before it—namely, the inapplicability of 35 U.S.C. § 315(e)(2) to invalidity grounds that were included in a petition but not instituted. *See, e.g., Trustees of Columbia University in the City of New York v. Symantec Corp.*, 390 F. Supp. 3d 665, 674, 677-681 (E.D. Va. July 2, 2019); *Oil-Dri Corp. of Am. v. Nestlé Purina Petcare Co.*, No. 15-CV-1067, 2017 WL 3278915, at *7 (N.D. Ill. Aug. 2, 2017) (collecting cases); *SK Hynix Inv. V. Netlist, Inc.*, No. IPR2018-00364, Paper No. 32, at 6-10 (P.T.A.B. Aug. 5, 2019). Indeed, the holding in *Shaw* seems tailored to prevent the injustice faced by that particular petitioner; namely, the prejudice from being estopped from asserting grounds in other tribunals that tbe PTAB decided never to address:

> We cannot say we agree with the PTO's bandling of Shaw's petition. We also cannot say that the PTO's decision made the proceeding more efficient, particularly given that the Payne-based ground was alleged anticipation by a single reference while the two instituted grounds were alleged obviousness over combinations of references.
>
> We have no authority, however, to review the Board's decision to institute IPR on some but not all grounds. "Denial of a ground is a Board decision not to institute inter partes review on that ground." 37 C.F.R. § 42.108(b). We thus lack jurisdiction to review the Board's decision not to institute IPR on the Payne-based ground, which includes its decision not to consider the Payne-based ground in its final written decision.
>
> . . . .
>
> *Shaw's argument is predicated on its concern that the statutory estoppel provisions would prevent it from raising the Payne-based ground in future proceedings.*

. . . .

> The PTO argues that Shaw's statutory interpretation of the estoppel provision is incorrect because "the denied ground never became part of the IPR." PTO Br. 38. We agree with the PTO that § 315(e) would not estop Shaw from bringing its Payne-based arguments in either the PTO or the district courts. Both parts of § 315(e) create estoppel for arguments "on any ground that the petitioner raised or reasonably could have raised *during* that inter partes review." Shaw raised its Payne-based ground in its petition for IPR. the PTO denied the petition as to that ground, thus no IPR was instituted on that ground. The IPR does not begin until it is instituted. *See Cuozzo*, 793 F.3d at 1272 ("IPRs proceed in two phases. In the first phase, the PTO determines whether to institute IPR. In the second phase, the Board conducts the IPR proceeding and issues a final decision." (citations omitted)). Thus, Shaw did not raise—nor could it have reasonably raised—the Payne-based ground *during* the IPR. The plain language of the statute prohibits the application of estoppel under these circumstances. In light of our construction of the statute, mandamus is not warranted. Thus, we deny Shaw's petition for writ of mandamus.

Shaw, 81 F.3d at 1299-1300 (emphasis added). The specter of this injustice, however, has since been eliminated by the Supreme Court in *SAS Inst.*, which held that 35 U.S.C. § 318 requires the PTAB take an all-or-nothing approach to the grounds included in an IPR petition. 138 S. Ct. at 1355 ("Where a statute's language carries a plain meaning, the duty of an administrative agency is to follow its commands as written, not to supplant those commands with others it may prefer. . . . Because SAS challenged all 16 claims of ComplementSoft's patent, the Board in its final written decision had to address the patentability of all 16 claims.") (internal citation omitted). In other words, there will never be another situation like the petitioner's in *Shaw*.

I further note that the *Shaw* panel's interpretation of "during" in 35 U.S.C. § 315(e) as applying strictly to that time period *following* institution of the IPR, is based on a critical, but ultimately incorrect, assumption—that a petitioner actually has an ability to raise additional invalidity grounds, not included in its petition, post-institution. *See Shaw*, 817 F.3d at 1300 ("The IPR does not begin until it is instituted. . . . Thus, Shaw did not raise—nor could it have reasonably

raised—the Payne-based ground *during* the IPR") (emphasis in original)). The PTAB has since confirmed the undersigned's understanding that no such ability exists:

> As Petitioner acknowledges, our rules preclude adding any new grounds of unpatentability following filing of the petition, and these rules have not changed post-*SAS*. Petitioner's argument that subsection 315(e) estops a party only with respect to grounds that could have been raised during the trial (i.e., after institution) would render subsection 315(e) (and our implementing rule) effectively meaningless. That is, the estoppel effects of subsection 315(e), under Petitioner's interpretation of the statute, could not apply to any grounds other than those actually asserted in the earlier petition. Thus, the result of Petitioner's interpretation of the statute, could not apply to any grounds other than those actually asserted in the earlier petition. Thus, the result of Petitioner's interpretation of "reasonably could have raised" is that only grounds raised in the petition that results in a final written decision could be estopped.
>
> Such an interpretation of subsection 315(e)(1) would render superfluous "reasonably could have raised."

SK Hynix Inv. V. Netlist, Inc., No. IPR2018-00364, Paper No. 32, at 7-8. It is therefore determined that *Shaw* does not prevent the application of estoppel to Respondents' Wu and Halbert/Amidi combination.

Accordingly, the undersigned hereby finds that Respondents are estopped from asserting the '907 patent claims are invalid on the grounds of obviousness over Wu or the Halbert/Amidi combination. Those grounds of invalidity not affected by estoppel are addressed below.

2. Obviousness

a) Halbert and Amidi

Netlist does not contend estoppel applies to the Staff or, correspondingly, to the Staff's independent theory of invalidity based on prior art references Halbert (RX-2360) and Amidi (RX-1432). (*See* CIB at 58-59; CRB at 39-40, 41-44, 44-45.) On this issue, the Staff first argues Netlist's decision not to appeal a prior PTO determination that Halbert and Amidi would have been

combined to create the invention claimed in the parent '185 patent "clearly and convincingly shows that the *Halbert* and *Amidi* references would be combined . . . ." (SIB at 67.) The Staff also cites the 1023 ID's determination on which elements of the, again, parent '185 patent are met by the Halbert and Amidi combination such that, in the Staff's view, "[t]he only outstanding claim features [assumedly, of the '907 patent] are memory devices on shared data lines and the 'first module control signals' and 'receive/do not receive' limitations." (*Id.* (citing 1023 ID at 121).) The Staff then discusses additional arguments Netlist made in the "Patent Owner Response" to the '185 patent IPR along with certain excerpts of Amidi (*see* SIB at 67-70) before concluding:

> Accordingly, in the Staff's view, statements that the structure and function of Amidi's chip-select and multiple ranks would direct a POSITA to the combination, and Netlist's failure to contest that Amidi's additional memory ranks would be combined with Halbert's buffer circuit, support finding that the combination of Halbert and Amidi teaches the "chip-select" interpretation of the claims of the '907.
>
> . . . .
>
> Thus, the evidence shows that the claims of the '907 patent, if construed to merely require a chip-select signal to the memory devices for performance/non-performance of the memory read/write command, would have been obvious in light of the combination of Halbert and Amidi.

(*id.* at 69; *see generally id.* at 44-50 (discussing '185 patent IPR history); SRB at 21-22). The Staff then provides a form of claim chart aligning some but not all limitations of claim 1 of the '907 patent to statements made in a certain "Patent Owner Response." (*See* SIB at 71-73.) As to dependent claims, the Staff identifies each along with a citation to Dr. Subramanian's testimony or '185 patent IPR documents. (*Id.* at 73-75.)

In opposition, Netlist describes the Staff's combination of Halbert and Amidi as "unique" as compared to that proposed by Respondents' in this investigation:

> In addition to the combination of Halbert and Amidi advanced by Respondents and Dr. Subramanian, Staff advances yet another unique combination of Halbert and Amidi. Staff's combination is based on (1) a finding from a different agency (2) regarding a different patent (3) using a different standard of proof and different claim construction rules, (4) combined with the testimony of Dr. Subramanian about a figure he did not create showing a version of the Halbert and Amidi combination that he did not advance and (5) an out-of-context portion of a PTAB declaration from Dr. Baker. SPHB at IV.H.4.b; Tr. (Subramanian) at 721:24-725:14; Tr. (Baker) at 829:1-830:25, 831:24-832:16, 833:12-23.

(*Id.*) More generally, Netlist asserts the evidence fails to show one of skill in the art would combine the two references, and even if combined there remains a failure to disclose claim elements 1a, 1b, 1c, 1d, 1e, and 1f of claim 1, and *all* dependent claims. (*Id.* at 62-63.) Regarding motivation to combine, Netlist views the necessary combination as involving:

> (1) adding ranks to Halbert; (2) modifying the functionality of Halbert's register controller by adding Amidi's CPLD logic, which is designed as a separate component from Amidi's register; (3) fundamentally changing the concurrent memory transaction functionality of Halbert's memory ranks to operate in a non-concurrent manner; and (4) altering Halbert's chip select function from operating in a concurrent manner to a non-current manner.

(*Id.* at 63-64.) Netlist claims "[i]n reality, combining these two references would negate the benefits that either could offer alone." (*Id.* at 64 (citing Baker, Tr. at 844:25-845:15); *see id.* at 65-66 (citing Baker, Tr. at 829:8-830:6, 843:22-844:5, 844:25-845:15; CX-2727C at 468, 471, 547-553, 566, 570-571; RX-2006C at Q/A 566).)

Regarding disclosure of particular claim elements, Netlist argues the 1023 ID already found, in an impliedly dispositive manner for claim 1 in this investigation, that "Halbert always reads from or writes to all of its disclosed memory devices." (*Id.* (citing 1023 ID at 131-133); *see id.* at 64-65 (citing Baker, Tr. at 829:18-830:2, 839:19-840:2, 843:5-8, 843:12-16, 845:2-15; CX-2727C at Q/A 529).) Further, Netlist claims the Halbert and Amidi combination "is still not configured to control its interface circuits using a CAS latency parameter" in apparent relation to

dependent claim 8 (*see id.* at 65-66 (citing CX-2727C at Q/A 468, 570; CX-2631 at 4:6-59)) and there is no sufficient motivation to use tri-state logic devices, in apparent relation to claim 14 (*id.* at 66 (citing CX-2727C at Q/A 566)).

In its reply brief, Netlist addresses the Staff's obviousness theory of Halbert and Amidi—a theory which it characterizes as "a different combination" than Respondents' and one which appears to be based on an IPR final written decision for the '185 patent and not the '907 patent. (*Id.* at 41.) Netlist also disputes that any waiver has occurred based on acts not taken in relation to that IPR, either in fact or by law (*see id.* at 41-42) and that the claims of the '907 patent are as similar to the '185 patent so as to provide a probative comparison (*see id.* at 42-43 (citing SIB at 67)). Even then, Netlist argues the Staff compares the two incorrectly. (*See id.* at 43.) As to dependent claims, Netlist primarily takes issue with the Staff's reliance on Dr. Subramanian's testimony—a problem, according to Netlist, because these claims require antecedent basis in claim 1 and the Staff's claim 1 analysis is fundamentally different than Respondents'. (*Id.* at 44-45.)

Upon review of the parties' briefings, it first appears there is no dispute that Halbert, Amidi, or any of the other cited art, qualify as prior art to the '907 patent. Additionally, the undersigned finds the parties' discussions of Halbert/Amidi lackluster. Netlist has not complied with the spirit of Ground Rule 13.3 (Order No. 22) with its conclusory statement "the combinations of these references advanced by Respondents and Staff do not disclose claim elements [1a], [1b], [1c], [1d], [1e], [1f] of claim 1, or any of the dependent claims" (CIB at 63) followed only with a discussion of "CAS latency" (*id.* at 65 (relevant to claim 8)) and "tri-state logic" (*id.* at 66 (relevant to claim 14)).

As to whether the Staff has presented its own independent Halbert/Amidi invalidity theory, the undersigned cannot discern that theory from the record. The Staff's briefing includes no

explanation how a Halbert and Amidi combination renders each and every limitation of independent claim 1 of the '907 patent obvious, opting instead for a more general discussion on how prior '185 patent IPR proceedings confirm Halbert and Amidi are combinable (*see* SIB at 44-50), the combination discloses "receive/do not receive" (*id.* at 67-70), and other "conflicting arguments" from Netlist (*id.* at 71-73). As to dependent claims, the Staff changes tact and lists each claim next to varying citations of expert testimony or '185 patent IPR documents, at least one of which, RX-2451, is not in evidence. (*Id.* at 73-74.) In light of these deficiencies, especially with respect to independent claim 1, the undersigned finds the Staff has not presented a clear and convincing theory of invalidity.

Accordingly, claims 1-8, 10, 12, 14, and 15 of the '907 patent have not been shown to be obvious, and thus invalid, in light of Halbert, Amidi, and other prior art.

b) QBM Products

Respondents contend a combination a collection of prior art products from third-party Kentron, referred to as the "QBM Products" (RIB at 44) renders claims 1-8, 10, 12, 14, and 15 obvious (*id.* at 44-45) alone and when in combination with other prior art. Respondents begin by first explaining:

> The QBM products went through an evolution. Subramanian, Tr. 768:3–:11. First built with two ranks and without a command/address register, the next generation of QBM was designed with an Advanced Buffer and, optionally, with four ranks. *See* RX-2006C at Q/A 224; RDX-2006C.307; Subramanian, Tr. 757:23–758:16. Such a four-rank QBM with standard memory stacking rendered obvious the asserted claims. RX-2006C at Q/A 1045-1189.

(*Id.* at 44.) To show how each limitation of claim 1 ([1.a] through [1.h]) is either disclosed or obvious in light of the QBM Products, Respondents rely on Dr. Subramanian's testimony and analysis. (*See id.* at 44-45 (citing RX-2006C at Q/A 1046-1063).) Respondents rely even more

entirely on that testimony for the dependent claims. (*Id.* at 45 (citing RX-2006C at Q/A 1064-1085, 1136-1157).)

In their reply brief, Respondents observe Netlist as failing to dispute that the QBM Products incorporate a distributed buffer architecture (RRB at 30 (citing CIB at 69-72)) and emphasize that the QBM2 product was an "evolution" of QBM1 making it obvious that features of one would be combined into the other (*id.* at 30-31 (citing RX-2006C at Q/A 1050, 1124-1125)). Respondents restate their contention that registering and re-driving a signal is "producing" that signal under claim 1, and further contend Netlist misinterprets their theory and evidence as it concerns dependent claim 8. (*Id.* at 31-32.)

In opposition, Netlist argues "the evidence establishes that Respondents' QBM Products combination does not disclose elements [1a], [1b], [1c], [1d], [1e], [1f] of claim 1 or any dependent claims of the '907 patent." (CIB at 69 (citing CX-2727C at Q/A 1135-1229).) Netlist contends Dr. Subramanian has applied a variety of secondary references to cure these deficiencies, but does so "without explaining why a person of ordinary skill in the art would have been motivated to combine them with the QBM Products." (*Id.* (citing CX-2727C at Q/A 1275-1325).) Netlist continues:

> While Respondents refer to this "reference" as the "QBM Products," it is actually the combination of two separate products (including at least preliminary—but not implemented— design(s), the QBM1 Product, and the QBM2 Product), and 13 different documents to create a fictitious product that never existed. CX-2727C (Baker) at Q/A 1127; Tr. (Subramanian) at 654:16-659:25. Moreover, Respondents provided no analysis regarding why a person of ordinary skill in the art would have been motivated to combine the QBM1 product with the QBM2 product, let alone combine both product versions with every technical disclosure ever made about either of them. In fact, a skilled artisan would have not have been motivated to combine and/or modify any of these disclosures to create the combination. CX-2727C (Baker) at Q/A 1125-1132.

(Id at 70.) Netlist views one particular modification, the addition of JEDEC standard command and address registers to the QBM1 module, as prohibited by the QBM designers' rejection of such a change (*id.* (citing CX-2727C at Q/A 1142)) and, even if done, it would not meet the "produce" claim element (*id.* at 71 (citing CX-2727C at Q/A 1195); *see* CRB at 46). Netlist also asserts there is a failure of the QBM Products to disclose the timing control of claim 8 (CIB at 71 (citing CX-2727C at Q/A 1217)) or suggest any number of ranks beyond two would be used (*id.* at 71-72 (citing CX-2727C at Q/A 1170); *see* CRB at 45-46). As to dependent claims, Netlist's reply brief points out Respondents do not present a claim-by-claim analysis, and improperly summarize these claims "recite only conventional techniques" in violation of Ground Rule 13.1. (CIB at 46 (citing RIB at 45).) Netlist adds that Respondents' presentation on these claims otherwise fails to go beyond the mere showing that each element was known in the art. (*Id.* at 47 (citing *KSR*, 550 U.S. at 418).)

The Staff takes the position that the QBM Products fail to "show all of the limitations of the '907 patent." (SIB at 76.) The Staff appears to take issue with Respondents' contention that the QBM Products were envisioned to consist of four ranks of memory, thereby preventing clear and convincing evidence of invalidity. (*See id.*)

Upon review of the parties' briefings, it first appears there is no dispute that the QBM Products or, more specifically, the QBM1 and QBM2 products along with that collection of documents describing these products, qualify as prior art to the '907 patent. Additionally, the undersigned notes that the arguments contained in the parties' briefings are cursory and conclusory in nature. For independent claim 1, Respondents make only a cursory attempt to explain how the QBM Products match claim elements (RIB at 44-45), and for dependent claims, cite to questions and answers in Dr. Subramanian's testimony without any real explanation (*id.* at 45; RRB at 31

(addressing claim 8 in passing)). For its part, Netlist offers the summary statement that "the evidence establishes that Respondents' QBM Products combination does not disclose claim elements [1a], [1b], [1c], [1d], [1e], [1f] of claim 1, or any of the dependent claims" (CIB at 69) but follows only with discussions of "registering and re-driving of chip select signals" (*id.* at 71 (relevant to claim limitation 1b)), "scheduling EN/DIS and W/R commands" (*id.* (relevant to claim 8)), and four ranks of memory (*id.* at 71-72 (relevant to claim limitation 1c)). While these heavily abbreviated discussions are not a violation of the Ground Rules per se, they are—in essence—"incorporating by reference" an expert's testimony in an attempt to circumvent the page limits on post-hearing briefing, and are not the caliber of briefing expected from the parties given the disputed status of these issues. Nevertheless, all limitations of independent claim 1 and the asserted claims depending therefrom are discussed below.

To begin and with respect to limitation 1a, Respondents contend the QBM Products disclose this element. (RIB at 44 (citing RX-2006C at Q/A 1046-1047).) Upon review of the cited testimony and evidence, the undersigned finds that this element disclosed. Dr. Subramanian has persuasively explained how the QBM Products consisted of a DIMM module which communicated with a system memory controller through standardized control and sets of data lines in 64 or 72-bit bus widths. (RX-2006C at Q/A 1047.) Netlist's expert, Dr. Baker, does not dispute this limitation in his testimony. (*See* CX-2727C at Q/A 1136.) Therefore, limitation 1a is met.

With respect to limitation 1b, Respondents contend the QBM Products render this element obvious. (RIB at 40 (citing RX-2006C at Q/A 1048-1050; Subramanian, Tr. at 763:13-764:6).) Upon review of the cited testimony and evidence, the undersigned finds that this element would have been obvious. Dr. Subramanian has persuasively explained that use of registers on memory modules to buffer incoming address and command signals and then retransmit these signals to

memory devices was known and otherwise contemplated by the QBM designers, and would have provided the benefit of decreasing the load on these lines. (RX-2006C at Q/A 1049.) Dr. Subramanian also explained how another circuit within the QBM1 product generates a "BE" signal which, when sent to a "2 to 1 QBM Bus switch," effectively controls the routing of data to one of two ranks, or banks, of memory devices (*id.* (citing RX-3201; RX-3205)) and how compatibility objectives would have motivated a person of ordinary skill to place all of these signal generations on the memory module as opposed to the memory controller—and did so motivate the QBM designers themselves in providing an "Advanced Buffer" in the QBM2 product which sends "EN/DIS" and "W/R" signals to QBM Switches and "ADD/CMD" signals to memory devices (*see id.* (citing, *inter alia*, RX-3211C at -68717, -68718; RX-3212 at -268903, -268918; RX-3208 at -283990, -283991)). To the extent Netlist argues the QBM designers' decision not to use a register shows it would not have been obvious to one of ordinary skill (*see* CIB at 71), this is effectively a "teaching away" argument, which is not persuasive given Netlist's failure to show any disparagement or discouragement towards the use of a register. *In re Peterson*, 315 F.3d 1325, 1332 (Fed. Cir. 2003) ("While [the prior art reference] mentions a preferred alloy that does not contain rhenium, it does not disparage or otherwise discourage the use of alloys containing rhenium."); *see Santarus, Inv. V. Par Pharm., Inc.*, 694 F.3d 1344, 1356 (Fed. Cir. 2012) ("Describing a formulation as 'second best' is not a 'clear discouragement,' as is required by our precedent.").

Netlist's expert, Dr. Baker, also argues against this compatibility objective with, "[i]t is therefore unclear to me how a person of ordinary skill in the art would have desired to make the QBM Product compliant with an *existing* JEDEC Standard when the premise of the inventions and disclosures is that [QBM] is a new technology." (CX-2727C at Q/A 1145.) The undersigned

disagrees given the undisputable importance that standardization has to the memory module market. The evidence shows even "new" module technologies, if they are ever to be used, must be incorporated into products which comply with standards in order to be adopted by consumers. (*See, e.g.*, '907 patent at 1:59-67 ("In general, once the memory space is defined for an electronic system, it would not be feasible to modify the memory space without an extensive design change. This is especially true for the case in which a memory space is defined by a consortium, such as the Joint Electron Device Engineering Council (JEDEC)."); CX-2003C at Q/A 89-106; RX-2006C at Q/A 425.)

Additionally, Netlist and Dr. Baker challenge whether the QBM Products "produce" module control signals by simply registering and re-driving those signals. (CIB at 71; CX-2727C at Q/A 1162-1165.) As discussed above, Order No. 17 construed "produce" as "create, *i.e.*, bring into existence." (Order No. 17 at 135.) It is logical to assume that to drive a signal is to create it. Thus, signals which are *re*-driven are, in effect, recreated (*i.e.*, produced) in satisfaction of the element. The undersigned further notes the '907 patent's discussion of its own buffers as "regenerating" signals. ('907 patent at 16:64-7:4.) Therefore, limitation 1b is met.

With respect to limitation 1c, Respondents contend the QBM Products render this element obvious in combination with other art. (RIB at 44-45 (citing RX-2006C at Q/A 1051-1053; RX-1433; RX-1434; RX-0338; RX-2597; RX-3198; RX-1432).) Upon review of the cited testimony and evidence, the undersigned finds that this element would have been obvious in light of Amidi. Dr. Subramanian has persuasively shown that adding two additional ranks to the pre-existing two ranks of the QBM Products would have been an obvious modification to obtain the cost benefit of using four lower-density memory devices in place of two higher-density memory devices, as in,

for example, Amidi. (RX-2006C at Q/A 1049, 425; RX-1432 at [0008]-[0010], Figs. 5, 6A.)[9] Netlist's opposition to a motivation to add additional ranks to the QBM Products (CIB at 71-72) fails to address the this technique known as rank multiplication and while Dr. Baker mentions it, he does not, therefore, discuss the benefits it would bring (CX-2727C at Q/A 1151-1152, 1168-1172). Additionally, based on at least the above disclosures, the analogous nature of the QBM Products, Amidi, and the '907 patent cannot reasonably be questioned.

Dr. Subramanian has also shown it would have been obvious, and actually contemplated by the QBM designers, to place one of the additional ranks on the same bus as a first original rank, and the other additional rank on the same bus as a second original rank (*i.e.*, stacked memory devices)—and to selectively activate the ranks which share a data bus through standardized chip-select signals. (*Id.* at 1052 (citing, *inter alia*, RX-3206C at -279836); *see* RX-1451 at -6402).) As discussed above on the issue of infringement and domestic industry, the undersigned finds a person of ordinary skill in the art would understand well-known "chip select signals" as causing a memory device, or memory chip, to receive or not receive a data signal associated with a write operation—as well as cause a memory device to output or not output a data signal associated with a read command. Put another way, these known signals are a means to select which memory devices participate in a read or write command. (RX-1433 at -48062, -48068; RX-1451 at -6397, -6400-6403; RX-2006C at Q/A 1052-1053.) Indeed, based on the record, the undersigned is unaware of any technique other than chip-select signals for preventing conflicts on a set of data lines shared by two or more memory devices. *KSR*, 550 U.S. at 421 ("When there is a design need or market

[9] The undersigned observes that Dr. Subramanian's discussion of motivation to combine occurs in the context of limitation 1b, even though he does not tie the combination to any sort of grounds for satisfying that limitation. (*See* RX-2006C at Q1048-1050.) This is contrasted with limitation 1c where the combination is directly relied on.

pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.") To the extent Netlist criticizes Respondents for not identifying with specificity which memory devices are "first" and "second" in this configuration (*see* CX-2727C at Q/A 1172), the undersigned finds it clear that the "first memory devices" and "second memory devices" would be those which are stacked and share a set of data lines coming from the QBM switch, and must therefore respond alternatingly to chip-select signals so as to not cause data conflicts on their shared lines (*see* RX-2006C at Q/A 1052). Therefore, limitation 1c is met.

With respect to limitation 1d, Respondents contend the QBM Products render this element obvious. (RIB at 45 (citing RX-2006C at Q/A 1054-1057).) Upon review of the cited testimony and evidence, the undersigned finds that this element would have been obvious. Dr. Subramanian has persuasively shown that the QBM Products rely on QBM switches, each placed in the data path between the external memory controller and the memory devices. (RX-2006C at Q/A 1055 (citing RX-3206 at -279836).) The evidence shows each QBM switch communicates on a set of eight data signal lines leading to the external memory controller, and two sets of eight data signal lines each leading to a memory device (two memory devices total, one from each rank). (RX-3206 at -279836).) Dr. Subramanian has persuasively explained that when two additional ranks are "stacked" on the two existing ranks, each memory device of the additional ranks would naturally share the set of data lines with the memory device they are stacked upon. (RX-2006C at Q/A 1052.) Dr. Baker does not dispute this limitation beyond a disagreement that it would have been obvious to add additional ranks of memory to the QBM Products. (CX-2727C at Q/A 1182-1184.) Therefore, limitation 1d is met.

With respect to limitation 1e, Respondents contend the QBM Products render this element obvious. (RIB at 45 (citing RX-2006C at Q/A 1054-1057).) Upon review of the cited testimony and evidence, the undersigned finds that this element would have been obvious. Dr. Subramanian has persuasively explained how the QBM Switches present in the QBM Products respond to ME, W/R and BE signals sent from the Advanced Register to allow or disallow 8-bit data segments to be communicated between the external memory controller and each memory device connected thereto. (RX-2006C at Q/A 1057.) Dr. Baker does not meaningfully dispute this limitation. (CX-2727C at Q/A 1185-1187.) Therefore, limitation 1e is met.

With respect to limitation 1f, Respondents contend the QBM Products render this element obvious. (RIB at 45 (citing RX-2006C at Q/A 1058-1059).) Upon review of the cited testimony and evidence, the undersigned finds that this element would have been obvious. Dr. Subramanian has persuasively explained how the QBM Switches present in the QBM Products (which, when given additional ranks, connect to four memory devices each) used buffers on the DQ data lines (RX-3208 at -283984) such that the external memory controller only sees one load at the input pin of the switch (RX-3211 at -68717). Dr. Baker does not meaningfully dispute this limitation. (CX-2727C at Q/A 1188-1190.) Therefore, limitation 1f is met.

With respect to limitations 1g and 1h, there appears to be no dispute that the QBM Products render obvious limitations 1g, and 1h of independent claim 1. (*See* CIB at 69; CRB at 45-47.) In light of Dr. Subramanian's undisputed testimony on these limitations and claims (RX-2006C at Q/A 1060-1063), the undersigned finds that these elements would have been obvious. Therefore, limitations 1g and 1h are met.

With respect to dependent claim 2, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-

1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim would have been obvious in light of Amidi. Dr. Subramanian has persuasively explained how accomplishing the known technique of rank multiplication as disclosed in Amidi (RX-1432 at Figs. 6A, 8) would require a larger number of chip select signals sent to the increased number of memory devices as compared to the number of chip select signals received by the QBM Products' Advanced Buffer circuit (RX-2006C at Q/A 1065). Dr. Baker does not dispute rank multiplication's need for additional signals. (CX-2727C at Q/A 1191-1197.) Therefore, claim 2 is met.

With respect to dependent claim 3, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim is so disclosed. Dr. Subramanian has persuasively explained how the QBM Switch of the QBM Products presents a load equivalent to the load of one memory device despite having multiple memory devices connected to it; specifically, less than 3pF. (RX-2006C at Q/A 1067; RX-3208 at -283977; RX-3211C at -68717 ("System sees only 1 load at input of Switch pin.").) Dr. Baker does not meaningfully dispute this claim. (CX-2727C at Q/A 1198-1200.) Therefore, claim 3 is met.

With respect to dependent claim 4, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim would have been obvious. Dr. Subramanian has persuasively explained how, when rank multiplication is employed, stacked memory devices sharing a set of data lines must receive different chip select signals to avoid data conflicts. (RX-2006C at Q/A 1069.) Dr. Baker does not

meaningfully dispute this need or this claim. (CX-2727C at Q/A 1201-1203.) Therefore, claim 4 is met.

With respect to dependent claim 5, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim would have been obvious. Dr. Subramanian has persuasively explained how a person of skill in the art would be motivated to design the QBM Switch, located between the memory devices and the external memory controller, such that the load presented to the memory devices is the same as the memory controller would present to avoid signal integrity issues due to mismatched loads. (RX-2006C at Q/A 1071; *see, e.g.*, RX-1436 at -48313.) Dr. Baker does not meaningfully dispute this claim. (CX-2727C at Q/A 1204-1206.) Therefore, claim 5 is met.

With respect to dependent claim 6, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim has not been shown to be obvious. While Dr. Subramanian has shown that the QBM Switches were one byte wide (RX-3206C at -279836) and explains that "it was well known at the time to use either four or eight bit wide memory devices to build 72 bit wide modules" (RX-2006C at Q/A 1073), the same QBM Products materials show memory devices which are also one byte (*i.e.*, 8 bits) wide (RX-3206C at -279836), his opinion on why a person of ordinary skill would use or try to use memory devices which were not also one byte wide (*i.e.*, "a second data width different from the first width") is conclusory by only stating that such memory devices were known (*see* RX-2006C at Q/A 1073). This is not sufficient. *KSR*, 550 U.S. at 418 ("As is clear from cases such

as *Adams*, a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art."). Therefore, claim 6 is not met.

With respect to dependent claim 7, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim is so disclosed. The QBM Switches in the QBM Products are controlled by a "W/R" signal which controls the direction of data flow to the memory devices (as in a write operation) or from the memory devices (as in a read operation). (RX-3205 at *11, 12, 15; RX-3208C at -283990.) Dr. Baker does not meaningfully dispute this claim. (CX-2727C at Q/A 1212-1214.) Therefore, claim 7 is met.

With respect to dependent claim 8, Respondents contend the QBM Products disclose this claim. (RRB at 31 (citing RX-2006C at Q/A 1076-1077, 1148-1149).) Upon review of the cited testimony and evidence, the undersigned finds that this claim is disclosed. Dr. Subramanian testified that the "Command Scheduler" in the QBM Products' Advanced Buffer uses the latency parameter set in the JEDEC mode register with bits A6-A4 to control QBM Switch timing. (*See* RX-2006C at Q/A 1077.) Netlist's expert, Dr. Baker, does not dispute that the Advanced Buffer uses this parameter, only that control over the timing of signals sent to the QBM Switch does not mean control over the timing of the data signals passing through that switch. (CX-2727C at Q/A 1217.) The undersigned finds, however, that control over the timing of the QBM Switch's status of read or write (the W/R signal) is control over the timing of the signal passing through that switch, analogous to the use of latency disclosed in the '907 patent:

> As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the

> particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits 416. During the latency, address and control signals pass from the memory controller 420 to the control circuit 430 which produces controls sent to the control logic circuitry 502 (e.g., via lines 432) which then controls operation of the components of the data transmission circuits 416.
>
> . . . .
>
> For a write operation, during the CAS latency, the control circuit 430, in one embodiment, provides enable control signals to the control logic circuitry 502 of each data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data.

('907 patent at 15:52-16:2.) Therefore, claim 8 is met.

With respect to dependent claim 10, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim would have been obvious. As with claim 4, Dr. Subramanian has persuasively explained how stacked memory devices sharing a set of data lines must receive different chip select signals to avoid data conflicts. (RX-2006C at Q/A 1069, 1079.) Dr. Baker does not meaningfully dispute this need or this claim. (CX-2727C at Q/A 1201-1203, 1218-1220.) Therefore, claim 10 is met.

With respect to dependent claim 12, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim has not been shown to be obvious. As with claim 6, Dr. Subramanian has not explained why a person of ordinary skill would use or try to use memory devices which not the same bit width as the Advanced Buffer to which the memory devices are connected. (RX-2006C at Q/A 1073, 0181). Therefore, claim 12 is not met.

With respect to dependent claim 14, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim is so disclosed. Dr. Subramanian testified that a person of ordinary skill would have understood from a QBM Switch Block Diagram that the QBM Switch includes tri-state buffers responsive to the "WR and RD signals." (RX-2006C at Q/A 1083; *see* RX-3208C at -283984, -283985, 283988.) Dr. Baker does not meaningfully dispute this disclosure or claim. (CX-2727C at Q/A 1224-1226.) Therefore, claim 14 is met.

With respect to dependent claim 15, Respondents contend it is perhaps "disclosed by, but at least obvious in light of" the QBM Products. (RIB at 45 (citing RX-2006 at Q/A 1064-1085, 1136-1157).) Upon review of the cited testimony and evidence, the undersigned finds that this claim is so disclosed. The QBM Switch of the QBM Products is disclosed as being one byte (*i.e.*, 8 bits) wide with a corresponding 8-bit wide set of data signal lines leading to the external memory controller. (RX-3206C at -279836.) Dr. Baker does not meaningfully dispute this disclosure or claim. (CX-2727C at Q/A 1227-1229.) Therefore, claim 15 is met.

Accordingly, claims 1, 2, 3, 4, 5, 7, 8, 10, 14, and 15 have been shown to be obvious, and thus invalid, in light of the QBM Products and other prior art. Claims 6 and 12 have not been so shown.

c) Secondary Considerations

Netlist's initial brief contends objective indicia of non-obviousness of the '907 patent claims include: "(1) commercial success and licensing, (2) satisfaction of long-felt need, (3) failed attempts by others, (4) copying, (5) unexpected results, and (6) industry praise." (CIB at 76 (citing CX-2727C at Q/A 1329-1357; JX-0030C at 144:1-147:25).) To show these considerations, Netlist

primarily relies on the explanations of Dr. Baker, the alleged adoption of its patents by the JEDEC standardization group, and the development agreement it signed with Samsung. (*See id.* at 76-77 (citations omitted).) Netlist's reply brief briefly addresses this topic, only arguing that "there is no holding in the 1023 [Investigation] that would establish that its claims are not essential to JEDEC standards" and, as shown in other sections, "the '907 Claims map to JEDEC DDR4 LRDIMM Standards." (CRB at 47 (citing CX-2727C at Q/A 1345-1348).)

Respondents dispute the existence of any of these considerations and assert that "[s]econdary considerations must result from what is claimed and what is novel in the claim, otherwise there is no nexus." (RIB at 46 (citing *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011)).) Respondents argue no such nexus has been shown. (*Id.*; *see* RRB at 33-34.) In particular, Respondents claim "load reduction," "rank multiplication," and "distributed buffers" were known in the prior art. (RIB at 46-47 (citing RX-2006C at Q/A 1202-1203; Hong, Tr. at 137:24-138:10; RX-2599 at *5041-5134); *see* RRB at 33 (citing RX-2006C at Q/A 1213).) Respondents add that "[e]vidence regarding HybriDIMM is likewise irrelevant, at least because any alleged success was due to flash memory aspects that are not covered by the 907 claims." (RIB at 47 (citing RX-2006C at Q/A 1222-1225); RRB at 33.) Regarding JEDEC standards, Respondents assert that "Netlist never proposed anything to JEDEC, and instead was trying to distinguish its products from the standard." (*Id.* (citing RX-2006C at Q/A 1205-1209); *see* RRB at 32 (citing RX-2006C at Q/A 133-136).) As to commercial success, Respondents' reply brief states "the overwhelming majority of the 'multi-billion-dollar' memory module market referenced by Netlist is properly attributed to the DRAM chips (and other related intellectual property), not the aspects of the accused RCD and Data Buffers allegedly practiced by the 907 patent." (RRB at 33 (citing RX-2006C at Q/A 1197-2000).)

The Staff agrees secondary considerations do not support non-obviousness in this investigation. (SIB at 76.) The Staff particularly agrees that "the problem to be solved, and motivation and manner of combining distributed buffers with the known RDIMM architecture (and/or Amidi's chip-select structure and function) is strongly taught in the prior art references – per Netlist's own characterization of the references." (*Id.* at 77.)

Upon review of Dr. Baker's testimony on this issue, and the evidence cited therein, the undersigned finds little connection, or "nexus," to the invention of the '907 patent and Netlist's proposed considerations so as to outweigh the above determinations of obviousness. First, with the exceptions of licensing and industry praise, these considerations largely turn on accepting Netlist's assertion that the '907 patent was adopted or incorporated into the standard, and it was that "standardization" that led to all the commercial success LRDIMMs encountered in the market. (*See* CIB at 76-77; CX-2727C at Q/A 1333, 1339-1340, 1344, 1345-1348, 1350-1352.) The only feature of the '907 patent claims mentioned in Netlist's briefs as supposedly causing this chain of events, however, is "Netlist's distributed buffer architecture and related technology." (CIB at 77.) The above invalidity analysis shows this (along with load isolation stemming from the use of buffers) was a known feature, and Netlist's CEO could not dispute this fact at the hearing. (Hong, Tr. at 137:5-138:10 ("Q. And let's put [QBM Products disclosure] up side by side. Let's pull up CDX-2001, your witness statement, and RX-3205. And, in fact, it shows the same distributed buffer architecture you said in your witness statement Netlist invented; right? A. Yes.").) Thus, contrary to Dr. Baker's claim of "JEDEC knew of Netlist's innovative distributed buffer technology taught by the '907 patent prior to incorporation, and incorporated it anyway" (CX-2727C at Q/A 1346), the evidence shows it is more likely the JEDEC organization (comprised of persons of ordinary skill in the art) knew of distributed buffer technology prior to Netlist's '907

patent. Indeed, the evidence shows Netlist was not the agent who supplied this proposal to the DDR4 working groups. (*See* RIB at 47 (citing RX-2006C at Q/A 1205-1209); *see* RX-2006C at Q/A 136; JX-0044C at 180:10-181:4; JX-0027C at 118:14-20; JX-0028C at 276:1-5; JX-0030C at 35:1-14, 153:1-11; JX-0035C at 39:3-19; JX-0039C at 25:20-26:21.)

As to licensing, Netlist points to its Samsung agreement (CIB at 76), but again, there is no showing that any substantive portion of the consideration paid by Samsung can be attributed to the '907 patent, as opposed to other members of its patent portfolio or even to the joint-development aspects of that agreement. Additionally, Netlist mentions other "industry participants have shown a willingness to license Netlist's patents," but there is no mention of these entities or how far that willingness goes in the evidence cited. (*See* CIB at 76 (citing CX-2727C at Q/A 1330-1334).)

As for praise from others, Netlist points to a variety of documents and articles "prais[ing] the performance that Netlist's distributed buffer architecture and related technology allowed" (CIB at 77); but, again, "distributed buffer architecture" cannot be said to be "Netlist's." Moreover, Dr. Baker provides no more than an identification of titles for a majority of the cited publications. (*See* CX-2727C at Q/A 1356.) For those remaining documents, Dr. Baker does not sufficiently explain a connection between the subject matter of the praise and features of the '907 patent claims. (*See id.* at Q/A 1355 (citing CX-0821; CX-0827; CX-0838).) These articles also appear to be reprints of Netlist-issued press releases, as opposed to outside evaluations, as all three contain safe harbor statements concerning "our products" such as "HyperCloud™." (*See* CX-0821; CX-0827; CX-0838.)

Accordingly, the undersigned does not find sufficient secondary considerations of non-obviousness have been shown so as to disturb the above determinations of obviousness.

3. Written Description

In addition to obviousness, Respondents contend Netlist's "straight-line" interpretation of independent claim 1 of the '907 patent, all asserted claims are invalid for lack of written description under 35 U.S.C. § 112 (pre-AIA). (RIB at 47-50.) Specifically, Respondents argue "the specification only provides support for a 'fork in the road' layout, where data is sent to one 'fork' and not the other 'fork.' . . . Netlist's proposed construction (adopted by ALJ Pender), however, essentially covers just one 'fork,' as shown here, and ignores the other 'fork.'" (*Id.* at 48.) To explain, Respondents provide an unnumbered demonstrative showing an annotated version of Figure 4A of the '907 patent. (*Id.*) Even more specifically, Respondents argue:

> Netlist's claim construction (adopted by ALJ Pender) has two problems: First, there is no written description for preventing data sent to the "first memory device" (*e.g.*, 412A above) from also being received (and acquired) by the "second memory device" on the same fork (*e.g.*, 412C above). *See* RX-2006C at Q/A 90–91, 162–66, 170–74. Instead, the patent repeatedly discloses that data sent to 412A is also received by 412C. *See id.* at Q/A 90–91; RX-3869C at Q/A 37–39. According to the patent, it is 412B and 412D (not 412C) that do not receive any data sent to 412A. *See supra* p. 13 (annotating Figure 4A to show what is actually disclosed by the patent).
>
> Second, there is no written description for any embodiment *without* the "fork in the road." RX-2006C at Q/A 54–123, 162, 171–74. Under relevant case law, the fork in the road layout "permeates the entire patent" and there is "no hint or discussion" of a straight line configuration without a fork in the road. *Rivera v. Int'l Trade Comm'n*, 857 F.3d 1315, 1320 (Fed. Cir. 2017) (affirming invalidity for lack of written description). It is improper as a matter of law to ignore one of the "forks" in Figure 4A above, as done by Netlist, because there must be written description for the *full scope* of the claim, which according to Netlist includes a layout with *only* the "straight line" and no "fork in the road" whatsoever—a configuration entirely missing from the figures and written description of the 907 patent. *See, e.g.*, *ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1376–79 (Fed. Cir. 2009) (affirming lack of written description under § 112 where specification only disclosed a device with a "spike" but the claim tried to cover devices without a "spike"); *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1344–47 (Fed. Cir. 2005) (affirming lack of

> written description under § 112 where the claim tried to cover two embodiments but the specification only described one of them).

(*Id.* at 48-49.) Respondents add that the specification of U.S. Patent No. 8,417,870 (referred to as "the '131 Application") (RX-2389), which the '907 patent claims priority to, lacks written description for other limitations. (*Id.* at 50-51.)

In their reply brief, Respondents repeat an assertion from the Staff that the *Markman* order in this investigation (Order No. 17) somehow "only found support for [the straight line] construction in the claim language itself (amended in 2016), and not in the written description filed in 2009 (or even 2010) as required by § 112" for the "receive / do not . . . receive" limitation. (RRB at 34 (citing RIB at 47-48; SIB at 79-80).) With respect to the possible support provided by Figures 3A and 4A, Respondents contend:

> Figures 3A and 4A do not provide written description for two reasons: they both require buffer 416, which creates the "fork in the road," and they both teach that data sent to 412A is also received by 412C. *See* RPostHB at 13, 48–49. According to the patent, it is 412B and 412D (not 412C) that do not receive any data sent to 412A. *See id.* at 13. Netlist argues that the "chip select" signal prevents data from being ***written*** to 412C, *see* CPostHB at 73, but as repeatedly pointed out by the Staff, Netlist disclaimed the "chip select" signal and "writing" as sufficient to satisfy the claims, *see* SPostHB at 6, 29, 43, 79; RX-2437.00025 ("Netlist . . . is not seeking to construe 'output or receive' as 'perform the memory read or write command.'"). Instead, the claim construction ("acquire") depends on the ***internal*** operations of the memory devices, for which there is no written description. *See* RPostHB at 50.

(RRB at 34.) Respondents dispute that the knowledge of one skilled in the art can provide the missing description. (*Id.* at 35 (citing *Rivera*, 857 F.3d 1322).) Respondents conclude with "[h]ere, there is no disclosure in the patent whatsoever about the internal operations of the DRAM, as Netlist's experts have conceded" (*id.* (citing RIB at 50; RX-2006C at Q/A 165; Levitt, Tr. at 413:23-414:4; Baker, Tr. at 824:2-21)) and "[t]he inventors did not have in mind – and did not describe in their patent – data going to 412A but ***not*** being 'acquired' by 412C" (*id.*). Regarding

priority to the '131 Application, Respondents generally argue there is no disclosure therein for both address *and* control signals generated by a module controller, and Figure 3 of that application is a mere "schematic" which cannot function to disclose "physical location" of the buffers. (*See id.* at 35-36.)

The Staff appears to agree with Respondents in that "the disclosures of the '907 patent do not reasonably convey to a person of ordinary skill in the art that the inventor was in possession of the invention as claimed in the final issue '907 patent as construed (*i.e.* applied for the infringement analysis) in this investigation." (SIB at 78-79 (citing *Ariad Pharm.*, 598 F.3d at 1353-54).) As mentioned above, the Staff views the *Markman* order in this investigation (Order No. 17) as itself "discuss[ing] lack of written description support for the correlation of 'do not . . . receive' to known chip-select signals." (*Id.* at 79-80 (citing Order No. 17 at 25-27, 37-38).) The Staff also appears to condition a finding of adequate written description on obviousness in light of the Amidi reference. (*See id.* at 80; SRB at 21-22.) Apart from this limitation, the Staff appears to find adequate written support for the "produce" claim limitation (*see* SIB at 81) and the limitation regarding buffer circuit location (*id.* at 81-82.)

Netlist disputes a lack of written description and views Respondents as arguing "if that single structural element of one of multiple embodiments described in the specification of the '907 Patent—a buffer circuit that performs the selection of which memory devices should be read from or written to—is not included in the claims, they necessarily lack a sufficient written description." (CIB at 72 (citing CX-2727C at Q/A 91).) Netlist asserts this is opposite to the law which "start[s] with the claims and determin[es] whether the specification 'reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date'" which "can be satisfied by 'words, structures, figures, diagrams, formulas, etc.'" (*Id.* at 72-73 (citing

Ariad, 598 F.3d at 1351; *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997)).) Netlist continues, "[a] embodiment fully disclosed throughout the specification and figures is the 'straight line' configuration covered by the asserted claims." (*Id.* at 73 (citing CX-2727C at Q/A 95; '907 patent at Figs. 3A, 4A, 17:5-8; Subramanian, Tr. at 643:23-647:16).) In its reply brief, Netlist explains how Figure 4A in particular discloses first memory devices 412A and second memory devices 412C in a straight line configuration and argues Respondents' "red X" annotation of this figure (discussed above (*see* RIB at 48)) is a poor attempt to hide what is clearly disclosed (CRB at 50).

As for the claims' implication of internal workings of memory devices, Netlist argues that "there is no requirement to describe every detail of a feature or component that is already within the knowledge of a person of ordinary skill in the art." (CIB at 74 (citing *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005)).) Netlist observes that all experts "testified that a POSITA would know how to use the memory devices discussed in the '907 Patent and be familiar with the relevant JEDEC specifications for those devices." (*Id.* (citing Baker, Tr. at 825:15-826:10; Levitt, Tr. at 464:11-25, 465:13-466:13; RX-2006C at Q/A 50).) Regarding priority to the '131 Application, Netlist claims that application provides adequate written description for all asserted claims so as to enable the claim of priority. (*Id.* at 74-75 (discussing limitations [1b] and [1f]); *see* CRB at 52.)[10]

Here, the undersigned finds neither Respondents nor Staff have presented a clear and convincing case of lack of written description. To begin, Respondents' initial briefing barely even identifies which claim limitation supposedly lacks support. (*See* RIB at 47-48, 49-50 (discussing

[10] It is assumed that if Netlist's claim limitation numbering scheme is used here, it is actually limitation [1h] which recites "corresponding limitations." (*Compare* RIB at 51 *with* CIB at xx.)

issue in terms of "straight line" or "fork in the road" themes).) It is only in a paragraph on page 48 of Respondents' brief when data "being received (and acquired)" is mentioned (RIB at 48) that the undersigned can infer the limitation at issue is "receive / do not receive" as found in independent claim 1—designated by Netlist as limitation 1c (*see* CIB at xx).[11] Respondents' reply brief fortunately confirms this inference as it places its written description analysis under a heading of "a. 'receive / do not . . . receive.'" (RRB at 34.)

With this limitation in mind, it is the undersigned's view that Order No. 17 settled the issue. That order ultimately determined that the specification's discussion of chip-select signals (including the disclosures of the '386 and '537 patents incorporated by reference) matched the claims' use of "receive / do not receive" so as to make it proper to construe the term based on that known feature:

> The phrase "memory devices responding . . . by receiving" strongly indicates that "receiving" is something the memory devices do rather than a result of some other external act. (*See* CIMB at 28; CRMB at 18-20.) Netlist's chip-select explanation matches this language while Respondents' "fork in the road" interpretation does not. It is undisputed that the "fork in the road" effect is due to the action of buffer circuits, or data transmission circuits, *apart* from the memory devices. (*See* CIMB at 13-14; RIMB at 35-38.) I find here especially—the claims' own use of the term is highly instructive, perhaps the most instructive, piece of intrinsic evidence on the term's meaning. *Phillips*, 415 F.3d at 1314.
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> . . . .
>
> Each of [claims 2, 4, and 10] elaborates on the "first module control signals" introduced in claim 1 and which cause the first and second memory devices to "output or receive / do not output or receive" data. (*Id.* at cl. 1.) Notably, each of these claims focuses on chip-select signals which the '386 and '537 patents (incorporated by

[11] For example, following Order No. 17, it is the undersigned's view that the "straight line" or "fork in the road" dichotomy is more closely linked to the "configured to isolate memory device load" limitation (limitation 1f) than the "receive / do not receive" limitation (limitation 1c). (*See, e.g.*, Order No. 17 at 89-90 (discussing Respondents' "fork in the road" interpretation); 1023 ID at 124 (linking claim term "selective isolation" to "fork in the road").)

> reference into the '907 patent) teach are sent to the memory devices and the memory devices respond to—not the buffer circuits. (*See* '386 patent at Fig. 1A, 7:45-8:45; '537 patent at Fig. 9A, 16:59-18:3.) Respondents confirm the connection between the "first module control signals" (which controls the "output or receive / do not output or receive") and chip-select signals through their argument on the claim term "produce." (*See* RIMB at 25-29.)

(Order No. 17 and 27-28; *see id.* at 33-34 (further discussing '386 and '537 patents discussions of chip-select signals).)

Based on this reliance on the disclosures of chip-select signals in the '907 patent and the '386 and '537 patents incorporated therein on this very feature (*see* '907 patent at 10:39-45 ("The control circuit 430, 430' may produce additional chip-select signals or output enable signals based on address decoding. Examples of circuits which can serve as the control circuit 430, 430' are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein.")) in order to construe "receive / do not receive," the undersigned finds the argnment that the '907 patent lacks written description for the as-ordered construction of the term is not persuasive. Thus, the undersigned finds no clear and convincing evidence that the '907 patent does not comply with the written description requirement of 35 U.S.C. § 112.

With respect to Respondents' claim that the '131 Application does not provide adequate written description so as to support Netlist's claim of priority (RIB at 50-51), the undersigned does not understand the relevance of this issue. It does not appear that any party has asserted that the prior art status of those references Respondents and the Staff apply against the '907 patent turns on the '907 patent's effective date of invention. (*See* RIB at 50-51; RRB at 35-36; CIB at 74-75; CRB at 52; SIB at 15-16; *see generally* SRB.) The undersigned therefore finds it is not necessary to determine the question of whether the asserted claims of the '907 patent can properly claim priority to the filing date of the '131 Application.

VI. DOMESTIC INDUSTRY – ECONOMIC PRONG

Netlist argues that an economic domestic industry exists[12] as evidenced by its significant and substantial domestic investments directed to its HybriDIMM products[13], including [redacted] in plant and equipment, [redacted] in labor, and [redacted] in research and development. (CIB at 97 (citing CX-2006C at Q/A 24, 28, 72, 73-75).) According to Netlist, this amounts to [redacted] which is a tremendous amount for a company of its size. (*Id.* at 96.) Netlist submits that to determine its investment incurred specifically for the HybriDIMM products, it calculated the "HD Ratio," which "is a measure of the percentage of Netlist's overall R&D investments in HybriDIMM as compared to its overall R&D investments."[14] (*Id.* at 97 (citing CX-2006C at Q/A 30-31, 43-69, 76).) Netlist therefore argues that using the "HD Ratio," it invested over [redacted] of its total engineering expenses in HybriDIMM in 2015, nearly [redacted] in 2016, and [redacted] for January 2017 to August 2017. (*Id.*)

Netlist submits that it first publicly demonstrated the HybriDIMM in August 2016 and has since conducted numerous public and private demonstrations. (*Id.* at 96 (citing CX-2001C at Q/A 129-133).) Netlist further submits that it [redacted]

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12 Netlist does not argue that a domestic industry "is in the process of being established." (*See* CIB at 94-102; CRB at 68-71.)

13 While Netlist contends that it started to focus development efforts on the ASIC version of the HybriDIMM product in 2017, it represented that it is not relying on that version to satisfy the domestic industry requirement. (*See* CIB at 96 n.11; RX-3810C at *12 ("Netlist is solely relying on the FPGA version to satisfy the domestic industry requirement").) Therefore, the undersigned considers Netlist's investments with respect to its FPGA HybriDIMM products and references to "HybriDIMM" herein refer to those FPGA HybriDIMM products.

14 Netlist claims that "[t]he HD Ratio also allocates the salaries of employees in the U.S. who directly and materially support Netlist's efforts in developing and commercializing HybriDIMM." (*Id.* (citing CX-2006C at Q67-69).)

[redacted] (*Id.* (citing CX-2001C at Q/A 132-33).) Netlist therefore asserts that the HybriDIMM is "commercially viable." (*Id.*) Netlist argues that contrary to Respondents' position, there is no requirement that a domestic industry article be commercialized and that "the Commission has expressly held that non-commercial articles can provide the basis for a domestic industry." (CRB at 68-69 (citing *Certain Non-Volatile Memory Devices and Products Containing the Same*, Inv. No. 337-TA-1046, Comm'n Op. at 41 (Oct. 26, 2018); *Certain Computers and Computer Peripheral Devices, and Components Thereof and Products Containing Same*, Inv. No. 337-TA-841, Comm'n Op. at 40 n.30 (Jan. 9, 2014)).)

Respondents argue that Netlist's HybriDIMM product [redacted] (RIB at 84 (citing RX-3871C at Q/A 59-68).) Respondents further argue that Netlist [redacted] (*Id.* (citing RX-3871C at Q/A 60; JX-2008C at 60:4-61:11; RX-2197 at *8; JX-2012C at 17:22-18:25).) Respondents therefore submit that by the end of 2016, [redacted] (*Id.* at 84-85 (citing JX-2013C at 14:1-15:6, 20:15-21:15; Whitley, Tr. at 221:6-17; RX-3871C at Q/A 48-50, 62).)

According to Respondents, at the end of 2017, [redacted] (*Id.* at 85 (citing Sasaki, Tr. at 240:20-244:22).) Respondents claim that Netlist has [redacted] (*Id.* (citing Hong, Tr. at 177:4-14; 284:19-285:11; RX-3871C at Q/A 64; JX-2017C at 35:6-37:21).) For example, Respondents

assert that at the evidentiary hearing in the 1023 Investigation, Netlist's CEO testified that its [redacted] (*Id.* at 85-86 (citing RX-3772C at Q/A 137; RX-3771C at Q/A 32; JX-0030C at 115:1-3).) Respondents, however, contend that [redacted] (*Id.* at 86 (citing Hong, Tr. at 179:6-185:9; RX-3775C at *9; RX-3776C at *3).) Thus, Respondents argue that the HybriDIMM product is not [redacted] (*Id.*)

Respondents also argue that Netlist's economic prong evidence terminates in May 2017 and therefore it cannot show that its purported domestic industry for the HybriDIMM was in existence as of the filing date of the complaint. (RRB at 57.) Respondents claim that [redacted] (*Id.* at 58 (citing RX-3871C at Q/A 64; JX-2017C at 35:6-37:21; JX-2014C at 20:23-23:16).) Respondents further contend that Staff's position is not supported by the case law cited by Staff because the conditions for finding a domestic industry in those cases are missing here. (*Id.* at 59-60 (citing SIB at 99).)

Staff submits that from 2014 to August 2016, the evidence shows a domestic industry. (SIB at 96; SRB at 27.) Staff asserts that as early as May 2017, engineers were splitting time between the FPGA version of the HybriDIMM product and other versions. (SIB at 96 n.58 (citing Milton, Tr. at 297:18-23).) Staff also asserts that Netlist's specific work on the LRDIMM portion of the FPGA version of the HybriDIMM was completed by August 2016. (*Id.* at 97 (citing CX-2001C at Q/A 131-32; CX-2005C at Q/A 8, 11; RX-3871C at Q/A 43, 49).) Staff therefore argues that considering the time period from January 2014 to August 2016, the evidence shows that Netlist

satisfies the economic prong of the domestic industry requirement under all three subsections. (*Id.* at 98.)

Staff disagrees with Respondents' argument regarding commercialization even though the evidence shows that [redacted] (*Id.* (citing *Certain Non-Volatile Memory Devices and Products Containing the Same*, Inv. No. 337-TA-1046, Comm'n Op. at 41-42 (Oct. 26, 2018)).) Staff also argues that even though Netlist completed work on the LRDIMM portion of the HybriDIMM before the filing of the complaint, the Commission has previously determined that a domestic industry can be found based on past activities and has rejected the argument that investments in a discontinued product cannot form the basis for an existing domestic industry. (*Id.* at 98-99 (citing *Certain Electronic Digital Media Devices and Components Thereof*, Inv. No. 337-TA-796, Comm'n Op. at 99-102 (Sept. 6, 2013); *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Comm'n Op. at 25 (Sept. 23, 1996)).) Lastly, Staff contends that Respondents' nexus argument should be rejected because "[w]hile the evidence does not show that the HybriDIMM product practices claims of either of the Asserted Patents, to the extent it is found otherwise, the evidence shows that the HybriDIMM embodies the inventions of the Asserted Patents (*i.e.* JEDEC Standard Compliant DDR4 LRDIMM)." (*Id.* at 99.)

As an initial matter, Respondents fail to present compelling argument or legal authority to conclude that commercial availability of a patented article in the United States is required to show that a domestic industry exists. For example, in *Certain Non-Volatile Memory Devices*, the Commission stated that the term "article" in section 337(a)(2) "is sufficiently capacious to embrace pre-commercial or non-commercial items." *Certain Non-Volatile Memory Devices*, Inv. No. 337-TA-1046, Comm'n Op. at 41 (Oct. 26, 2018). Similarly, in *Certain Road Construction Machines*,

the administrative law judge determined, and the Commission did not review, that there was no requirement that articles be commercialized to satisfy the domestic industry requirement. *See Certain Road Construction Machines and Components Thereof*, Inv. No. 337-TA-1088, Initial Determination at 71-79 (Feb. 14, 2019); *Certain Road Construction Machines*, Notice of Comm'n Determination to Review-in-Part a Final Initial Determination at 2 (Apr. 12, 2019).

In this Investigation, the evidence shows that the HybriDIMM product is complete and [redacted] (CX-2001C at Q/A 132; CX-2006C at Q/A 26.) Additionally, the evidence shows that Netlist [redacted] (CX-2001C at Q/A 132.) However, even if Netlist [redacted] as Respondents allege, the undersigned finds no requirement for the HybriDIMM to be commercialized in order to satisfy the domestic industry requirement. Accordingly, the undersigned finds that the HybriDIMM product is an article subject to an existing domestic industry.

As to the relevant time period, subsections 337(a)(3)(A) and (B) "concern investments in plant and equipment and labor and capital 'with respect to the *articles* protected by the patent.'" *Certain Ground Fault Circuit Interrupters and Products Containing Same*, Inv. No. 337-TA-739, Comm'n Op. at 78 (Jun. 8, 2012) (emphasis in original) (citing 19 U.S.C. §§ 1337(a)(3)(A), (B); *Certain Unified Communications Systems, Products Used With Such Systems, & Components Thereof*, Inv. No. 337-TA-598, Order No. 9 (Sept. 5, 2007)). In contrast, the phrase "investment in its exploitation" in subsection 337(a)(3)(C) refers to the asserted patent or other intellectual property right being asserted and requires the complainant to establish a nexus between the asserted patent and the U.S. investment in its exploitation. *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 36-38 (Aug. 22, 2014).

The evidence shows that Netlist began investing in engineers dedicated to working on HybriDIMM in 2014. (CX-2006C at Q/A 24, 28; CX-2312C at *138.) Netlist asserts that the LRDIMM portion of the HybriDIMM product is the portion that practices the Asserted Patents and the evidence shows that Netlist's specific work on the LRDIMM portion was completed by August 2016. (*See* CIB at 54, 93, 95; CRB at 29-30, 65-66; CX-2005C at Q/A 11; RX-3871C at Q/A 43; CX-2001C at Q/A 131; RX-3772C at Q/A 131.) According to Netlist's vice president of engineering, the work on the FPGA HybriDIMM was completed around August 2017. (JX-2013C at *9-10.) Accordingly, as to subsections 337(a)(3)(A) and (B), Netlist's relevant investments in the HybriDIMM (*i.e.*, the article) would be from 2014 to August 2017. As to subsection 337(a)(3)(C), however, Netlist's relevant investments would be from 2014 to August 2016 when investments were made with respect to the LRDIMM portion of the HybriDIMM, which allegedly was the portion that practices the Asserted Patents.

Additionally, the undersigned finds Respondents' argument that Netlist cannot show a domestic industry at the time the complaint was filed unpersuasive. The Commission has stated that "a domestic industry can be found based on complainant's past activities in exploiting the [asserted] patent." *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Comm'n Op. at 25 (Sept. 23, 1996) (emphasis in original) (noting that it had only been several months since the complainant was exploiting the asserted patent). Additionally, the Commission has previously rejected the argument that investments in a discontinued product cannot form the basis of an existing domestic industry. *Certain Electronic Digital Media Devices and Components Thereof*, Inv. No. 337-TA-796, Comm'n Op. at 99-102 (Sept. 6, 2013).

Here, the evidence shows Netlist's investments in HybriDIMM from 2014 to August 2017, when work on HybriDIMM was completed. (*See* CX-2006C; JX-2013C at *9-10; RX-3871C at

Q/A 49.) In addition, the evidence shows that at least as of 2018, Netlist was in the process of demonstrating HybriDIMM, negotiating purchase orders for HybriDIMM, and manufacturing HybriDIMM. (*See* CX-2001C at Q/A 131-132, 176.) Therefore, because the complaint was filed only a few months after Netlist completed work on the HybriDIMM, Netlist made significant investments in HybriDIMM (as discussed below), and because the evidence shows that Netlist continued to invest, albeit more modestly than before, in the HybriDIMM after August 2017, Netlist's investments in the HybriDIMM satisfy the existence of a domestic industry. *See Certain Variable Speed Wind Turbines*, Comm'n Op. at 25; *Certain Electronic Digital Media Devices*, Comm'n Op. at 99-102.

A. 337(a)(3)(A) – Significant Investment in Plant and Equipment

Netlist contends that it has made significant investments in plant and equipment within the U.S. in direct connection with its HybriDIMM products. (CIB at 99.) Netlist asserts that between January 2014 and the filing of the complaint in this Investigation, it used an average of [redacted] square feet in connection with its HybriDIMM products, invested a total of [redacted] in facility costs, and invested [redacted] in equipment. (Id. (citing CX-2006C at Q/A 70-72).) Netlist claims that since November 2013, its California headquarters comprised at least 8,203 square feet and the vast majority of research and development for the HybriDIMM products occurred in that facility. (Id. at 99-100 (citing CX-2006C at Q/A 13, 71).)

Netlist calculated the allocation of investments in its domestic facilities by taking the number of HybriDIMM engineers and dividing it by the total headcount of U.S. employees ("Headcount Percentage"). (*Id.* at 100 (citing CX-2006C at Q/A 30, 70-72).) Netlist claims that from 2014 through August 2017, the annual Headcount Percentages for its HybriDIMM products were [redacted] (*Id.* (citing CX-2006C at Q/A 72).) Netlist explains that

these Headcount Percentages are less than the HD Ratios because they are compared to its total employees, not just its research and development employees. (*Id.* at 100 n.13.) Therefore, Netlist claims that using these percentages, it invested [redacted] in domestic facility costs, including lease payments, property taxes, general insurance, utilities, and repairs and maintenance. (*Id.* at 100 (citing CX-2006C at Q/A 72).) With respect to square footage, Netlist claims that it dedicated an average of [redacted] of its total square footage, *i.e.*, [redacted] square feet, to HybriDIMM. (*Id.* (citing CX-2006C at Q/A 72).) Netlist submits that this "is a very significant investment, both from a quantitative and qualitative perspective." (*Id.*)

Netlist also contends that it incurred annual domestic costs related to equipment used in domestic activities related to HybriDIMM, including "investments in laptops for engineers, servers, microscopes, development boards, test platforms, CPUs, motherboards, flash testers, and other equipment used with HybriDIMM by Netlist engineers." (*Id.* at 100-101 (citing CX-2006C at Q/A 73; CPX-2005C).) Netlist asserts that between 2014 and the end of August 2017, it spent [redacted] in equipment costs, and over this time using the HD Ratio, it incurred [redacted] in capital equipment costs attributable to HybriDIMM, which it claims is "clearly a significant expense." (*Id.* at 101 (citing CX-2006C at Q/A 73; CPX-2005C).)

Netlist contends that even if investments during 2017 were ignored entirely, it still invested [redacted] in facility expenses ([redacted]) directly attributable to HybriDIMM. (CRB at 70 (citing CX-2006C at Q/A 70-72; CDX-2006C.004).) Similarly, Netlist contends that from 2014 to 2016, it invested [redacted] for HybriDIMM-related equipment investments. (*Id.* (citing CX-2006C at Q/A 73-74; CDX-2006C.005).)

Staff[15] agrees with Netlist that it has made significant investments in plant and equipment in the United States with respect to the HybriDIMM. (SIB at 100.) Staff claims that Netlist's facilities are located in Irvine, California where the research and development of the HybriDIMM occurred, including [redacted] (*Id.*) Staff also claims that Netlist made investments in equipment employed in the research and development of the HybriDIMM at its facilities in Irvine, including [redacted] expenses relating to the HybriDIMM are significant, both quantitatively and qualitatively, based on the modest size of Netlist as a company and the relative importance of the FPGA version of HybriDIMM to Netlist's business. (*Id.* (citing CX-2001C at Q/A 51-54; 60-61, 147; CX-2006C at Q/A 23-24, 71-73; 1023 ID at 155).)

Based on the evidence presented, the undersigned finds that Netlist has shown that it satisfies the economic prong of the domestic industry requirement based on significant investments in plant and equipment.[16] The evidence shows that from 2014 to August 2017, Netlist invested [redacted] in facilities costs in connection with the HybriDIMM product, which includes lease payments, property taxes, general insurance, utilities, and repairs and maintenance. (CX-2006C at Q/A 72; CX-2312C at 140.) The evidence also shows that from 2014 to August 2017, Netlist

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15 Respondents do not present arguments specifically addressing plant and equipment investments for the HybriDIMM product. (*See* RIB at 83-94; RRB at 56-60.)

16 Contrary to Netlist's assertion (*see* CRB at 71), the undersigned finds that in this case, Netlist's investments made in connection with R&D activities cannot be placed in the labor or capital and plant and equipment categories. In outlining Netlist's investments in R&D, Netlist's own witness states that it "made expenditures related to R&D of HybriDIMM *other than in labor, facilities, and equipment.*" (CX-2006C at Q/A 74 (emphasis added).) Therefore, it would not be appropriate to include these expenditures in subsections 337(a)(3)(A) or (B).

invested at least [redacted][17] in capital and equipment costs attributable to HybriDIMM engineering. (CX-2006C at Q/A 73; CX-2312C at 142.) This amounts to a total investment in plant and equipment of [redacted] from 2014 to August 2017 related to HybriDIMM. The undersigned agrees with Netlist and Staff that those investments are significant within the meaning of section 337(a)(3)(A) based on Netlist's modest size as a company and the relative importance of the HybriDIMM product to Netlist's overall business.[18] (*See* CX-2006C at Q/A 24, 72-73; *see also* SIB at 98 n.60; *Certain Printing and Imaging Devices and Components Thereof*, Inv. No. 337-TA-690, Comm'n Op. at 27 (Feb. 17, 2011) (citing *Certain Stringed Musical Instruments*, Inv. No. 337-TA-586, Comm'n Op. at 26 (May 16, 2008)).) Accordingly, the undersigned finds that Netlist has made significant investments in plant and equipment with respect to HybriDIMM, and thus, has satisfied the economic prong of the domestic industry requirement for the Asserted Patents pursuant to subsection 337(a)(3)(A).

B. 337(a)(3)(B) – Significant Employment of Labor or Capital

Netlist contends that between January 2014 and the filing of the complaint, it "invested at least [redacted] in labor for individuals working directly on FPGA HybriDIMM R&D, or providing necessary support to that effort." (CIB at 97 (citing CX-2006C at Q/A 24); CX-2312C at *138.) Netlist explains that it categorizes employees as working on specific projects or products, tracked by department code. (*Id.* at 97-98 (citing JX-2031C at *160; CX-2006C at Q/A 29-30).)

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[17] The undersigned notes that while Ms. Sasaki testified that this amount was [redacted] the exhibit cited in her testimony shows the amount to be [redacted] (*Compare* CX-2006C at Q/A 73, *with* CX-2312C at 142.)

[18] In addition, even if viewed conservatively and the investments made in 2017 are disregarded, Netlist still made significant investments in plant and equipment amounting to [redacted] (*i.e.*, [redacted] in facilities costs and [redacted] in capital and equipment costs) from [redacted] (*See* CX-2006C at Q/A 72; CX-2312C at 142.)

Netlist claims that it hires engineers specifically to work on certain products and once hired, typically work only on that product while at Netlist. (*Id.* at 98 (citing CX-2006C at Q/A 29-30).) Netlist therefore asserts that "engineers assigned to HybriDIMM in the U.S. prior to the filing of the complaint spent virtually all of their time working on the FPGA HybriDIMM." (*Id.* (citing CX-2006C at Q/A 30-31, 44-66).)

According to Netlist, around the time of filing the complaint, it employed [redacted] in the U.S. (29 at Netlist's headquarters in Irvine) and [redacted] of those employees were engineers dedicated to working on the FPGA version of HybriDIMM. (*Id.* (citing CX-2006C at Q/A 16, 65).) Netlist contends that since 2014, it employed [redacted] people in the U.S. ([redacted]). (*Id.* (citing CX-2006C at Q/A 16).) Netlist argues that its "development of HybriDIMM in the U.S. reflects a 'massive undertaking' of its engineers." (*Id.* (citing CX-2001C at Q/A 78-99; CX-2006C at Q/A 43-66; CX-2005C at Q/A 17-26).)

Netlist submits that its engineers began work on HybriDIMM in [redacted] and once operational, Netlist prototyped it during the summer of [redacted] and worked over at least the subsequent year to refine the design. (*Id.* (citing JX-2031C at *160-165, 171-172; CX-2006C at Q/A 23).) Netlist argues that from [redacted] to the filing of the complaint in the fall of 2017, it invested [redacted] in U.S. engineering salaries, including benefits for engineering dedicated to HybriDIMM.[19] (*Id.* at 98-99 (citing CX-2006C at Q/A 31-42, 51-52; CPX-2005C).) In addition, Netlist argues that it invested [redacted] in salaries allocable to HybriDIMM for U.S. operations and management. (*Id.* at 99 (citing CX-2006C at Q/A 68-69, 75; CPX-2005C).)

[19] Netlist claims that this includes [redacted] and at least [redacted] (*Id.* at 99.) Netlist also claims that this does not include [redacted] that it invested in 2013 when it started work on HybriDIMM and thus, its actual investment is "materially understated." (*Id.* at 98 n.12 (citing CX-2006C at Q42, 75).)

Based on this evidence, Netlist asserts that its domestic labor investment with respect to HybriDIMM between January 2014 and the filing of the complaint is objectively, quantitatively, and qualitatively significant. (*Id.*) Netlist argues that "[w]ithout the domestic labor R&D dedicated to HybriDIMM, it would not exist" and "[e]vidence of this type of R&D focus consistently supports a finding of qualitative significance." (*Id.* (citing CX-2001C at Q/A 77-97; *Handheld Electronic Computing Devices*, Inv. No. 337-TA-769, Initial Determination, Order No. 34 at 8 (Feb. 6, 2012) (unreviewed)).) Netlist therefore contends that it has invested significant sums in labor related to the FPGA-based HybriDIMM and "[f]or a company of its size, this investment is quantitatively and qualitatively gigantic." (*Id.* at 99.)

In addition, Netlist argues that only two engineers, Jerry Alston and Jordan Horwich, worked on the ASIC version of the product prior to August 2017. (CRB at 69.) Netlist submits that Mr. Alston was hired in late May 2017 and Mr. Horwich was hired in late June or July 2017, and therefore "to the extent their salaries may have been included in the [redacted] labor investment total for 2017, that total–at most–included four months of Mr. Alston's salary and just two to three months of Mr. Horwich's salary." (*Id.* (citing RX-4223C; JX-2009C at 10:7-10, 11:10-12:22; Sasaki, Tr. at 255:4-8).) Therefore, based on Mr. Alston's annualized salary in 2017 of [redacted] and Mr. Horwich's annualized salary in 2017 of [redacted] Netlist argues that at most, the 2017 labor number was overstated by [redacted] which is four months of Alston salary + [redacted] which is three month of Horwich salary). (*Id.* at 69-70 (citing CPX-2005C).) According to Netlist, "[t]his still leaves well over [redacted] in 2017 labor investment directed solely to the FPGA HybriDIMM." (*Id.* at 70.) Moreover, Netlist contends that even if investments during 2017 were ignored entirely, it still invested in domestic engineering labor for HybriDIMM [redacted]

[redacted] (*Id.* (citing CX-2006C at Q/A 39-42; CDX-2006C.003).)

Respondents assert that Netlist's pre-complaint allocation is defective because Netlist's engineers have been [redacted] (RIB at 86-87 (citing JX-2013C at 14:1-15:6; Hong, Tr. at 177:18-178:20, 297:14-23).) Respondents therefore contend that Netlist's pre-complaint expenditures included the ASIC version and Netlist therefore "failed to carve that (non-DI) portion out of its claimed economic prong evidence." (*Id.* at 87; *see* RRB at 56-57.)

Staff submits that Netlist has made significant employment of engineering labor in the United States with respect to HybriDIMM, including [redacted] (SIB at 100 (citing CX-2006C at Q/A 24, 39-41).) In addition, Staff claims that Netlist's investments in labor relating to the research and development of the HybriDIMM are also significant, both quantitatively and qualitatively, based on Netlist's modest size as a company and the relative importance of HybriDIMM to Netlist's business. (*Id.* at 100-01 (citing CX-2001C at Q/A 51-54, 60-61, 147; CX-2006C at Q/A 23-24, 68-69; 1023 ID at 159).)

Based on the evidence presented, the undersigned finds that Netlist has shown that it satisfies the economic prong of the domestic industry requirement based on significant employment of labor or capital. Specifically, the evidence shows that Netlist spent [redacted][20] in engineering labor from 2014 to August 2017, most of which was related to HybriDIMM. (CX-2006C at Q/A 39-42.) However, the evidence also shows that two of Netlist's engineers, Jerry Alston (hired in May 2017) and Jordan Horwich (hired in June/July 2017), worked on the ASIC

[20] While Ms. Sasaki testified that the total investment from 2014 to August 2017 was [redacted], it appears that the total, based on the dollar amounts for each individual year, is actually [redacted] (*See* CX-2006C at Q/A 42.)

version of the product prior to August 2017. (*See* RX-4223C; JX-2009C at 10:7-10; Sasaki, Tr. at 254:23-255:10, 297:18-23.) Mr. Alston's annualized salary in 2017 was [redacted] and Mr. Horwich's annualized salary in 2017 was [redacted] (CPX-2005C at Tab "Annual 2015-16-17 US Salaries".) Therefore, Netlist's investment in engineering labor from 2014 to August 2017 appears to have been overstated by about [redacted] (*i.e.*, [redacted] which is four months of Mr. Alston's annual salary + [redacted] which is three month of Mr. Horwich's annual salary), which accounts for the salaries of Mr. Alston and Mr. Horwich when they were working on the ASIC version and not solely the FPGA version of HybriDIMM. Accordingly, the undersigned finds that Netlist's investment in labor and capital from 2014 to August 2017 for HybriDIMM was [redacted]. The undersigned finds that these investments are significant, based both on the relatively modest size of Netlist as a company, and based on the importance of HybriDIMM to Netlist's business.[21] (*See* CX-2006C at Q/A 24, 72-73; *see also* SIB at 98 n.60; *Certain Printing and Imaging Devices*, Comm'n Op. at 27 (citing *Certain Stringed Musical Instruments*, Comm'n Op. at 26).) Therefore, the undersigned finds that Netlist has satisfied the economic prong of the domestic industry requirement for the Asserted Patents pursuant to subsection 337(a)(3)(B).

C. 337(a)(3)(C) – Substantial Investment in its Exploitation

Netlist argues that it has made substantial domestic expenditures related to R&D and engineering of HybriDIMM, including tooling, testing fees, software maintenance fees, office supplies, telephone fees, engineering education and training, subscription fees, travel expenses, and some outside testing services. (CIB at 101 (citing CX-2006C at Q/A 74; CPX-2005C).) Netlist submits that since 2014, it incurred [redacted] in research and development and

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[21] In addition, even if viewed conservatively and the investments made in 2017 are disregarded, Netlist still made significant investments in labor or capital amounting to [redacted] from 2014 to 2016. (*See* CX-2006C at Q39-41.)

engineering expenditures directly related to HybriDIMM, including at least [redacted] in 2014, [redacted] in 2015, [redacted] in 2016, and [redacted] from January 2017 to August 2017. (*Id.* (citing CX-2006C at Q/A 74-75; CPX-2005C).) Netlist asserts that "[t]hese investments are qualitatively and quantitatively substantial for a company of Netlist's size." (*Id.* (citing CX-2006C at Q/A 24).) Moreover, Netlist argues that similar amounts from companies of varying sizes, including companies larger than Netlist, constituted substantial investments. (*Id.* at 101-102 (citing *Certain Electronic Devices, Including Wireless Communication Devices, Portable Music and Data Processing Devices, and Computers*, Inv. No. 337-TA-794, Comm'n Op. at 102, 104-05 (July 5, 2013); *Certain Table Saws Incorporating Active Injury Mitigation Technology and Components Thereof*, Inv. No. 337-TA-965, Initial Determination, Order No. 10 at 16-17 (Mar. 22, 2016)).) Netlist contends that when taken in the aggregate, and particularly when viewed in relation to its overall domestic investments, Netlist's total investments in HybriDIMM are significant. (*Id.* at 102.) According to Netlist, its total investment of [redacted] in HybriDIMM over the three years preceding the filing of the complaint makes up [redacted] of its total company-wide investments during that time and approximately [redacted] of its overall company-wide R&D expenses during that time. (*Id.* (citing CX-2006C at Q/A 24).)

Netlist further submits that to the extent that investments in 2017 are not taken into account, it invested [redacted] in research and development from 2014 to 2016. (CRB at 70 (citing CX-2006C at Q/A 74; CDX-2006C.006).) With respect to showing a nexus between its R&D work and the claims of the Asserted Patents, Netlist argues that showing such a nexus is not necessary for subsections 337(a)(3)(A) and (B), but does not specifically address a nexus for subsection 337(a)(3)(C). (*Id.* at 71.)

Respondents contend that Netlist has failed to show a nexus between its alleged engineering, research, and development expenditures and the asserted claims. (RIB at 88 (citing *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 38 (Aug. 22, 2014); RX-3871C at Q/A 86-90.) Respondents claim that Netlist relies on the LRDIMM portion of the HybriDIMM for purposes of the technical prong of the domestic industry requirement, which was "finalized and fully functional since August 2016." (*Id.* (citing RX-3772C at Q/A 130-31; RX-3770C at Q/A 35-37; JX-2033C at 286:1-22; JX-2013C at 56:2-12, 57:17-58:12; RX-3871C at Q/A 43-45; Milton, Tr. at 285:23-288:3; RX-2277C).)

Staff submits that Netlist has made substantial investment in engineering and research and development in the United States with respect to the HybriDIMM, including [redacted] in 2014, [redacted] in 2015, and [redacted] in 2016. (SIB at 101 (citing CX-2006C at Q/A 74).) According to Staff, "when considering the time period ending in 2016 (pre-ASIC), the evidence shows a nexus between the asserted patents and Netlist's investments in their exploitation through engineering and research and development of the FPGA version of the HybriDIMM." (*Id.*) Staff also contends that these investments are significant quantitatively and qualitatively based on Netlist's modest size as a company and the relative importance of the HybriDIMM to Netlist's business. (*Id.* (citing CX-2001C at Q/A 51-54, 60-61, 147; CX-2006C at Q/A 23-24; 1023 ID at 163).)

In order to establish a domestic industry under section 337(a)(3)(C), Netlist must establish investments in research and development for the domestic industry products and show a nexus between the asserted patents and the U.S. investment in their exploitation. *Certain Integrated Circuit Chips and Products Containing the Same*, Inv. No. 337-TA-859, Comm'n Op. at 38 (Aug. 22, 2014). The Commission has explained that "this nexus may readily be inferred based on evidence that the

claimed investment is in the domestic industry article, which itself is the physical embodiment of the asserted patent." *Id.* at 40. Further, the Commission has explained that "no patent-by-patent allocation is required for research and development investment under subparagraph (C)." *Id.* at 41. The Commission reasoned that such an approach would risk "freezing cognizable investment at the point at which the patented technology is reduced to practice," and would run contrary to the reality that "most firms have little reason to keep research and development records on a patent-by-patent basis, as opposed to a project-by-project basis (to the extent that project-by-project records are kept)." *Id.* at 41-42.

Consistent with the above determination that the HybriDIMM products satisfy the technical prong of the domestic industry requirement for the '907 patent and the evidence of record showing Netlist's investment in domestic research and development related to the HybriDIMM, the undersigned finds that Netlist has established a nexus between its research and development activities and the '907 patent based on the patented articles themselves, *i.e.*, the HybriDIMM products. (*See* CX-2006C at Q/A 74; *Certain Integrated Circuit Chips*, Comm'n Op. at 40.) Specifically, the evidence shows that from 2014 to 2016, Netlist invested [redacted] in domestic research and development. (CX-2006C at Q/A 74; CX-2312C at 144.) As previously stated though, Netlist's relevant investments with respect to subsection 337(a)(3)(C) would be from 2014 to August 2016 when investments were made with respect to the LRDIMM portion of the HybriDIMM. Although Netlist presents evidence of investments for the full year 2016 instead of from January 2016 to August 2016, if viewed conservatively and the undersigned disregards investments made in 2016, Netlist still made substantial investments in research and development amounting to [redacted] from 2014 to 2015. (*See id.*) The undersigned finds that these investments are substantial, based both on the relatively modest size of Netlist as a company, and

based on the importance of HybriDIMM to Netlist's business. (*See* CX-2006C at Q/A 24, 72-73; *see also* SIB at 98 n.60; *Certain Printing and Imaging Devices*, Comm'n Op. at 27 (citing *Certain Stringed Musical Instruments*, Comm'n Op. at 26).) Accordingly, the undersigned finds that Netlist has satisfied the economic prong of the domestic industry requirement for the '907 patent pursuant to subsection 337(a)(3)(C).

However, as determined above, Netlist has not shown that the HybriDIMM products satisfy the technical prong of the domestic industry requirement as to the '623 patent. Accordingly, because the undersigned has determined that the HybriDIMM products do not practice the '623 patent, Netlist cannot make an articles-based nexus showing between its research and development activities and the '623 patent based on its HybriDIMM products. Netlist did not provide any other reasons for finding a nexus between its research and development investments and the '623 patent. (*See* CIB at 94-102; CRB at 68-71.) Therefore, the undersigned finds that Netlist fails to satisfy the economic prong of the domestic industry requirement for the '623 patent pursuant to subsection 337(a)(3)(C).

In sum, the undersigned finds the economic prong of domestic industry has been satisfied under subsections (A), (B), and (C) for the '907 patent, and satisfied under subsections (A) and (B) for the '623 patent.

VII. OTHER AFFIRMATIVE DEFENSES

A. Equitable Estoppel, Waiver, and Implied License

In their initial post-hearing brief, Respondents argue "the same facts that show the public interest precludes an exclusion order in light of Netlist's violation of its RAND commitments, Netlist's claims are barred by the doctrine of equitable estoppel." (RIB at 90.) Indeed, as suggested, this defense is predicated on a finding that Netlist has failed to offer a license to the

asserted patents on RAND terms as required of JEDEC participants. (*See id.* at 90-91.) Respondents tie their waiver and implied license defenses to the same predicate. (*Id.* at 91 n.22.)

As discussed below, the undersigned finds the evidence does not show Netlist has breached a RAND obligation. Thus, this affirmative defense fails, as it did in the 1023 Investigation. (*See* 1023 ID at 197 n.41.)

B. Unclean Hands

Apart from RAND issues, Respondents also contend that "blatantly false statements that Netlist has made in support of its domestic industry allegations in this and the 1023 Investigation leave it with unclean hands" such that it "should be entitled to no relief in this Investigation and barred from bringing further actions against SK hynix." (RIB at 91, 94.) Respondents note the relevant considerations are whether: "(1) the accused party has committed an 'unconscionable act'; and (2), the misconduct 'has an immediate and necessary relation to the equity that the requesting party seeks in respect of the matter in litigation.'" (*Id.* at 91 (citing *Aptix*, 269 F.3d at 1376; *Keystone Driller*, 290 U.S. at 245).)

As to unconscionable act, Respondents point to the 1023 Investigation where [redacted] (*id.* at 91-92 (citing RX-3770C at Q/A 20; RX-3771C at Q/A 32; RX-3772 at Q/A 37)) and Netlist itself "represented that it [redacted] (RX-3773C.00084) to counter SK hynix's contention that [redacted] . . . ." (*id.* at 92). Respondents also point to this investigation where Netlist's Ground Rule 7-3 disclosures contended [redacted]

[redacted] (*id.* (citing RX-3843 at ¶ 15)) and its witness testified to the same (*id.* (citing CX-2001C at Q/A 54, 133, 139, 141)).

Respondents allege Netlist made these representations even though it "[redacted]" (*Id.* at 92-93 (citing Hong, Tr. at 168:9-178:20; Sasaki, Tr. at 250:14-251:9; JX-2013C at 9:20-10:3, 14:6-11; JX-2008C at 24:21-25:17, 32:17-33:15, 55:22-56:5, 61:1-7; JX-2013C at 14:6-11, 32:12-14, 68:6-12).) Respondents add:

> The falsity of Netlist's representations to the Commission regarding [redacted] RX-3775C.00003; RX-3776C.00003; Hong, Tr. at 182:6-184:21; RX-3771C at Q/A 32.23 [redacted] JX-2008C at 24:21-25:17, 32:17-33:15, 55:22-56:5, 61:1-7; JX-2013C at 14:6-11, 32:12-14, 68:6-12; Hong, Tr. at 168:9-12, 173:3-23, 176:22-178:20; Sasaki, Tr. at 250:14-251:9. [redacted] JX-2013C at 68:6-12; Hong, Tr. at 178:3-20. Thus no version of HybriDIMM constitutes a domestic industry today, despite Netlist's misrepresentations to the contrary

(*Id.* at 93.) Respondents assert that the necessary relation" factor is met by "Netlist sought—and gained—an unfair advantage by [redacted] (*Id.* at 94 (citations omitted).)

In their reply brief, Respondents contend "Netlist side-steps the core of Respondents' arguments" because [redacted] are irrelevant to the fact of

what Netlist told the Commission in the 1023 Investigation [redacted] (*See* RRB at 60.) Respondents add:

[redacted] JX-2017C (2018.08.16 Gail Sasaki Dep. Tr.) at 27:12-19.

(*Id.* at 60-61.)

Respondents claim similar statements on the status of FPGA HybriDIMM made in this investigation lack candor and are demonstrably false. (*Id.* at 61.) For example, Respondents state "[i]n this Investigation, Netlist would have the CALJ believe that "Netlist intended—and still intends—to sell [FPGA HybriDIMM] to customers." (*Id.* at 63 (comparing CIB at 105 with JX-2013C at 14:6-11, 8:22-9:12, 9:24-10:3; citing RX-2325C at *14; JX-2014C at 20:23-23:16).) For another example, Respondents state "Netlist represents that he FPGA HybriDIMM 'was fully functional and ready for distribution to customers as early as [redacted] (*Id.* at 64 (comparing CIB at 96 n.11 with RX-2074C at *76-77; citing JX-2007C at 26:1-31:14, 35:5-9, 36:17-41:19; RX-2183C at *12; RX-2188C; RX-2189C; RX-2190C).) For another example, Respondents identify a Netlist witness declaration stating, "[redacted]" (*Id.* at 64-65 (comparing RX-2327C at *6 with RX-2089C at *2-3; citing JX-2013C at 37:21-38:3, 39:17-20; Milton, Tr. at 289:3-291:2).) Respondents conclude these have immediate relation to Netlist's claim of domestic industry in this investigation. (*Id.* at 65.)

In opposition, Netlist primarily claims that in both investigations "[the] evidence has always supported the notion that Netlist's product development plan has been first to create an FPGA-based version of HybriDIMM in a first phase of development and, subsequently, to create

[redacted] in a second phase of development." (CIB at 104.) Netlist characterize Respondents as "cherry-pick[ing] snippets of forward-looking and aspirational testimony by Netlist's executives in the 1023 Investigation regarding the business plan of the company" which nonetheless "corroborates Netlist's steadfast approach to developing HybriDIMM and the business challenges of creating an industry-first product." (*Id.* at 104-105.)

Netlist disputes that its statements are anything like the misconduct in *Gilead Sciences* because "Netlist made no false statements, let alone any intentionally false statements." (*Id.* at 105.) Further, Netlist claims it has "performed multiple public and private demonstrations of its FPGA version of the HybriDIMM product" and "has offered [it] for sale and shipped to customers." (*Id.* at 106 (citing CX-2001C at Q/A 129-133, 139; CX-2005C at Q/A 8; CX-2007C at Q/A 50; JX-2015C at 79:25-80:18).) Netlist does caption, however, the testimony of its employee, Mr. Milton as one who "is not involved in the business side of the company and he was not even involved in the HybriDIMM project between the summer of 2016 and the summer of 2017." (*Id.* (citing CX-2005C at Q/A 7).) Netlist repeats the position that FPGA HybriDIMM was "ready for mass production—technically and in terms of manufacturing capacity . . . ." even though "[redacted]." (*Id.* ("Netlist grew to understand that other and greater business opportunities necessitate the development of an ASIC version of its HybriDIMM product.").) Netlist states again, "[redacted]" (*Id.* at 107.) Netlist argues its Board of Directors presentation, cited by Respondents, "does not change anything." (*Id.*) Netlist states:

[redacted]

[redacted] *See* Tr. (Sasaki) at 275:1-18.

(*Id.*)

With respect to "necessary and immediate relation," Netlist claims because it "is solely relying on the FPGA version to satisfy the domestic industry requirement in this Investigation, Respondents' arguments related to Netlist's business objectives for the ASIC version are irrelevant." (*Id.* at 108.) Netlist adds that the domestic industry findings in the prior investigation "did not center on any potential sales of that product" and "focused only on whether a domestic industry existed, not whether one was in the process of being established." (*Id.* at 108-109 (citing 1023ID at *171-172).) The Staff agrees with Netlist that no "immediate and necessary relation" has been shown. (SIB at 104.)

In its reply brief, Netlist emphasizes, in particular, the qualifications given from its employee, Mr. Milton, that his prior statements on [redacted] were in reference to "[redacted]" and [redacted] are not exclusive of one another. (CRB at 72 (citing Milton, Tr. at 284:13-285:17, 284:7-12).) Netlist again characterizes its 1023 Investigation testimony as "[redacted]" (*Id.* at 72.) Netlist concludes that, in any event, there is no precedent for barring it from any future Section 337 relief. (*Id.* at 73.)

Here, the undersigned understands Respondents' affirmative defense to be a serious allegation of malfeasance against Netlist, akin to the fraudulent acts required for inequitable conduct before the USPTO. For just one example, Respondents have presented a discrepancy between [redacted] and [redacted] and

related representations. (*See* RIB at 91-93 (citing, *inter alia*, RX-3770C at Q/A 20; RX-3771C at Q/A 32; RX-3772C at Q/A 137; RX-3775C at *3; RX-3776C at *3; Hong, Tr. at 182:6-184:21; RX-3771C at Q/A 32).)

Nevertheless, both parties acknowledge that the unconscionable act must have a "necessary and immediate relation" to the equity Netlist seeks in this investigation. On this point, Respondents contend there is a connection to Netlist's current economic prong domestic industry theory. (*See, e.g.*, RRB at 65.) The undersigned finds Respondents have not sufficiently shown such a connection. A review of Respondents' briefings reveals only a few mentions of statements, positions, or testimony—alleged to be false—that would have a connection to Netlist's current claim of significant investments in FPGA HybriDIMM as a domestic industry which "exists." A majority of Respondents' identified-as-false statements would only be relevant to a domestic industry alleged to be in the process of being established—as was the theory in the 1023 Investigation. (1023 ID at 164.)

For example, Respondents identify the statement from Netlist's G.R. 7.3 mandatory disclosure that [redacted] (RIB at 92.) Even if false, the undersigned does not see the connection to Netlist's presentation of FPGA HybriDIMM investments already incurred to show its industry "exists" in this investigation.

For another example, Respondents refer to August depositions in which Netlist witnesses supposedly testified that [redacted] (RIB at 93.) Respondents only loosely connect this testimony to Netlist's current economic prong theory, however, stating "[t]he truth is the FPGA HybriDIMM has been a dead product since before the 1023 hearing" and "[t]hus no version of HybriDIMM constitutes a domestic industry

today." (*See id.*) It is unclear here what the unconscionable act is beyond the Netlist's general contention that it has a FPGA HybriDIMM domestic industry in existence. Without further clarification, the undersigned views the ASIC "plan" testimony as more properly applied to the merits of Netlist's economic prong position.

For another example, and in direct reference to the "immediate and necessary relation" element of unclean hands, Respondents state "[h]ere, Netlist sought—and gained—an unfair advantage by misrepresenting facts to support domestic industry to FPGA HybriDIMM." (RIB at 94.) It is again unclear what advantage Respondents are referring to here that would pertain to the present investigation as opposed to the 1023 Investigation where economic prong domestic industry was determined to be satisfied. Indeed, Respondents next statement implies it is discussing what occurred in that prior case—"[i]n the 1023 Investigation Netlist's misrepresentations carried the day . . . ." (*Id.*)

Respondents' reply brief provides another example; they state "[i]n this investigation, Netlist would have the CALJ belief that 'Netlist intended—and still intends—to sell FPGA HybriDIMM to customers." (RRB at 63 (citing CIB at 105).) That quoted statement from Netlist, however, comes from its address of Respondents' unclean hands defense, *not* its economic prong discussion. (*See* CIB at 105.)

Respondents' reply brief also identifies Netlist's statement that "FPGA HybriDIMM 'was fully functional and ready for distribution to customers as early as [redacted]'" (RRB at 64 (citing CIB at 96 n.11).) While this statement is from Netlist's economic prong discussion, and Respondents subsequently provide various examples from the record suggesting it is a misrepresentation, FPGA HybriDIMM's status as "fully functional and ready for distribution" has only limited nexus to Netlist's current economic prong theory (*i.e.*, that its quantifiable investments

made "from January 1, 2014 through the filing date of the complaint in this Investigation" are significant or substantial). (*See* CIB at 96.) The same is true for the declaration from Netlist's employee Ms. Sasaki regarding shipments of [redacted]" (*See* RRB at 64 (citing RX-23237C at *6; CIB at 96).) Whether or not this is true has only a limited (*i.e.*, not necessary) relation to the reliability of Netlist's current economic prong theory. *Serdarevic v. Advanced Med. Optics, Inc.*, 532 F.3d 1352, 1362 (Fed. Cir. 2008) ("Because the defendants' alleged misconduct was not responsible for Serdarevic's delay, the district court was correct to conclude that the defendants' laches defense was not precluded by unclean hands"); *Gilead*, 888 F.3d at 1240 ("The court also found, with adequate evidentiary support, that the false testimony, in both respects, bore on the origin story of the February 2005 amendment, which was relevant to the invalidity issues in the litigation and hence immediately and necessarily related to the equity of the patent-enforcement relief Merck seeks in this case.").

Accordingly, the undersigned does not find that Respondents have shown Netlist acted with unclean hands so as to prevent any relief in the event a violation is found. The discrepancies and potential misrepresentations are more appropriately addressed in evaluating the reliability of Netlist's economic prong claims—*e.g.*, providing a basis to question whether Netlist has engaged entirely, as in 100%, in FPGA development to the exclusion of ASIC development prior to the complaint in the year 2017. (*See* RIB at 86-87; Order No. 40; CIB at 96 n.11 [redacted] . . . .").)

VIII. CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties, and subject-matter jurisdiction over the accused products.

2. The importation or sale requirement of section 337 is satisfied as to all Respondents.

3. Respondents do not infringe any asserted claim of U.S. Patent No. 9,535,623.

4. Respondents do infringe asserted claims 1-8, 10, 12, 14, and 15 of U.S. Patent No. 9,606,907.

4. Asserted claims 1, 2, 3, 4, 5, 7, 8, 10, 14, and 15 of U.S. Patent No. 9,606,907 are invalid under 35 U.S.C. § 103 as obvious; all other asserted claims are not invalid under 35 U.S.C. § 103.

5. The asserted claims of U.S. Patent No. 9,606,907 are not invalid under 35 U.S.C. § 112 as failing to comply with the written description requirement.

6. The technical prong of the domestic industry requirement for U.S. Patent No. 9,535,623 has not been satisfied.

7. The technical prong of the domestic industry requirement for U.S. Patent No. 9,606,907 has been satisfied.

8. The economic prong of the domestic industry requirement has been satisfied for U.S. Patent Nos. 9,535,623 and 9,606,907.

IX. RECOMMENDED DETERMINATION ON REMEDY & BOND

The Commission's Rules provide that the administrative law judge shall issue a recommended determination concerning the appropriate remedy in the event that the Commission finds a violation of section 337, and the amount of bond to be posted by respondents during Presidential review of the Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(l)(ii).

A. Limited Exclusion Order

Under section 337(d), the Commission may issue a limited exclusion order ("LEO") directed to a respondent's infringing products. 19 U.S.C. § 1337(d). A limited exclusion order instructs the U.S. Customs Service to exclude from entry all articles that are covered by the patent at issue that originate from a named respondent in the investigation. *See Fuji Photo Film Co. Ltd. v. Int'l Trade Comm'n*, 474 F.3d 1281, 1286 (2007).

Netlist argues that, "[i]n the event a violation of Section 337 is found, the CALJ should recommend that the Commission issue a Limited Exclusion Order directed to the relevant products of

the named Respondents, excluding any articles that infringe one or more claims of the Asserted Patents." (CIB at 119-120.) Netlist does not seek a general exclusion order.

Respondents do not dispute that, in the even a violation of section 337 is found, a LEO should issue. Respondents suggest, however, that such an order "should be tailored for administrability and to minimize harm to third parties" (RIB at 118) and argue a 12 month delay "commencing at the end of any suspension pending appeal of the FWDs of invalidity" is an appropriate tailoring (RRB at 80). Respondents also argue the nature of the Accused Products as compared to the asserted patent claims warrants a certification provision "so that any future design-around or other newly imported product from SK hynix could be readily identified to Customs as not subject to exclusion." (RIB at 118; RRB at 80.) Finally, Respondents request a repair exception to accommodate those products already sold to customers or new products "imported solely for research and testing purposes." (RIB at 119; RRB at 80.)

The Staff takes the position that "[t]o the extent a violation is found, a limited exclusion order extending to the accused products is the appropriate remedy, with the above discussed 6-12 month delay." (SIB at 107.)

In the event the Commission finds a violation, the undersigned recommends that a limited exclusion order issue prohibiting the importation of Respondents' RDIMMs and/or LRDIMMs found to infringe the asserted patents. The undersigned also recommends the inclusion of a provision whereby Respondents can certify that certain products are not subject to exclusion, as memory modules may be imported as subcomponents of larger devices, and ascertaining whether the modules are subject to the exclusion order would be difficult. The undersigned does not recommend incorporating the other exceptions requested by Respondents, as the record does not support them.

B. Cease and Desist Order

Under section 337(f)(1), the Commission may issue a cease and desist order ("CDO") in addition to, or instead of, an exclusion order. 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold, thereby undercutting the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate,* Inv. No. 337-TA-293 USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Prods. Containing Same, Including Air Conditioners for Automobiles,* Inv. No. 337-TA-334 (Remand), Comm'n Op. at 26-28, 1997 WL 817767, at *11-12 (U.S.I.T.C. Sept. 10, 1997).

In the event a violation of Section 337 is found, Netlist argues that a CDO should issue "prohibiting the domestic Respondents from engaging in the unlawful importation and/or sale within the U.S. of infringing articles." (CIB at 120.) Netlist submits that "the evidence showed that SK hynix America, Inc. maintains a commercially significant inventory of Accused Products." (*Id.* (citing CX-0282C); CRB at 80 (citing CX-0282C).) The Staff agrees that "the evidence shows approximately 4,000 units of LRDIMM products and 5,000 RDIMM products were in inventory as of September 1, 2016" with an implication that this is "commercially significant" to warrant a CDO. (*See* SIB at 107 (citing CX-0282C).)

Respondents contend that a CDO should not issue because "Netlist does not have a product that competes with the accused products" and otherwise has not shown why an alleged inventory is "commercially significant." (RIB at 119-120.) Respondents claim the singular exhibit cited by Netlist and the Staff to support a commercially significant inventory "is not in evidence." (RRB

at 80 (referring to CX-0282C).) In the event a CDO does issue, Respondents contend the order should include carve-outs for service and repair. (RIB at 120.)

Should the Commission find a violation of section 337, the undersigned does not recommend that a cease and desist order issue to SK hynix America. The exhibit that Netlist and the Staff rely on to show inventory, CX-0282C, is not in evidence. Accordingly, the record does not support a finding that SK hynix America maintains a commercially significant inventory, and thus the undersigned does not recommend issuance of a cease and desist order.

C. Bond During Presidential Review

Pursuant to section 337(j)(3), the Administrative Law Judge and the Commission must determine the amount of bond to be required of a respondent during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to issue a remedy. *See* 19 U.S.C. § 1337(j)(3). The purpose of the bond is to protect the complainant from any injury, *see* 19 C.F.R. § 210.42(a)(1)(ii), § 210.50(a)(3), and the Complainant bears the burden of establishing the need for a bond, *Certain Cast Steel Railways Wheels, Processes for Manufacturing or Relating to Same and Certain Prods. Containing Same*, Inv. No. 337-TA-655, Comm'n Op. at 12 (Mar. 19, 2010). In this investigation, however, Netlist does not seek a bond. (*See* CIB at 119-120; CRB at 80; RIB at 120 (citing CPB at 678).) Therefore, the undersigned does not recommend entry of any bond.

X. PUBLIC INTEREST

In connection with this Recommended Determination, and pursuant to Commission Rule 210.50(b)(1), 19 C.F.R. § 210.50(b)(1), the Commission ordered that the presiding administrative law judge:

> [S]hall take evidence or other information and hear arguments from the parties or other interested persons with respect to the public

> interest in this investigation, as appropriate, and provide the Commission with findings of fact and a recommended determination on this issue, which shall be limited to the statutory public interest factors set forth in 19 U.S.C. 1337(d)(1), (f)(1), (g)(1).

82 Fed. Reg. 57,291 (Dec. 4, 2017).

A. Agreement and Stipulation Regarding Certain Public Interest Factors

Netlist and Respondents entered into an Agreement and Stipulation Regarding Evidence and Recommendations Relating to the Statutory Public Interest Factors. (JX-2037.) That agreement includes the following provision:

> The findings of fact in sections XII (A) – (D) in the RD in Investigation No. 1023, relating to the statutory public interest factors, should be adopted in this Investigation and the parties request the CALJ adopt them. Based on these findings of fact, the same conclusions of law and recommendations regarding remedy relating to the statutory public interest factors as set forth in Sections XII (A) – (D) in the RD in Investigation No. 1023, e.g., "a delay of six to twelve months for any exclusion order," would be appropriate in this Investigation and the parties request the CALJ adopt them.

(*Id.* at 1-2 (footnotes omitted).) Moreover, if an exclusion order were to issue, Staff agrees with the private parties' stipulation that a six to twelve month delay is appropriate with respect to the public interest factors. (SIB at 105; SRB at 27-28.)

Based on the foregoing, the undersigned hereby adopts the findings of fact, conclusions of law, and recommendations set forth in JX-2037.

B. Patent Trial and Appeal Board ("PTAB") Final Written Decisions ("FWDs")

Netlist and Respondents submitted briefing on whether the PTAB's FWDs, rendering claims in the Asserted Patents invalid, weighs against imposition of any remedy. (*See* RIB at 95-97; RRB at 66; CRB at 73-74.) The parties refer to the "public interest" generally, but neither

party clearly connects their arguments on this issue to the specifically enumerated statutory public interest factors, *i.e.*, the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers. (*See id.*; 19 U.S.C. § 1337(d)(1), (f)(1), (g)(1).) Nevertheless, the parties treat this issue in the context of public interest and accordingly, the undersigned addresses the issue here.

Netlist argues that Respondents chose to advance their invalidity defenses under 35 U.S.C. § 102 and 103 in the PTAB and now must accept that they are estopped from litigating those same arguments elsewhere. (CRB at 73-74.) According to Netlist, the undersigned "should not rely on the FWDs in his public interest findings and should not recommend elimination or suspension of relief to which Netlist is otherwise due." (*Id.* at 74.) Netlist contends that Respondents' request to suspend any remedy is premature because if the FWDs are vacated and remanded, Respondents can return to the Commission to address the issue. (*Id.*)

Respondents submit that as of June 27, 2019, the PTAB has found all claims asserted in this Investigation to be unpatentable and thus, the undersigned should recommend against imposition of any remedy. (RIB at 95 (citing RX-2603 at *3327-3351; RX-2599 at *5041-5134).) Respondents argue that "[t]he public interest would be disserved by attributing exclusionary power to such invalid patent claims." (*Id.* (citing *Lear, Inc. v. Adkins*, 395 U.S. 653, 670 (1969)).) Respondents claim that the PTO recently expressed that a judicial remedy in a patent infringement case should not and would not be issued as long as the claims have been found by the PTAB to be unpatentable. (*Id.* (citing *BTG Int'l Ltd. v. Amneal Pharms. LLC*, Nos. 2019-1147 et al., Invited Brief for the Director – U.S. Patent and Trademark Office as Amicus Curiae in Support of Neither Party, at 9 (Fed. Cir. Feb. 1, 2019)).) According to Respondents, it would be "especially perverse

in the present circumstances where Respondents were deemed estopped even to advance meritorious invalidity positions accepted by the PTAB." (RIB at 96.)

Respondents contend that if the Commission finds a violation, the undersigned should recommend that any remedial order be denied, or at a minimum, decline to impose any remedy until such time as the PTAB's decisions are reversed, which Respondents claim is not likely to happen. (*Id.*; RRB at 66.) Respondents point out that the undersigned previously relied on the Commission's willingness to suspend enforcement of remedial orders pending final resolution of those PTAB decisions and thus, the undersigned should recommend suspension of any remedial orders until that time. (RIB at 96.)

Staff submits that it "will likely support a request for suspension of any remedial order pending the conclusion of the appeals of the PTO's determinations that the asserted claims of the two asserted patents are invalid." (SIB at 106 n.67.)

The undersigned finds that the parties have not presented any evidence to support declining to impose an exclusion order based on the PTAB's FWDs rendering claims in the Asserted Patents invalid.[22] The undersigned has already ruled on this matter with Order No. 49, which denied a similar request for a stay. No arguments have been presented in the parties' briefs that would cause the undersigned to modify the decision in Order No. 49. Moreover, the parties have already stipulated that a delay of six to twelve months for any exclusion order would be appropriate. (JX-2037.) Therefore, with respect to this issue, the undersigned finds no reason to recommend

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[22] Respondents' reference to the PTO's amicus brief in *BTG Int'l Ltd. V. Amneal Pharms. LLC* is misplaced. The portion of that brief Respondents quote is related to requesting a district court to stay infringement litigation in light of IPR proceedings. *See BTG*, Invited Brief for the Director – U.S. Patent and Trademark Office as Amicus Curiae in Support of Neither Party, at 9. It does not discuss the issue in this Investigation of whether an exclusion order from the Commission should be implemented or delayed based on the statutory public interest factors.

deviation from the previously stipulated delay of six to twelve months for imposition of any exclusion order.

C. RAND

Netlist contends that the RAND issue was resolved in the 1023 Investigation, the record in this Investigation is materially the same, and thus, there is no basis to revisit the RAND findings from the 1023 Investigation. (CIB at 109.) According to Netlist, it never ceased bargaining in good faith toward a RAND rate, even after the initial determination in the 1023 Investigation issued. (*Id.*) Netlist argues that in contrast, Respondents fail to meet their burden on any RAND-related defense and refuse to even consider or make counteroffers in licensing negotiations, thereby engaging in a patent holdout. (*Id.* at 110.)

Respondents argue that issuance of an exclusion order or cease and desist order in this Investigation has the potential to cause substantial harm to U.S. competition, consumers and innovation. (RIB at 97 (citing RX-0874 at *2).) Respondents claim that an exclusion order would likely force them to take a license from Netlist that would permit Netlist to "(i) extract excessive and unreasonable royalties that the evidence shows bear no relation to the value of Netlist's alleged SEPs, and (ii) distort competition in the module market by forcing SK Hynix to pay a discriminatory, non-competitive rate, which would result in harm to U.S. consumers, who will suffer reduced competition, increased prices, reduced innovation, and reduced participation in standard-setting." (*Id.* (citing CX-2002C at Q/A 374; RX-2005C at Q/A 26, 2009-47).) According to Respondents, the record in this Investigation includes new developments and evidence, not available during the 1023 Investigation, that prove Netlist violated its RAND obligations. (*Id.* at 97-98; RRB at 66-67.) Respondents also argue that the determination in the 1023 Investigation

does not dictate the result on the RAND issues in this Investigation because it has no collateral estoppel effect. (RRB at 66.)

Staff submits that valuation of Netlist's patents and a RAND rate is not necessary because the evidence does not show that the Asserted Patents are infringed or essential to any standard, especially given that the PTO determined that the claims of the Asserted Patents are unpatentable. (SIB at 108-09.) If the Commission does find that the Asserted Patents are essential, then Staff believes a six to twelve month delay of an exclusion order is sufficient to mitigate the harm to the public interest. (*Id.* at 110.)

1. Essentiality

Netlist does not specifically address this point, but Respondents rely on Netlist's contentions that each of the asserted patent claims is essential to a JEDEC standard. (RIB at 98-99 (citing CX-2007C at Q/A 17; RX-2074C at *63, 66, 68-69).) Respondents submit that similar to the 1023 Investigation, Netlist's admissions are sufficient to establish essentiality if infringement is found. (*Id.* at 99 (citing JX-2031C at *191).) Respondents also claim that Netlist acknowledged that each of the Asserted Patents was disclosed to JEDEC and Netlist committed to offer to license those patents "under reasonable terms and conditions that are demonstrably free of any unfair discrimination." (*Id.* (citing CX-2007C at Q/A 22-31; RX-2074C at *64, 67, 70).)

Staff contends that "the evidence does not show that the patents are essential to any standard." (SIB at 108; SRB at 27 (citing Levitt, Tr. at 444:18-445:2; Mangione-Smith, Tr. at 355:4-8).) Specifically, Staff contends that the claim construction for the '907 patent requires specific functionality by memory devices and it is undisputed that the JEDEC standards do not govern the internal workings of a memory device's response to a control signal. (SIB at 108-09 (citing Order No. 17 at 20; Levitt, Tr. at 444:18-445:2).) Staff therefore argues that the JEDEC

standards can be practiced without infringing the "do not . . . receive" limitation when properly interpreted to require more than merely "non-performance." (*Id.* at 109.) As to the '623 patent, Staff claims that the Clock-to-CA training is not required to practice the JEDEC standard and thus, the evidence does not show that practicing the JEDEC standard necessarily infringes the claims of the '623 patent. (*Id.* at 109 (Mangione-Smith, Tr. at 355:4-8).) Moreover, Staff contends that "given that the PTO has determined that the claims of the asserted patents are unpatentable, the evidence does not support finding that the asserted claims are 'essential' to practicing the standards." (*Id.*)

As stated in the determination in the 1023 Investigation, "a necessary pre-requisite to any determination that Complainant has violated a RAND licensing obligation is a showing that the asserted patents in this investigation are actually standard essential." (1023 ID at 182.) If the Asserted Patents are not essential to a JEDEC standard, then Netlist does not have a RAND licensing obligation for those patent claims. (*Id.*)

Netlist asserts that "[t]he Accused Products . . . and various of their components, comply with various JEDEC standards." (CIB at 15-16.) If the Accused Products comply with JEDEC standards, then a standard essential patent would necessarily be infringed by those products. *See Certain Memory Modules*, Initial Determination at 182. Indeed, the JEDEC Patent Policy defines "Essential Patent Claims" as "[t]hose Patent claims the use of which would necessarily be infringed by the use, sale, offer for sale or other disposition of a portion of a product in order to be compliant with the required portions of a final approved JEDEC Standard." (RX-2659 at *31.) Therefore, assuming that the Accused Products comply with JEDEC standards, as Netlist asserts, the evidence does not show that the Asserted Claims of the '623 patent are essential to any JEDEC standard because, as determined above, the Accused Products do not infringe the Asserted Claims

of the '623 patent. And because those claims are not essential to a JEDEC Standard, Netlist had no obligation to license those patent claims to Respondents under the JEDEC Agreement and thus, the issue of whether Netlist breached any RAND obligations as to that patent is moot. (*See* RX-2659 at *34; *Certain Magnetic Data Storage Tapes and Cartridges Containing the Same*, Inv. No. 337-TA-1012, Comm'n Op. at 102-05 (Apr. 2, 2018).)

As to the '907 patent, Netlist contends that the '907 patent claims are essential to JEDEC standards. (*See* CX-2007C at Q/A 17; RX-2074C at *63-69.) For example, Netlist's Vice President of Intellectual Property and Licensing testified that "based on our analysis, each of the asserted claims is essential to a JEDEC standard." (CX-2007C at Q/A 17.) In addition, pursuant to customary objections, Netlist admitted that it "was a member of at least one JEDEC committee that developed one or more final JEDEC standards to which the '907 patent is essential for DDR4 LRDIMM standard-compliant products." (RX-2074C at *64.) Accordingly, if the Commission determines that the '907 patent is infringed in this Investigation, the undersigned finds that the evidence of record would support the conclusion that the Asserted Claims of the '907 patent are essential to a JEDEC standard.

2. Enforceability

Respondents argue that under applicable New York law, the RAND commitments Netlist made are legally enforceable. (RIB at 99-100 (citing RX-2659 at *37).) Respondents contend that Netlist agreed to abide by the JEDEC Patent Policy, submitted multiple LOAs promising to offer a license under reasonable terms and conditions demonstrably free of unfair discrimination, and acknowledged that its RAND commitments are binding contracts. (*Id.* at 100 (citing RX-2659 at *34-35; CX-0530 at *27-28; Whitley, Tr. at 201:20-206:10; CX-2007C at Q/A 33, 114; RX-2337C at *21-22).) Respondents claim that their experts relied on consensus understandings of

"reasonable" and "unfair discrimination" and determined that Netlist's offers were not RAND. (*Id.* (citing RX-2004C at Q/A 50-51, 101-06, 345-49, 356).) Respondents also claim that "[c]ourts interpreting the same terms in the IPR policies of other SSOs have likewise been able to assess patent holders' compliance with RAND obligations." (*Id.* (citing *TCL Commc'ns Tech. Holdings, Ltd. V. Telefonaktiebolaget LM Ericsson*, 2018 WL 4488286, at *26, 48-52, 55-56 (C.D. Cal. Sept. 14, 2018)).) Moreover, Respondents argue that public policy concerns also favor enforcement of Netlist's RAND commitments in order to avoid anticompetitive consequences. (*Id.* at 100-101 (citations omitted).)

As stated in the 1023 ID, "it appears that the JEDEC Patent Policy is, by design, ambiguous about the meaning of reasonable license terms and conditions" and "the undersigned cannot determine what exactly the RAND commitment entails in terms of acceptable licensing terms." (1023 ID at 195.) In fact, the JEDEC Patent Policy merely defines "RAND" as "[r]easonable and non-discriminatory licensing terms and conditions" with no definition for "reasonable" or "non-discriminatory." (RX-2659 at *31; *see* 1023 ID at 194.) Respondents cite to *Cobble Hill Nursing Home* for the proposition that "[b]efore rejecting an agreement as indefinite, a court must be satisfied that the agreement cannot be rendered reasonably certain by reference to an extrinsic standard that makes its meaning clear." (*See* RIB at 100 (citing *Cobble Hill Nursing Home, Inc. v. Henry and Warren Corp.*, 548 N.E.2d 203, 206 (N.Y. 1989).) Respondents, however, never articulate any extrinsic standard or agreed-upon methodology by which the undersigned can determine the meaning of certain license terms and conditions, such as "reasonable" and "non-discriminatory." (*See* RIB at 99-100; 1023 ID at 194-95; *Cobble Hill*, 548 N.E.2d at 206; *166 Mamaroneck Ave. Corp. v. 151 East Post Road Corp.*, 575 N.E.2d 104, 105-06 (N.Y. 1991); *Joseph Martin, Jr., Delicatessen, Inc. v. Schumacher*, 417 N.E.2d 541, 544 (N.Y. 1981).) Instead,

Respondents ambiguously state that their experts rely on "consensus understandings of 'reasonable' and 'unfair discrimination.'" (*See* RIB at 100 (citing RX-2004C at Q/A 50-51, 101-06, 345-49, 356).) However, those "consensus understandings" are not an extrinsic standard or methodology, but are merely their expert's reliance on the Samsung JDLA as a comparable license. (*See* RX-2004C at Q/A 50-51, 101-06, 345-49, 356.) That testimony does not include references to any methodology or extrinsic standard, let alone an agreed-upon one, that clarifies the meaning of the terms "reasonable" and "non-discriminatory." (*Id.*) In addition, while Respondents cite to a district court interpreting an IPR policy for a standards setting organization, Respondents fail to explain why analysis of that policy should inject meaning into the JEDEC agreement, particularly when that court considered an agreement for a different organization than JEDEC that was subject to the laws of France instead of New York. *See TCL Commc'ns Tech. Holdings*, 2018 WL 4488286, at *5. Accordingly, the undersigned finds no reason to disturb the previous finding that the JEDEC agreement is unenforceable. (1023 ID at 195-196.) The undersigned, however, notes that similar to the 1023 Investigation, none of the parties asserts that the JEDEC agreement is unenforceable and thus, the undersigned analyzes whether Netlist breached its RAND obligations below.

3. RAND Obligations

Netlist argues that it "fulfilled whatever RAND obligations it may have" and Respondents are engaging in a patent holdout. (CIB at 109-19.) Netlist contends that Respondents are using the same arguments previously raised and rejected in the 1023 Investigation and thus, fail to meet their burden on any RAND defense. (*Id.* at 113) According to Netlist: (1) it made multiple licensing offers to Respondents; (2) [redacted] (3) it provided Respondents with its underlying methodology and data, explained the methodology's

judicial origins to Respondents, and invited Respondents to discuss the approach; and (4) the Commission has already denied arguments that Netlist breached a RAND obligation. (*Id.*) Netlist contends that this demonstrates its good faith efforts to arrive at a RAND distribution of the profits that Respondents earn from implementing Netlist's SEPs. (*Id.*) In addition, Netlist argues that the determination in the 1023 Investigation confirms that its negotiations were consistent with whatever RAND obligations it may have. (*Id.*)

Respondents assert that Netlist's offers to Respondents have not been on terms that are "reasonable" and "demonstrably free of any unfair discrimination." (RIB at 101-117.) Respondents argue that new evidence shows [redacted] (RRB at 67 (citing RDX-3873; Hong, Tr. at 108:25-109:4, 125:12-130:19; Whitley, Tr. at 211:9-214:3, 217:17-220:22; RX-2220C; RX-580C), 71-77.) Respondents further contend that they are not engaging in a patent hold-out and are not unwilling licensees. (*Id.* at 77-78.) Respondents argue that their refusal to acquiesce to Netlist's licensing demands does not suggest that they negotiated in bad faith or engaged in a holdout because the determination in the 1023 Investigation found that they did not infringe any asserted patents, Netlist also has failed suits in Germany and China, and the PTO found every asserted claim invalid. (*Id.* at 78.) Respondents therefore maintain that their [redacted] is "if anything, generous." (*Id.*)

Staff submits that "if the Commission accepts the private parties' contention that the patents are essential, and then accepts the private parties' contention that an obligation exists, then the remaining question is whether the evidence shows that Netlist has failed to comply with the 'RAND obligation' in a manner that has caused harm to one of the Commission's public interest facts such that Commission's relief should be modified." (SIB at 109-10 (footnote omitted).) Staff

argues that whether Respondents are required to take Netlist's highest license offer or are subject to an exclusion order, the effect in both cases is a high cost of the product for consumers. (*Id.* at 110.) Staff therefore contends that a six to twelve month delay would sufficiently mitigate the harm to the public interest in both cases. (*Id.*) In addition, Staff submits that evidence of increased cost/prices is generally not relevant to the public interest factors and thus, Staff argues that the evidence does not support deviating from the recommended six to twelve month delay even though this Investigation implicates a standard. (*Id.*) Staff also claims that the only material "new" evidence pertains to [redacted] (*Id.* at 111.) Staff asserts that the evidence shows that [redacted] and Netlist [redacted] (*Id.* (citing Sasaki, Tr. at 259:11-25).) Therefore, should the RAND issue require further adjudication, Staff contends that the evidence may support finding that [redacted] would be a relevant agreement for the purposes of a RAND rate analysis. (*Id.*) However, Staff states that "it would appear to be an inefficient use of Commission resources to determine a RAND rate for patents that have been determined to be unpatentable by the PTO." (*Id.*)

At the outset, it is important to reiterate that "the burden to prove an affirmative defense based on a breach of Complainant's RAND obligations lies with Respondents." (1023 ID at 192-93.) In the 1023 Investigation, the undersigned found that Respondents did not establish a violation of the JEDEC agreement by Netlist. (*Id.* at 195-97.) In particular, the undersigned found that the JDLA "is not the same type of agreement that is required under the JEDEC Patent Policy", the undersigned was "not persuaded by Respondents' argument that the [redacted]" and the undersigned found that "at the time [redacted] Complainant apparently believed it was receiving valuable consideration from having [redacted]

[redacted] (*Id.*) Therefore, the undersigned found that "Respondents have not made out a showing of unfair discrimination based on [redacted] (*Id.*) Thus, the central question here is whether Respondents have presented any evidence not considered in the 1023 Investigation that justifies a deviation from the determination in that investigation.

Staff contends that the only material new evidence since the 1023 Investigation is "the status of the [redacted] JDLA agreement and whether it may be applied as an 'effective rate'" and Respondents argue that new evidence shows [redacted] (*See* SIB at 111; RRB at 67 (citing RDX-3873; Hong, Tr. at 108:25-109:4, 125:12-130:19; Whitley, Tr. at 211:9-214:3, 217:17-220:22; RX-2220C; RX-580C), 71-77.) The majority of this evidence, however, is not new and was considered in the 1023 Investigation. (*See* 1023 ID at 184-97.) For example, evidence showing Mr. Whitley's "[redacted]" was considered in the 1023 Investigation. (*See id.*) Similarly, the JDLA itself, as well as evidence of various terms in the JDLA, were considered in the 1023 Investigation. (*See id.*)

Respondents present evidence showing that Netlist pursued various patent cases against Hynix and none of the cases found a Netlist patent valid and infringed, and that to comply with the obligations in the JDLA, [redacted] (*See* Hong, Tr. at 125:12-126:10; Whitley, Tr. at 219:2-220:22.) Moreover, the evidence shows that [redacted] and [redacted] (Sasaki, Tr. at 259:11-25.) As in the 1023 Investigation, Respondents' central argument here is that Netlist is obligated to offer them licensing terms comparable to the JDLA. (*See, e.g.*, RRB at

72.) The undersigned, however, finds that this evidence does not negate the conclusion from the 1023 Investigation that the JDLA is not the same type of agreement that is required under the JEDEC Patent Policy nor the finding that "at the time the JDLA was executed, Complainant apparently believed it was receiving valuable consideration from having [redacted] (*See* 1023 ID at 195-96.) Therefore, Respondents have failed to show why the undersigned should deviate from the previous determination in the 1023 Investigation that Respondents have not made out a showing of unfair discrimination based on the JDLA. (*See id.*)

Accordingly, even assuming the Asserted Patents are standard essential and the JEDEC agreement is enforceable, the undersigned finds no reason to deviate from the previous determination that Netlist did not violate its RAND obligations. (*See id.* at 196-97.) Therefore, the undersigned finds that the evidence does not support foregoing or delaying an exclusion order on the basis of a RAND obligation by Netlist. However, even if the Commission were to find that Netlist breached its RAND obligations, the undersigned agrees with Staff that the practical effect would be a high product cost for consumers, which would be sufficiently mitigated by a six to twelve month delay for imposition of an exclusion order. (*See* SIB at 110.) Moreover, as Staff notes, the Commission has found that "evidence that an exclusion order could lead to higher prices is not dispositive of the public interest." *See Certain Automotive Parts*, Inv. No. 337-TA-557, Comm'n Op. at 12-13 (July 5, 2007) (citing *Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Comm'n Op. at 6 (Jan. 1990)). Thus, the undersigned finds that even if the Commission determines that Netlist breached its RAND obligations, the evidence does not support recommending deviation from the previously stipulated six to twelve month delay for imposition of an exclusion order.

4. Recommendation

Based on the foregoing, the undersigned recommends that should the Commission find a violation, entry of an exclusion order be delayed by six to twelve months.

XI. INITIAL DETERMINATION

Based on the foregoing, it is the Initial Determination of the undersigned that Respondents do not infringe any asserted claim of U.S. Patent No. 9,525,623, but do infringe the asserted claims 1-8, 10, 12, 14, and 15 of U.S. Patent No. 9,606,907. The undersigned further determines that asserted claims 1, 2, 3, 4, 5, 7, 8, 10, 14, and 15 of the '907 patent have been shown to be invalid, but claims 6 and 12 have not been so shown. Additionally, the domestic industry requirement has been satisfied for the '907 patent, but not for the '623 patent.

The undersigned hereby CERTIFIES to the Commission this Initial Determination and the Recommended Determination. The parties' briefs, which include the final exhibits lists, are not certified as they are already in the Commission's possession in accordance with Commission rules. *See* 19 C.F.R. § 210.38(a).

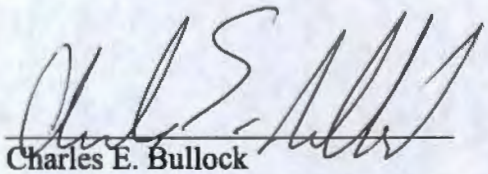
The Secretary shall serve the confidential version of this Initial Determination upon counsel who are signatories to the Protective Order (Order Nos. 1, 3) issued in this Investigation. A public version will be served at a later date upon all parties of record.

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission unless a party files a petition for review pursuant to 19 C.F.R. §210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion a review of the Initial Determination or certain issues therein.

Within ten days of the date of this document, the parties shall submit to the Office of Administrative Law Judges a joint statement regarding whether or not they seek to have any portion of this document deleted from the public version. The parties' submission shall be made

by hard copy and must include a copy of this Initial Determination with red brackets indicating any portion asserted to contain confidential business information to be deleted from the public version.[23] The parties' submission shall include an index identifying the pages of this document where proposed redactions are located. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.



Charles E. Bullock
Chief Administrative Law Judge

[23] If the parties submit excessive redactions, they may be required to provide an additional written statement, supported by declarations from individuals with personal knowledge, justifying each proposed redaction and specifically explaining why the information sought to be redacted meets the definition for confidential business information set forth in Commission Rule 201.6(a). 19 C.F.R. § 201.6(a).

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **INV. NO. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **PUBLIC VERSION FINAL INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMDY AND BOND** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on **11/4/2019**.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT NETLIST, INC.	
James M. Wodarski, Esq. **MINTZ LEVIN COHN FERRIS GLOVSKY and POPEO PC** One Financial Center Boston, MA 02111	☐ Via Hand Delivery ☑ Express Delivery ☐ Via First Class Mail ☐ Other: _____
FOR RESPONDENTS SK HYNIX, INC., SK HYNIX AMERICA, INC. and SK HYNIX MEMORY SOLUTIONS, INC.	
Michael R. Franzinger, Esq. **SIDLEY AUSTIN LLP** 1501 K Street NW Washington, DC 20005	☐ Via Hand Delivery ☑ Express Delivery ☐ Via First Class Mail ☐ Other: _____

Public Version

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	**Inv. No. 337-TA-1089**

ORDER NO. 17: CONSTRUING TERMS OF THE ASSERTED PATENTS

(August 30, 2018)

The claim terms construed in this Order are done so for the purposes of this Investigation. Hereafter, discovery and briefing in this Investigation shall be governed by the construction of the claim terms in this Order. Those terms not in dispute need not be construed. *See Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms).

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TABLE OF ABBREVIATIONS

CIMB	Complainant's Initial Markman Brief
CRMB	Complainant's Reply Markman Brief
RIMB	Respondents' Initial Markman Brief
RRMB	Respondents' Reply Markman Brief
SIMB	Commission Investigative Staff's Initial Markman Brief
SRMB	Commission Investigative Staff's Reply Markman Brief

I. INTRODUCTION

By publication of a notice in the Federal Register on Dec. 4, 2017, the U.S. International Trade Commission ordered that:

> Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain memory modules and components thereof by reason of infringement of one or more of claims 1-8, 10, 12, 14-22, 24-25, 27, 29-35, 38, 43-45, 47, 48, 50, 52, and 58 of the '907 patent and claims 1-5, 7-15, 17-25, 27, and 29 of the '623 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337;

82 FR 57290-1 (Dec. 4, 2017). The complainant in this investigation is Netlist, Inc. ("Netlist"). The named respondents are SK hynix, Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc. ("Respondents"). The Office of Unfair Import Investigations ("Staff") is also a party to this Investigation.

On January 30, 2018, I issued the procedural schedule for this investigation. (*See* Order No. 7.) In accordance with that schedule, the parties exchanged: (i) on February 23, 2018, their lists of proposed terms for construction, as required by G.R. 8.1; and (ii) on March 5, 2018, their preliminary constructions for those terms, as required by G.R. 8.2. The parties filed their Joint Claim Construction Chart on March 12, 2018. Thereafter, on March 26, 2018, the parties filed their initial claim construction briefs, and, on April 9, 2018, the reply claim construction briefs. On March 30, 2018 and April 9, 2018, respectively, the Staff submitted its initial and reply briefs.

In parallel, and on February 20, 2018, Respondents filed a motion for summary determination of non-infringement for reasons of issue preclusion and claim preclusion. For issue preclusion specifically, Respondents' motion turned on a comparison of claim terms at issue in this investigation, which also happen to be identified in the parties' Markman briefing, and terms

determined to be non-infringed in a prior Investigation, Inv. No. 337-TA-1023 (the "1023 Investigation"). The parties, and the Staff, submitted several rounds of briefing and on April 12, 2018, I granted the motion with an initial determination. This terminated the investigation in its entirety. (Order No. 13.)

On May 29, 2018, the Commission gave notice that it had determined to review and upon review, vacate Order No. 13 and remand to me for further proceedings. (EDIS Doc. No. 646160.) The notice read:

> The Commission finds that the ALJ erred by finding that SK hynix did not infringe the asserted claims of the '907 and '623 patents without first resolving the parties' relevant claim construction disputes. The Commission therefore remands the investigation to the ALJ for further proceedings.

(*Id.* at 2) Concurrently, the Commission issued a Remand Order (EDIS Doc. No. 646161) which elaborated on the error:

> Here, the ID found that SK hynix did not infringe the "output or receive / do not output or receive" limitations of the '907 patent, and the "a notification signal [...] indicating a [or at least one] status of one or more training sequences" of the '623 patent. The parties' claim construction briefing, however, shows that the parties have disputes over the proper construction of those limitations. The ALJ was therefore required to construe claim terms to resolve those disputes prior to ruling on the infringement or noninfringement of those limitations and whether issue preclusion applies. Because the ALJ did not do so, the Commission reviews and vacates the ID's summary determination that SK hynix does not infringe the asserted claims, and remands the investigation to the ALJ for further proceedings, including resolving the parties' claim construction disputes.

(Remand Order at 3.)

With the investigation returned to me, I therefore issued Order 14 on June 14, 2018, an initial determination extending the target date and amending the procedural schedule to accommodate that extension. Due to conflicts with my other pending investigations, no Markman

hearing could be scheduled for this investigation. Thus, the parties' claim construction disputes are resolved on the briefings.

II. RELEVANT LAW

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms."

Id. at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be "highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.* "Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee." *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999).

The specification "is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be ... the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Id.* at 1317; *see also Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by

demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see also Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) "the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;" or (2) "the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009); *see also GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."); *Omega Engineering, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("[W]here the patentee

has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution."). Nevertheless, there is a "heavy presumption that a claim term carries its ordinary and customary meaning." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is "exacting" and requires "a clear and unmistakable disclaimer." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012); *see also Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope" to deviate from the ordinary meaning) (citation omitted). As the Federal Circuit has explained, "[w]e do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that." *Thorner v. Sony Comp. Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012). 'The party seeking to invoke prosecution history disclaimer bears the burden of proving the existence of a 'clear and unmistakable' disclaimer that would have been evident to one skilled in the art." *TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1063-64 (Fed. Cir. 2016) (citing *Elbex Video, Ltd. v. Sensormatic Elecs. Corp.*, 508 F.3d 1366, 1371 (Fed. Cir. 2007)).

Courts are not required to construe every claim limitation of an asserted patent. *See O2 Micro Intern. Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (citations omitted). Rather, "claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement." *Id.* at 1362 (quoting *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997)); *see also Embrex*, 216 F.3d at 1347 ("The construction

of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.") (citation omitted). In addition, "[a] determination that a claim term 'needs no construction' or has the 'plain and ordinary meaning' may be inadequate when a term has more than one 'ordinary' meaning or when reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *O2 Micro*, 521 F.3d at 1361. Claim construction, however, is not an "obligatory exercise in redundancy." *U.S. Surgical Corp.*, 103 F.3d at 1568. "[M]erely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction." *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004).

Regarding claim preambles, the Federal Circuit has held that "a claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp*, 55 F.3d 615, 620 (Fed. Cir. 1995). Put another way, "the preamble may be construed as limiting "if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Am. Med. Sys., Inc. v. Biolitec, Inc.*, 618 F.3d 1354, 1358 (Fed. Cir. 2010) (citing *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002)); *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). The Federal Circuit held "the preamble has no separate limiting effect if, for example, 'the preamble merely gives a descriptive name to the set of limitations in the body of the claim that completely set forth the invention.'" *Id.* at 1359 (citing *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1434-35 (Fed. Cir. 2000)).

III. LEVEL OF ORDINARY SKILL

A. Netlist's Position

For the '907 patent, Netlist argues a person of ordinary skill would "have an electrical or computer engineering background, and specifically, a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one, and preferably two, years of work experience relating to memory systems." (CIMB at 12-13.) Netlist adds that this is the same level as determined in the 1023 Investigation for the parent to the '907 patent, U.S. Patent No. 8,516,185, (the "'185 patent") and "such a person would also be familiar with the design of memory devices and memory modules." (*Id.* at 13.)

For the '623 patent, Netlist argues a person of ordinary skill would "have a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and memory module handshaking and training procedures." (CIMB at 47.)

B. Respondents' Position

Respondents argue the ordinary level of skill for the '623 patent should be the same as that which they argued for the parent patent at issue in the 1023 Investigation, U.S. Patent No. 8,489,837 (the "'837 patent"), which is "a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems." (RIMB at 8.) Respondents add the person should be "familiar with computer memory systems and basic CPU architecture, technical standards governing the operation of memory devices" and techniques related to how computer memory is accessed. (*Id.*)

For the '907 patent, Respondents again look to the level determined for the '185 patent in the 1023 Investigation, namely:

> [A] person or ordinary skill would have "an electrical or computer engineering background, and specifically, a Bachelor's degree in electrical engineering, computer engineering, or in a related filed and at least one—and preferably two—years of work experience relating to memory systems."

(RIMB at 19.)

C. Staff's Position

The Staff argues along the same lines as the private parties, in that the level of ordinary skill for each asserted patent should be the same as that determined for their parent patents in the 1023 Investigation under principles of issue preclusion. (*See* SIMB at 6-7.)

D. Analysis

For the '907 patent, I see no reason to depart from the parties' agreed level of ordinary skill, which is that also determined in the 1023 Investigation for the parent of the '907 patent. Thus, I find the level of ordinary skill for the '907 patent to be a person having an electrical or computer engineering background, and specifically, a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one—and preferably two—years of work experience relating to memory systems.

For the '623 patent, the parties' descriptions of ordinary skill only differ in how they describe experiences the hypothetical person would have had. I find the identity of disclosure between the '623 patent and the '837 patent, at issue in the 1023 Investigation, justifies adopting the ordinary skill description determined in that investigation. Thus, I find the level of ordinary skill for the '623 patent to be a person with a Bachelor's degree in electrical engineering, computer engineering, or in a related field and at least one year of work experience relating to memory systems, and would be familiar with the design of memory devices, memory modules, and built-in-self test or BIST.

IV. CLAIM CONSTRUCTION OF AGREED TERMS

The parties' Joint List of Claim Terms for Construction and Proposed Constructions and initial Markman briefs do not indicate any claim terms for which there is an explicit agreed construction. (*See* EDIS Doc. No. 638742; *see generally* CIMB; RIMB; SIMB.)

V. CLAIM CONSTRUCTION OF DISPUTED TERMS

A. "output or receive ... data" / "do not output or receive any data"

The term "output or receive ... data" / "do not output or receive any data" appears in asserted claims 1, 16, 43, and 58 of the '907 patent. These claims read:

> 1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
>
> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
>
> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices **output or receive** each N-bit wide data signal associated with the memory read or write command while the second memory devices **do not output or receive** any data associated with the memory read or write command;
>
> M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective

set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

....

16. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices **output or receive** each N-bit wide data signal associated with the memory read or write command while the second memory devices **do not output or receive** any data associated with the memory read or write command;

a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one

or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines, wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

43. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices;

a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices **output or receive** the data associated

with the memory read or write command while other memory devices not in the subset of the memory devices **do not output or receive** any data associated with the memory read or write command;

a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.

....

58. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices including first memory devices and second memory devices;

a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices **output or receive** data associated with the first memory read or write command while the second memory devices **do not output or receive** any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices **output or receive** data associated with the second memory read or write command while the first memory devices **do not output or receive** any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;

a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals

> from when the logic is responding to the first module control signals, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and
>
> a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

(emphasis added).

The constructions proposed by the parties for this term are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
"transmit or acquire data / do not transmit or acquire data"	Plain and ordinary meaning, with the same understanding as stated for term 1 [below, *i.e.*, "when considered with the surrounding language of the respective claim, the resulting physical arrangement of the elements of the claim (when given their plain and ordinary meaning) is a 'fork in the road' layout (as that phrase was used in the 1023 ID and post-hearing briefs), examples of which are shown [above on pages 32–33], such that the "first memory devices" (in ranks A and C in the example below)	non-selected devices do not receive any data or send any data associated with the memory controller read/write command "receive any data associated with" - plain and ordinary meaning reflects the notion that no data transmitted to the selected/first memory devices is transmitted to the unselected/second memory devices

	and the "second memory devices" (in ranks B and D in the example below) are not coupled to the buffer circuit by the same module data lines, and instead are coupled to the buffer circuit by different module data lines, such that data associated with a write command intended for the "first memory devices" is communicated by the buffer circuit to, and received by, the "first memory devices" but not the "second memory devices" (as shown by the blue arrow in the examples [above on pages 32–33])"].	

1. Netlist's Position

In its opening brief, Netlist explains its view that "when read in the context of the claims an in view of the specification, a person of ordinary skill would properly understand that 'output . . . data' refers to the final stage of a read operation from a memory device in the selected rank, *i.e.*, transmitting data." (CIMB at 24.) Netlist continues, "when read in the context of the claims and in view of the specification, a person of ordinary skill would properly understand that 'receive . . . data' refers to the first stage of a write operation to a memory device in the selected rank, *i.e.*, acquiring data." (*Id.*) Netlist acknowledges "the intrinsic record does not expressly articulate what is meant by 'output or receive . . . data' in the context of memory devices." (*Id.*) Nevertheless, Netlist claims persons of ordinary skill would understand the terms according to Netlist's proposed construction because "[i]n order to perform a write operation, a selected memory device must acquire data sent to it along the shared data line from the buffer circuit. Conversely, in order to perform a read operation, a selected memory device must transmit data

along the shared data line to the buffer circuit." (*Id.*) Netlist then references expert testimony from the 1023 Investigation to argue that "when a chip select signal activates a particular rank of memory devices for a write operation, the memory devices in that rank are capable of 'receiving data.'" (*Id.* at 24-25 (citing CIMB, Ex. 7 at 649:14-652:2).)

Netlist also disputes that this term requires the first and second memory devices be coupled to different physical terminals of each buffer circuit. (*Id.* at 25.) Netlist states "[t]he notion that the claimed buffer circuit can transmit only to the first memory devices, and not to the second memory devices, is not supported by the intrinsic record," especially because "the first and second memory devices of the claim are connected to a shared data line." (*Id.*) Netlist offers a baseball analogy to distinguish between transmitting a signal (throwing) and receiving (catching) a signal. (*See id.*)

Netlist also argues "[r]ead properly in the context of the claims, 'output or receive' are actions performed by the first memory devices 'in response to [] control signals' associated with a read or write command produced by the '[module] control circuit.'" (*Id.* (citing '907 patent at cls. 1, 16, 43, 58).) Netlist continues:

> The '907 Patent describes that the module control signals received by the memory devices may include "bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals" associated with each read or write command. Ex. 1, '907 Patent, at 10:24-34 (emphasis added); *see also id.* at FIGS. 3A-3D, 10:24-29, 10: 39-41, 10:8-12. As clearly disclosed, the chip-select signals select, or activate, the memory devices in the particular rank targeted for a specific read or write operation. Ex. 1, '907 Patent, at 10:24-34, 17:5-8.

(*Id.* at 26.)

Netlist then references the prosecution history and points to its own statement to the Examiner, explaining Figure 3B of the '907 patent, where the A memory devices output or receive data and C memory devices do not because the specification states, "'each specific [read or write]

operation is targeted to a specific one of rank A, B, C, or D.'" (*Id.* (citing CIMB, Ex. 4; '907 patent at Fig. 3B, 17:5-8).) Netlist also points to statements in the Examiner's first Notice of Allowance where "a single rank can 'accept the entire data width'" was recognized. (*Id.* at 27 (citing CIMB, Ex. 8).) In Netlist's view, "[t]his unequivocally confirms that first memory devices (*e.g.*, only Rank A) will receive the entire data width in response to being selected by a chip-select signal. This also confirms that the second memory devices (*e.g.*, only Rank C), residing on the same data line as Rank A, will not receive the entire data width." (*Id.*) Again, Netlist observes, in the second Notice of Allowance, "the Examiner stated that the 'non-selected memory devices' (*e.g.*, second memory devices having not received an active chip-select signal) will 'not output or receive data associated with the memory read or write command.'" (*Id.* at 27-28 (citing CIMB, Ex. 9).)

Netlist concludes "[t]his intrinsic evidence makes clear that a memory device's ability to output or receive data corresponds directly to which chip-select signal (active versus inactive) is sent from the module control circuit." (*Id.* at 28.) Netlist also disparages Respondents' and the Staff's interpretation because "the ability of the claimed memory devices to output or receive data is not connected to the operation of the buffer circuit. More striking still, the buffer circuit is not even referenced, to say nothing of encompassed, by this claim element." (*Id.*)

In its reply brief, Netlist confirms its view that Respondents and the Staff are improperly focused on the buffer circuit for this particular claim term so as to "force their 'fork in the road' layout into the claims where the claim language does not require or even suggest it." (*See* CRMB at 18-19.) Netlist also faults Respondents for rearranging claim excerpts to show "a causal relationship between the buffer circuits of claim 1[c] and the memory devices of claim 1[b] that is simply not present in the actual claim." (*Id.* at 19-20.) Netlist argues "[i]n the claim language, the transmission of data onto, or the acquisition of data from, the data lines performed by the memory

devices is unrelated to and not reliant on the internal structure or function of the buffer circuit." (*Id.* at 20.) Netlist states clearly, "the claimed buffer circuit element does not govern whether memory devices 'output or receive . . . data' in the context of the claims." (*Id.* at 21.)

Netlist then accuses Respondents' analysis of being a result-oriented approach. (*Id.*) Netlist contends the prosecution history disclaimer discussed by Respondents and the Staff is neither clear nor unequivocal, and not relevant to actions performed by the memory devices as opposed to the buffer circuit. (*Id.* at 22 (citing summary determination briefing).) Netlist again states clearly, "[t]here is no evidence in the intrinsic record, and neither Respondents nor Staff point to any, supporting an argument that the claimed buffer circuits somehow control whether and when the memory devices do or do not output data." (*Id.* (emphasis in original))

Netlist also refers to the '907 patent's "teach[ing] that only one rank of memory devices is targeted to 'output' data for a single read operation." (*Id.* at 23.) Netlist explains:

> Otherwise, a data collision would occur if two memory devices coupled to the same data line (*e.g.*, Rank A and Rank C) output data for the same operation. In a similar vein, two memory devices on the same data line that would both "receive" data during the same write operations would reduce available storage space by half, *e.g.*, all memory devices on the same data line would always store the exact same data.

(*Id.*) Netlist claims that Respondents' and the Staff's interpretation would result in a non-functioning memory module. (*Id.*)

Netlist then addresses Respondents' criticisms. Netlist contends that even though Figures 4A, 4B, and 5 do not show chip-select signal pathways, they are still there through these figures' disclosed relationships to Figures 3A and 3B, where the control pathways are shown. (*Id.* at 24 (citing '907 patent at 3:63-65, 13:48-56).) Netlist instructs "limiting claim scope to certain embodiments of the specification is error." (*Id.* (citing *Superguide Corp. v. DirecTV Enterprises,*

Inc., 358 F.3d 870, 875 (Fed. Cir. 2004); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).)

For the Staff, Netlist argues that it is not seeking to construe "output or receive" as "perform the memory read or write command." (*Id.* at 25.) Rather, according to Netlist, its position is that these terms "refer[] to the final stage of a read operation from a memory device in the selected rank, *i.e.*, transmitting data to the buffer circuit" and "the first stage of a write operation to a memory device in the selected rank, *i.e.*, acquiring data sent from the buffer circuit." (*Id.*)

Netlist concludes with a critique of Respondents and Staff for making attorney argument on how an artisan would understand DDR SDRAM device function, before continuing to offer its own technical explanation of chip-select signals. (*See id.* at 25-27.)

2. Respondents' Position

In their opening brief, Respondents argue this claim term "when read in the context of the surrounding claim language, as well as the specifications and prosecution histories discussed above—requires the 'fork in the road' layout. . . ." (RIMB at 58-59.) Respondents argue Netlist's construction is a mere replacement of "receive" with "acquire" and "output" with "transmit," which is improper. (*Id.* at 59.)

More specifically, Respondents state:

> The claim language "output or receive ... data" / "do not output or receive any data" requires the "fork in the road" layout because it requires that the ***second*** memory devices "do ***not*** … receive any data" when data is communicated to the ***first*** memory devices. Thus, in the annotated version of Figure 4A below, if 412**A** is the "first" memory device (as everyone agrees), then 412**C** cannot be the "second" memory device (as proposed by Netlist), because it is on the same data path as 412A and would ***receive*** all the same data being communicated to 412A. *See, e.g.*, Ex. 9, '907 patent, Ex. 9 at 17:67–18:2 ("data bits pass from the data lines 518 to the first

> terminal Y1 and on to the memory devices 412A, 412**C**") (emphasis added); *see also id.* at 11:38–:49, 15:39–:49, 15:65–16:16 (same).

(*Id.* at 59-60.)

Respondents then claim Netlist's expert "concedes that when two memory devices are on the same data path (*e.g.*, 412A and 412C), "both ranks of memory will *receive* the same data." (*Id.* at 60 (citing RIMB, Ex. 19 at 161:7-162:25; RIMB, Ex. 20 at 12).) Respondents add in footnote that command signals, or chip-select signals, then "tell one rank to ignore the received data, and tell the other rank to write the received data to memory." (*Id.* at n.8. (citing RIMB, Ex. 19 at 162:17-162:25; RIMB, Ex. 20 at 12).) Respondents thus reason that memory devices 412B and 412D, as shown in Figure 4A, must be the claimed "second memory devices" as they do not receive the data by virtue of being on the other side of the fork. (*See id.*) Respondents also observe how the '907 patent specification frequently describes ranks A and C as a "first group of memory devices" and ranks B and D as a "second group of memory devices." (*Id.* at 61-62 (citing '907 patent at 15:39-51, 15:65-16:16).)

Respondents then argue "the case law is clear that once claim scope is disclaimed in a parent application (here, the '185 patent), it cannot simply be reclaimed in a child patent (here, the '907 patent), even with different claim language." (*Id.* at 62-63 (citing *Hakim v. Cannon Avent Group, PLC*, 479 F.3d 1313, 1315-18 (Fed. Cir. 2007); *Bourns, Inc. v. United States*, 537 F.2d 486, 491-92 (Ct. Cl. 1976).) Respondents thus conclude that the disclaimers from the '185 patent, overcoming the Rajan reference, applies to the claims of the '907 patent as well. (*Id.* at 63.)

Next, Respondents discuss Netlist's reference to a "chip-select signal" as the mechanism that effectuates the "output or receive" limitation. (*Id.* at 63-65.) Respondents explain:

> Netlist's reasoning is incorrect as a technical matter and inconsistent with the claim language. The chip-select signal is one of the command signals used to tell a memory device to ***write*** data to memory,13 but it does not determine which memory device will

> ***receive*** the data in the first place, and the claim language is "receive" not "write." As explained above, it is the "buffer circuit" (416) which — in response to a write command to a given rank of memory —creates the "fork in the road" by selecting either the upper data path (452) or the lower data path (452), meaning ***all*** the memory devices on that data path will ***receive*** the data (even memory devices that do not ultimately ***write*** the data to memory, as Netlist's own expert concedes). *See supra* p. 60 & note 8.

(*Id.* at 64.) Respondents then claim the "while" language used in the limitation is not indicative of a causal a relationship between any chip-select signal and "output and receive." (*Id.*) Rather, "the word 'while' simply means that two things happen 'at the same time. . . .'" (*Id.* at 64-65 (citing RIMB, Ex. 23 at 1561; RIMB, Ex. 22 at 1347).)

In their reply brief, Respondents compare Netlist's acknowledgment that "'swapping a claim term for its synonym is error in claim construction'" (RRMB at 16 (citing CIMB at 13)) with their desire to replace "output" with "transmit" and "receive" with "acquire" (*id.*). Respondents argue Netlist goes a step further—construing their own construction so that "acquiring" actually means "the first stage of a write operation." (*Id.* (citing CIMB at 24).) Respondents contend this is improper as the specification uses "write" and never "receive" to talk about writing data to memory. (*Id.* at 16-17 (citing '907 patent at 14:62-15:9, 16:17-21).)

Respondents then repeat their position that when memory devices are on the same data path, they will both "receive" the same data. (*See id.* at 18-22 (citing '907 patent at 11:39-44, 15:44-46, 16:8-11, 17:67-18:2; RIMB, Ex. 20 at 12; RIMB, Ex. 19 at 161:7-18, 162:17-25).) Respondents also fault Netlist for not addressing how, in the example of Figure 4A, memory device 412C does not "receive" any data (*id.* at 22), and for suggesting the prosecution history addressed the meaning of the word "receive" when, in actuality, it does not appear in that history (*id.* at 23 (referring to CIMB, Ex. 4 at 28)). Respondents also point to the notices of allowance in the '907 prosecution history, and highlight how they include "different buffers are enabled and

disabled" or "not just prevented from passing [data] through the interface" language. (*Id.* at 24-25 (citing RIMB, Ex. 11 at 396, 440, 457-458).) Respondents reason this language represents a "fork in the road" layout. (*Id.* at 25.) Respondents add "this was the same examiner who had rejected the '185 claims in light of the 'straight line' configuration found in Rajan" and how also rejected one-time dependent claim 36 (discussed *supra*) for lack of written description. (*Id.* at 25-26.) In Respondents' view "Netlist acquiesced to both of those rejections, and never asked the examiner to revisit those rejections, estopping Netlist from trying to recapture that claim scope now." (*Id.* at 26 (citing *UCB, Inc. v. Yeda Res. & Dev. Co.*, 837 F.3d 1256, 12621 (Fed. Cir. 2016); *Hakim*, 479 F.3d at 1318).)

3. Staff's Position

In its opening brief, the Staff explains its view that Netlist "seeks to construe the claim such that it is satisfied so long as the read/write command is performed with the first devices, as opposed to the second devices, via the chip-select signal." (SIMB at 41.) The Staff views this approach as "disregarding the express limitation directed to the second memory devices." (*Id.*) To the contrary, the Staff argues the limitation "is plainly understood to prohibit any of the data from the read or write command, which is intended for the selected first memory devices, from also being transmitted to the second memory devices" under its ordinary meaning. (*Id.* at 42.)

The Staff also references its discussion of the first claim term, above, to again argue "the ['907 patent claims] were amended in the November 2106 amendment to remove language directed to performance of the read or write command, and replaced with the current disputed 'do not . . . receive any data' claim language." (*Id.* at 42-43 (citing "FH at 403").) "Thus," the Staff reasons, "the term cannot be construed to be the same as the second memory devices 'not performing a read or write command.'" (*Id.* at 43.)

The Staff then considers the prior art, including that described in the '907 patent specification, and argues a person of ordinary skill would understand "do not output or receive" as requiring more than the merely known chip-select signals. (*Id.*) The Staff adds, on a technical ground, that chip-select signals do not inhibit communication. (*Id.*)

In its reply brief, and relevant to this claim term, the Staff explains that "a person of ordinary skill in the art would interpret the totality of the claim as *not encompassing* a memory module that allows the memory controller to concurrently connect and communicate to *both* the first memory devices and second memory devices." (SRMB at 10-11 (emphasis in original).) The Staff adds that Netlist's interpretation is inconsistent with the electrical isolation feature described in the specification as new and advantageous. (*Id.* at 13 (citing '907 patent at 14:54-62, 11:48-54).) More specifically, the Staff argues:

> Complainant's claim interpretation combines a prior art memory module that has two memory devices on shared data lines, and a prior art module control circuit that sends chip-select signals to targeted memory devices to perform the read or write operation. *See* CIB at 20. Complainant argues that there is no further limitation on the memory buffer, other than that the memory buffer permit transmission of data to the memory devices. *See* CIB at 29.

(SRMB at 17-18.) This, however and according to the Staff, is embodied exactly in the prior art described in the '907 patent specification and used to reject the parent '185 patent during its prosecution. (*See id.* at 17-21 (citing, *inter alia*, '907 patent at 7:19-25, Figs. 2C, 2D; CIMB at 13 (stating "[a]s a result, the '907 patent claims do not require this 'selective' functionality on the part of the buffer circuits")).)

4. Analysis

To begin, this term is at the heart of the larger dispute between the parties as to whether the asserted claims of the '907 patent require a "fork in the road" or "straight line" arrangement of memory devices. The parties briefed "output or receive / do not output or receive" as Term No. 2,

but I address it first because its resolution impacts much of the remaining '907 patent analysis. In the end, I agree with Netlist's interpretation even though I find it may not match the plain and ordinary meaning of "output" and "receive." I also find that under Netlist's interpretation, a central aspect of the '907 patent's specification (enabling data communication between the memory controller and at least one first memory device while isolating at least one second memory device from the memory controller") may be absent from several of the claimed embodiments. Nevertheless, I find the structure and language of the '907 patent's claims themselves, and other practical problems with Respondents' construction, favor Netlist's version of "output or receive / do not output or receive" as not involving electrical isolation; *i.e.*, not involving Respondents' "fork in the road."

First, as Netlist acknowledges, the '907 patent does not expressly define what is meant by "output" or "receive" (CIMB at 24), and it certainly does not disclose or discuss the technical details Netlist includes in its briefing to explain why "output" means "transmit" and why "receive" means "acquire" (CRMB at 25-27 (discussing, *e.g.*, data "latched," I/O portions of memory devices, two stages of a write operation).) Indeed, the term "output" is used in the '907 patent in a variety of contexts, as is "receive." (*See, e.g.*, '907 patent at 15:65-16:16 (tristate buffers output), 16:17-35 (multiplexer output), 16:36-55 (output memory buffer of a memory device and system memory controller), cl. 9 (input/output connections on a module control circuit, cl. 40 (output buffers), Abstract (control circuit configured to receive control/address information), 2:25-58 (data transmission circuits receive module control signals), 4:39-61 (register receives control lines), 14:6-24 (data transmission circuits receive data bits), 15:65-16 (control logic circuitry receives enable signals), 16:17-35 (data signals received from memory devices at terminals of data transmission circuit).) These varied contexts support the idea that the '907 patent uses "output" and "receive" according to general, plain and ordinary meanings.

Netlist, on the other hand, claims "output" and "receive," in the context of memory devices, refer to the effect of certain "chip-select signals" (CIMB at 28 ("[t]his intrinsic evidence makes clear that a memory device's ability to output or receive data corresponds directly to which chip-select signal (active versus inactive) is sent from the module control circuit")), but these signals are mentioned without much detail in the '907 patent specification:

> During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density that can be incorporated in each memory module.

('907 patent at 1:51-58);

> Another method increases the addressable memory space without extensive alteration of the software or hardware of an existing electronics system. This method combines chip-select signals with an address signal to increase the number of physically addressable memory spaces (*e.g.*, by a factor of 2, by a factor of 4, by a factor of 8, or by other factors as well).

(*id.* at 4:11-17);

> The control circuit 430, 430′ of certain embodiments is configurable to be operatively coupled to control lines 440, 440′ to receive control signals (*e.g.*, bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller 420, 420′.
>
> . . . .
>
> The control signals indicate, for example, the direction of data flow, that is, to or from the memory devices 412, 412′. The control circuit 430, 430′ may produce additional chip-select signals or output enable signals based on address decoding. Examples of circuits which can serve as the control circuit 430, 430′ are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein

(*id.* at 10:24-44). None of these excerpts discuss how chip-select signals would cause a memory device to "output" or "transmit," "receive" or "acquire" data associated with a read or write

command from the system controller as Netlist contends. The first excerpt simply states chip-select signals "select" or "activate" ranks of memory devices. The other excerpts mention chip-select signals as increasing addressable space or controlling direction of data flow.

Even the prior patents, U.S. Patent Nos. 7,289,386 (the "'386 patent") and 7,532,537 (the "'537 patent"), incorporated by reference into the '907 patent on the subject of chip-select signals (*see* '907 patent at 10:41-44) do not explicitly assign Netlist's proffered meaning to "output" and "receive." They, like the '907 patent, speak generally of chip-select signals as "selecting" or "activating" memory devices, and not with the level of detail Netlist describes. (*Compare* '386 patent at 2:34-42, 8:1-64 *with* CRMB at 25-27.)

Non-asserted claims of the '907 patent, however, shed light on the meaning of "output" and "receive." Specifically, previously-asserted independent claim 30 uses slightly different language than currently-asserted independent claims 1, 16, 43, and 58. The relevant portion reads:

> memory devices coupled to the module control circuit, the memory devices including first memory devices *responding to the first output address and control signals by receiving* each N-bit wide data signal associated with the first write command, and second memory devices *responding to the second output address and control signals by receiving* each N-bit wide data signal associated with the second write command;

('907 patent at cl. 30 (emphasis added).) The phrase "memory devices responding . . . by receiving" strongly indicates that "receiving" is something the memory devices do rather than a result of some other external act. (*See* CIMB at 28; CRMB at 18-20.) Netlist's chip-select explanation matches this language while Respondents' "fork in the road" interpretation does not. It is undisputed that the "fork in the road" effect is due to the action of buffer circuits, or data transmission circuits, *apart* from the memory devices. (*See* CIMB at 13-14; RIMB at 35-38.) I find here especially—the claims' own use of the term is highly instructive, perhaps the most instructive, piece of intrinsic evidence on the term's meaning. *Phillips*, 415 F.3d at 1314.

Certain dependent claims in the '907 patent also support Netlist's interpretation over Respondents'. For example, claims 2, 4, and 10 depend from claim 1 and read:

> 2. The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.

('907 patent at cl. 2);

> 4. The memory module of claim 3, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.

(*id.* at cl. 4);

> 10. The memory module of claim 1, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.

(*id.* at cl. 10 (*see also id.* at cls. 21, 22)). Each of these claims elaborates on the "first module control signals" introduced in claim 1 and which cause the first and second memory devices to "output or receive / do not output or receive" data. (*Id.* at cl. 1.) Notably, each of these claims focuses on chip-select signals which the '386 and '537 patents (incorporated by reference into the '907 patent) teach are sent to the memory devices and the memory devices respond to—not the buffer circuits. (*See* '386 patent at Fig. 1A, 7:45-8:45; '537 patent at Fig. 9A, 16:59-18:3.) Respondents confirm the connection between the "first module control signals" (which controls the "output or receive / do not output or receive") and chip-select signals through their argument on the claim term "produce." (*See* RIMB at 25-29.)

Other limitations within claims 1 and 16 are also hard to reconcile with Respondents' "fork in the road." Specifically, claims 1 and 16's use of the "N = M x *n*" formula for overall data bandwidth results in *n* representing an integer value. As discussed further below, claims 1 and 16 use *n* in additional ways, including through the following language:

> each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,

('907 patent at cl. 1);

> each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,

(*id.* at cl. 16). Both of these limitations recite the first and second memory devices being coupled to the buffer circuit through the same set of *n* module data lines. This means a set of 2, 4, 6, 8, etc. module data lines.

In their briefing, Respondents at one point take the position that *n* is not an integer for the number of data lines, but as an integer for the number of bits each data line carries; *i.e.*, "a set of *n* module data lines" means "a set of *8-bit* module data lines." (RIMB at 42, n.7; RRMB at 12-13.) Respondents appear to draw this interpretation from a moment in the '907 patent prosecution history, where the applicant characterized support for the then-new claim language as follows:

Cl #	Amendment	Support
4 12	each respective buffer circuit being coupled to a respective set of the *M* sets of *n* data lines, to respective one or more of the first memory	As shown in FIGS. 4A and 4B, memory device 412A (or memory devices $412A_1$ and $412A_2$) (respective one or more of the first memory devices) and memory device
	devices via a set of *n* module data lines, and to respective one or more of the second memory devices via the set of *n* module data lines	412C (or memory devices $412C_1$ and $412C_2$) (respective one or more of the second memory devices) are coupled to the buffer circuit 416 via a same set of 8-bit data lines 452.

(RRMB at 12 (citing RIMB at 11).)

I disagree this single statement should result in Respondents' interpretation of *n* for several reasons. First, Respondents themselves argue "the Federal Circuit has emphasized *en banc* that an obscure statement like this during prosecution 'often lacks the clarity of the specification and thus is less useful for claim construction purposes.'" (RIMB at 70 (citing *Phillips*, 415 F.3d at 1317); RRMB at 13.) Second, the preamble introducing the *n* value does so as a number of "data lines" ('907 patent at cl. 1 ("A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines . . .").) Third, at a different time Respondents do actually interpret the patent's specification as using 8 data lines to handle 8-bits of communication—not just one data line:

> [Figures 4A and 4B of the '907 patent] have the same "telltale 'fork in the road' layout": **8 data lines** come in to the buffer circuit 416, and 16 data lines come out of the buffer circuit 416, **with 8 of the 16 outgoing data lines comprising "path A"** that connects to the "first" memory devices 412A and 412C (or 412A1/412A2 and 412C1/412C2 in Figure 4B), and **the other 8 outgoing data lines comprising "path B"** that connects to the "second" memory devices 412B and 412D (or 412B1/412B2 and 412D1/412D2 in Figure 4B). *See id.* at 13:28–:29, 15:39–:51, 15:65–16:16.

(RIMB at 42, n.7 (emphasis added).) Fourth, the '907 patent specification also teaches a certain 1-bit to 1 data line correspondence, so that a buffer circuit which handles 8-bits would have 8 data lines:

> FIG. 5 schematically illustrates an example data transmission circuit 416 compatible with certain embodiments described herein. In one embodiment, the data transmission circuits 416 includes control logic circuitry 502 used to control the various components of the data transmission circuit 416, which may include one or more buffers, one or more switches, and one or more multiplexers among other components. **The illustrated embodiment of FIG. 5 is 1-bit wide and switches a single data line 518 between the memory controller 420 and the memory devices 412. In other embodiments, the data transmission circuit 416 may be multiple bits wide, for example, 8 bits, and switch a corresponding number of data lines 518.** In a multiple bit wide embodiment, the control logic circuitry 502 may be shared over the multiple bits.

('907 patent at 15:17-31 (emphasis added).)

Thus, I find it is appropriate to treat the first and second memory devices as both coupled to the same set of module data lines, where there are *n* number of module data lines in the set. This means the first and second memory devices cannot be on different respective sides of a "fork in the road" and must "output or receive / do not output or receive" according to a different mechanism than the "fork in the road."

Lastly, I find the overall organization of the '907 patent claims is suggestive more of Netlist's construction of "output or receive / do not output or receive" than Respondents'. As Netlist explains, "[e]ach of the independent claims 1, 16, 30, 43, 53, and 58 follows a similar pattern: a clause introducing the module control circuit; then the memory devices with "output or receive / do not output or receive;" then a buffer circuit description and functionality; the memory device and buffer circuit position information on the PCB itself. (*See* '907 patent at cl. 1, 16, 30, 43, 48, 53.) In this pattern, the "output or receive / do not output or receive" language appears before the buffer circuits (which indisputably contain the "fork in the road") are even introduced.

In Netlist's words, "[m]ore striking still, the buffer circuit is not even referenced, to say nothing of encompassed, by this claim element." (CIMB at 28.) I find this organization is by no means dispositive but likely to suggest to a person of ordinary skill that the "output or receive / do not output or receive" function is not related to the buffer circuits.

With that said, Respondents' briefing is persuasive still in that it revolves around what would be a plain and ordinary meaning of "receive"—a circuit element "receives" a signal when that signal reaches one of the circuit element's inputs. This is supported, in part, by those '907 patent excerpts cited above that use "receive" in a variety of contexts.

Respondents have also shown an obvious importance of a "fork in the road" functionality within the '907 patent family and a credible account of how that feature came about. (RIMB at 21-23, 31-57.) This history, however, should not override the meaning of "receive" as used it is used in the claims at-hand. *See Schoenhaus v. Genesco, Inc.*, 440 F.3d 1354, 1356–57 (Fed. Cir. 2006) ("In other words, the question before this court is not what the invention covers, but whether the claim term "orthotic device", as used in the patent, . . . refer only to a removable orthotic insert or the immovable insert portion of a shoe, or more generally to a shoe built to have the shape of the interior of the insert."). Indeed, Respondents support their central argument—that the claimed "first memory devices" and "second memory devices" must be on different data paths thereby justifying their interpretation of "receive"—by referring to the embodiments shown in the figures of the '907 patent and not on the actual claim language. (*See, e.g.*, RIMB at 58-62 (not discussing how "output" and "receive" are used within the claims); RRMB at 16-17 (stating "receive data" does not mean "write data," based off of specification and JEDEC usage).)

Respondents, and the Staff, also argue that statements made during the prosecution of the parent '185 patent, concerning the Rajan reference, amount to claim scope disclaimer and must also apply to the '907 patent. (*See* RIMB at 48-53, 62-63) The statements, however, related to the

meaning of "selective allowance" and "selective isolation" as *claimed* in the '185 patent. Even if these statements qualified as disclaimer, the terms so disclaimed "selective allowance" and "selective isolation" simply do not appear in the claims of the '907 patent. It is thus difficult to see why the alleged disclaimer would apply to "output or receive / do not output or receive." It is similarly difficult to apply those cases promoted by Respondents and the Staff requiring an applicant to ask an Examiner to revisit earlier rejections, such as *Hakim*.

Respondents also argue against Netlist's chip-select signal theory on technical grounds. In short, Respondents contend that chip-select signals do not *by themselves* control if a memory device will read or write data—there are additional command signals RAS, CAS, and WE which, through their 0/1 combinations instruct the memory device to READ, WRITE, or NO OPERATION. (RIMB at 64.) This distinction is well received, and finds support not only in the extrinsic evidence of the JEDEC standard but also in the intrinsic evidence of the '386 and '537 patents incorporated by reference into the '907 patent. Specifically, these patents disclose:

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. Cs_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

. . . .

The "Command" column of Table 1 represents the various commands that a memory device (*e.g.*, a DRAM device) can

execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (*e.g.*, state 4 of Table 1). In such embodiments, the command signal (*e.g.*, read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (*e.g.*, state 6 of Table 1). In such embodiments, the command signal (*e.g.*, refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

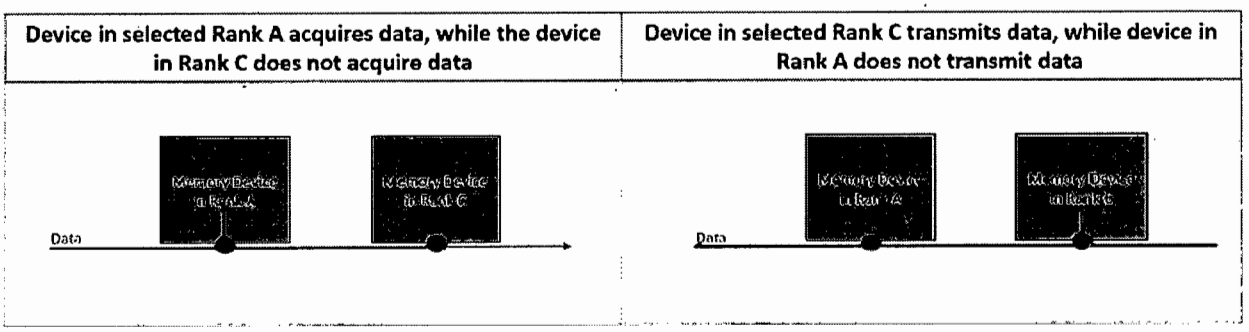
Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

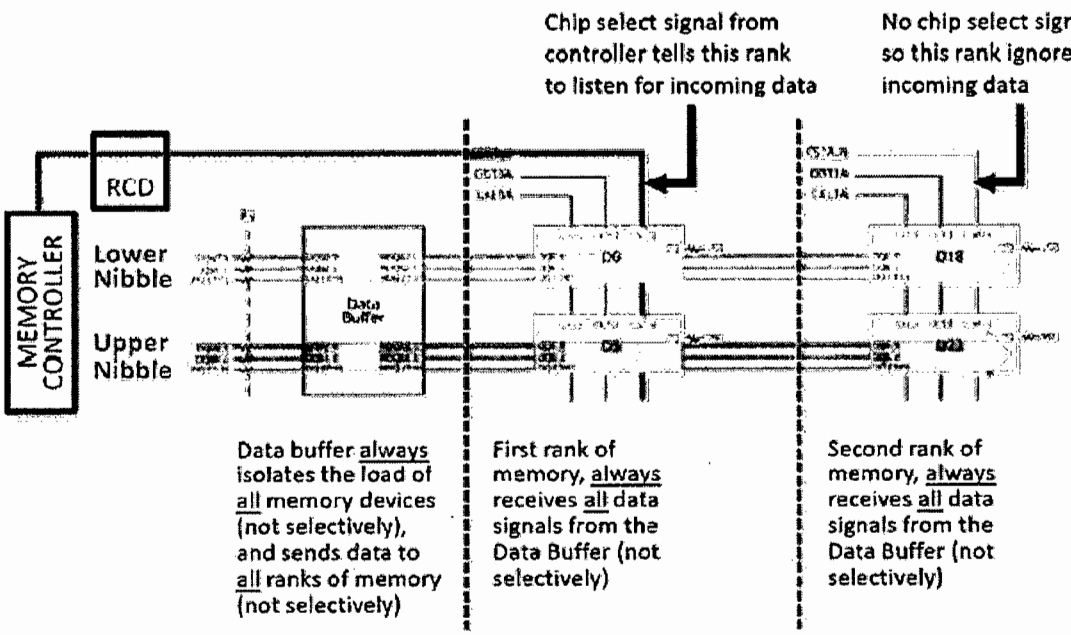
TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

('386 patent at 8:1-9:17.) This distinction, however, only serves to show that "first module control signals" *as claimed* should not be limited to chip-select signals, but would include any or all command signals that fit the language of "response to the first module control signals, the first memory devices output or receive each N-bit wide data signal." This is completely consistent with Respondents' observation that the claim language "while" in this limitation "simply means two things happen 'at the same time.'" (RIMB at 64-65; RRMB at 23.) To avoid any doubt, I do not in this Markman order construe "first module control signals" to be limited to chip-select signals, or any other particular combination of CS, RAS, CAS, WE, Command, etc. signals.

Finally, with respect to Netlist's baseball analogy, I agree with Respondents that it is not accurate (RRMB at 22-23) but on different grounds. In baseball, if a ball thrown from the catcher to the pitcher is not caught—the ball keeps going (*i.e.* continues traveling along a data path to another memory device or other circuit component). To the contrary, here, Netlist admits that despite their characterization of their interpretation as "straight line" and both parties' use of figures such as the following:





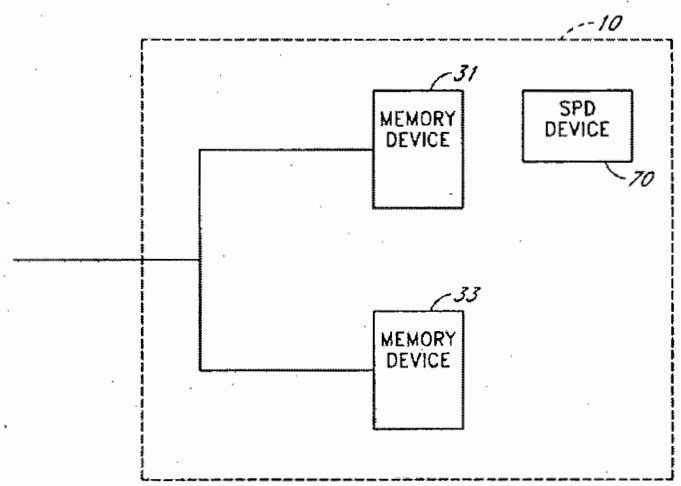
(CRMB at 27; RIMB at 52), the first and second memory devices are not actually connected in series so that any data not received keeps traveling. Netlist explains:

> When memory chips from multiple ranks share the same bidirectional data lines, this forms what is known in the art as a "multi-drop" data bus. The simplified diagram in Fig. 3A above is

> commonly used to depict this type of connection where, for example, DRAM dice from rank A and rank C are coupled to the same data lines. Although lines are diagrammed through DRAMs in rank A to DRAMs in rank C, rank A does not actually "feed" rank C.

(*Id.* at 25.) Indeed, I expect Netlist would not dispute the accuracy of an arrangement where memory devices are arranged in parallel and each memory device is effectively a backstop on its respective data line; as shown, for example, in Figure 1C of the '386 patent or in the inventor declaration regarding conception submitted during the '907 patent's prosecution:

FIG. 1C



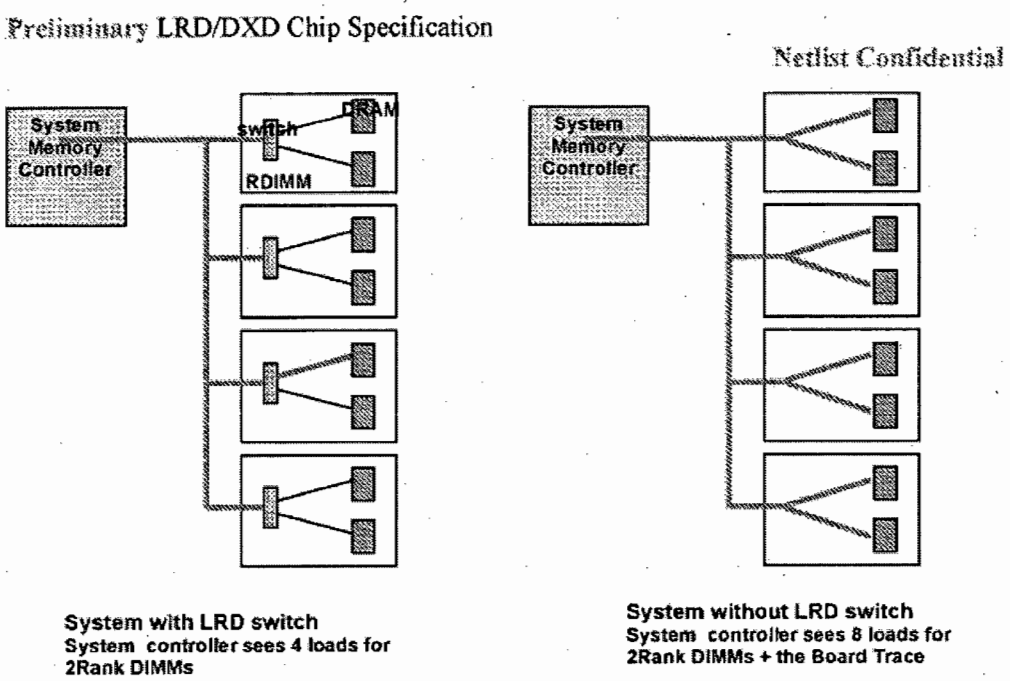


Figure 10: LRD Configuration

('386 patent at Fig. 1C; RIMB, Ex. 11 at 239.) Thus, a better analogy might be a dart (data) thrown at a dart board (memory device) which will either stick (memory device configured to receive) or bounce off and fall dead (memory device configured to not receive).

The Staff's arguments largely mirror the Respondents' in that they rely on an interpretation that matches what would be a plain and ordinary meaning of "receive" but does not match how "receive" is used with respect to memory devices in the actual claims of the '907 patent (*e.g.*, claim 30). The Staff also focuses heavily on the alleged prosecution disclaimer related to the '185 patent claims, which, again, involved the term "selectively" which does not appear in the '907 patent claims. With respect to the Staff's analysis of the '907 patent's prosecution history, and especially that discussion of cancelled claims reciting "same set of terminals," (SIMB at 27-29), I find Netlist's position on the import of this cancellation (CRMB at 14-18) to be more persuasive.

Thus, based on how the '907 patent claims themselves employ the terms "output" and, especially, "receive," I do not understand this limitation to invoke Respondents "fork in the road"

feature of electrical isolation—despite the patent's and its family members' primary focus on that feature in their specifications. *Superguide*, 358 F.3d at 875 ("The written description, however, is not a substitute for, nor can it be used to rewrite, the chosen claim language.")). Consequently, I construe "output or receive / do not output or receive" to mean "transmit or acquire / do not transmit or acquire."

B. "[M buffer circuits / each respective buffer circuit] being [operatively] coupled to . . . [a] respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines"

The term "[M buffer circuits / each respective buffer circuit] being [operatively] coupled to . . . [a] respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines" appears in claims 1 and 16 of the '907 patent. These claims read:

> 1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
>
> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
>
> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
>
> M buffer circuits each configured to receive the second module control signals from the module control circuit, **each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data**

lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

....

16. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or

receive any data associated with the memory read or write command;

a plurality of buffer circuits configured to receive the second module control signals from the control circuit, **each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines**, the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines, wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

('907 patent at cls. 1, 16 (emphasis added).)

The constructions proposed by the parties for these terms are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
"each buffer circuit is coupled to one or more DRAM devices in a first rank and one or more DRAM	Plain and ordinary meaning, with the understanding that, when considered with the surrounding language of the	"buffer circuit including logic …allowing communication" should be given the same

devices in a second rank via the same set of (N/M)-module data lines, wherein a rank is a collection of DRAM devices on the memory module that together transmit or acquire N bits of data during a read or write operation"	respective claim, the resulting physical arrangement of the elements of the claim (when given their plain and ordinary meaning) is a "fork in the road" layout	construction as the 1023 investigation because the same disclaimer applies to the '907 patent, otherwise the claim lacks written description support "Coupled to..." – Plain and ordinary meaning, coupled to two separate memory devices, including a selected memory devices (*e.g.* selected per claimed read/write command from memory controller) on shared first data lines (*e.g.* part of the "set of n module data lines" with a first terminal (*i.e.* Y1 and 452_1) and non-selected memory devices on second shared data lines (*e.g.* remainder of the set of n module data lines) with a separate second terminal "a set of n module data lines" - the "set" must include separate data lines for first and second memory devices (*i.e.* pair of n module data lines); otherwise the claim term is indefinite

1. Netlist's Position

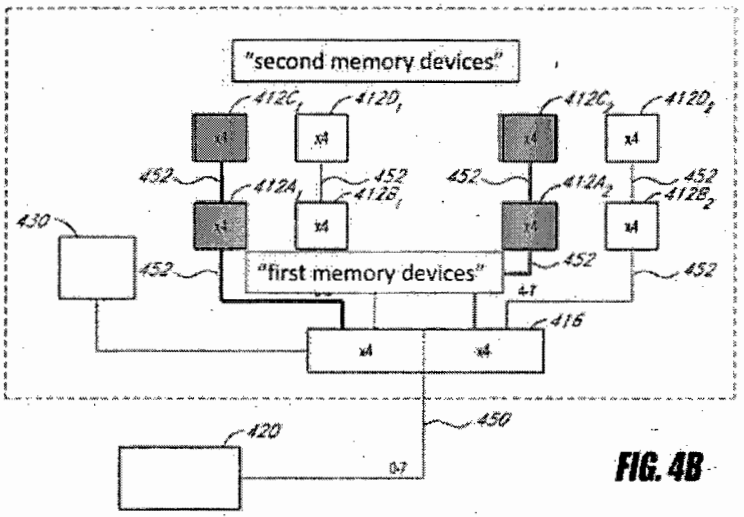
In its opening brief, Netlist claims it construes this term according to its plain meaning and there is no support in the intrinsic record for Respondents' "fork in the road" interpretation. (CIMB at 13.) Netlist contends the "fork in the road" concept comes from the claim term "selectively" which appears in the '185 patent (at issue in the 1023 Investigation, and parent to the '907 patent), but does not appear "expressly or by implication" in the '907 patent. (*Id.*)

Netlist also argues Respondents' and Staff's interpretation is inconsistent with principles of antecedent basis as the "claimed first and second memory devices are connected to a buffer circuit via the same set of the claimed module data lines." (*See id.* at 16, 18 (emphasis in original).) Netlist argues "[t]his embodiment is clearly supported by the specification that consistently describes and depicts memory devices in a first rank (*e.g.*, rank A) and memory in a second rank (*e.g.*, rank C) coupled to a buffer circuit via the same set of n data lines." (*Id.* at 18 (citing '907 patent at Figs. 3A-3C, 4A-4B, 9:35-58, 11:14-26, 13:27-34, 13:48-59, 14:25-49).)

Netlist continues, "[o]ther requirements of claims 1 and 16 describing the first and second memory devices are consistent with the specification's description of memory devices in first and second rank." (*Id.* (citing '907 patent at cls. 1, 16, 1:36-50, 17:5-8).) Netlist also points to a table from the '907 patent's prosecution history, where the Applicant linked memory devices A to "first memory devices" and memory devices C to "second memory devices" to show support for a claim amendment (*id.* at 18-19 (citing CIMB, Ex. 4 at 28-29)), which I reproduce below:

Cl #	Amendment	Support
4 12	each respective buffer circuit being coupled to a respective set of the *M* sets of *n* data lines, to respective one or more of the first memory devices via a set of *n* module data lines, and to respective one or more of the second memory devices via the set of *n* module data lines	As shown in FIGS. 4A and 4B, memory device 412A (or memory devices $412A_1$ and $412A_2$) (respective one or more of the first memory devices) and memory device 412C (or memory devices $412C_1$ and $412C_2$) (respective one or more of the second memory devices) are coupled to the buffer circuit 416 via a same set of 8-bit data lines 452.

(CIMB, Ex. 4 at 28-29.) Netlist provides the following annotated Figure 4B of the '907 patent to explain the Applicant's statement:



(CIMB at 20.) Netlist contends that in this figure, and Figure 4A preceding it, the claimed "M sets of n data lines" refers to a situation where n=8. (*Id.*) Specifically, Netlist states:

> Each of these figures shows n=8 data lines connecting the buffer circuit 416 to the system memory controller 420. Each figure also shows a total of n=8 module data lines connecting the buffer circuit to the memory devices in Rank A and to the memory devices in Rank C. The primary difference between the two illustrated embodiments is that in Figure 4A, the memory devices 412 are 8 bits wide, and all 8 module data lines connected to Ranks A and C are connected to a single memory device in each of those ranks, while in Figure 4B, the memory devices 42 are only 4 bits wide, meaning that the total of n=8 bits are split between the 4 module data lines that connect $412A_1$ to $412C_1$ and the 4 module data lines that connect to $412A_2$ and $412C_2$.

(*Id.* at 20-21.)

Netlist then presents Respondents' argument that the first and second memory devices are not coupled to the buffer circuit by the same module data lines, along with the following figure annotated by Respondents:

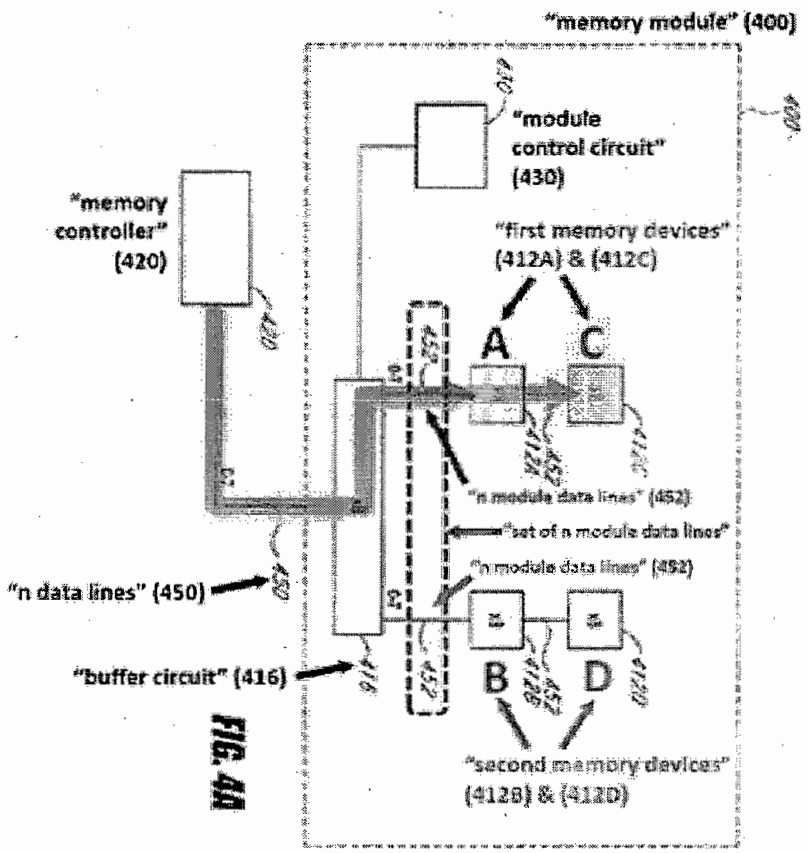


FIG. 4A

(*Id.* at 21-22. (citing CIMB, Ex. 5, App'x A at 1-2).) Netlist argues this cannot be right because Respondents' red dotted box of "set of n module data lines" includes 16 module data lines, not 8, thereby "ignor[ing] the requirement that the claimed corresponding claimed set of module data lines on the other side of the buffer circuit must also be n bits wide." (*Id.* at 22.)

Netlist then frames the Staff as rewriting the claim to read "set of [2x] n module data lines" which, according to Netlist, is not supported by the claims, the specification, or Netlist's explanation of this very limitation during prosecution." Netlist concludes:

> The relationship between the M, N, and n values is consistent through the entirety of the claims, and is supported by specification. *See e.g.*, Ex. 1, '907 Patent at 3A-3B, 4A-4B, 1:36-50, 5:46-50, 13:48-56, 14:25-49, 17:5-8. Changing any of the values required by the plain language of the claim does violence to the first principle that claims are presumed to mean what they say.

(*Id.* at 23.)

In its reply brief, Netlist repeats its position that Respondents are trying to inject their "fork in the road" layout where it does not belong. (CRMB at 9-10.) Netlist argues, with respect to Figures 4A and 4B, that treating the claimed "first memory devices" as 412A and 412C, and "second memory devices" as 412B and 412B, necessitates the "the 'set' of module data lines must contain a total of 2n module data lines." (*Id.* at 10.) Netlist, again, asserts this is contrary to the specification and plain language of the claims. (*See id.* at 10-12.) Netlist also sees a contradiction between Respondents' interpretation and claim 16 "which refers back to 'the set of n module data lines' . . . requires that the buffer circuit cause communication between what Respondents now identify as two differently sized collections of data lines." (*Id.* at 12 (emphasis in original).)

Netlist then addresses the Staff's position that, during prosecution, the Applicant disclaimed claim scope through the cancellation of claim language directed to "groups" of memory devices. (*Id.* at 14.) To the contrary, Netlist argues it canceled the identified claim "without substantive discussion" and "thus did not address, much less acquiesce to, any of the Examiner's statements in the rejection or any interpretation of the '907 patent's independent or dependent claims." (*Id.* at 15. (citing CIMB, Ex. 4).) Moreover, according to Netlist, the cancelled claim, rejected by the Examiner for lack of written description, required first and second groups of memory devices be coupled to a same set of terminals on a buffer circuit. (*See id.* at 16 (citing CRMB, Exs. 26, 27).) Netlist contends the Examiner was acting to exclude a claim directed to the following embodiment—a version of Figure 4A modified by Netlist:

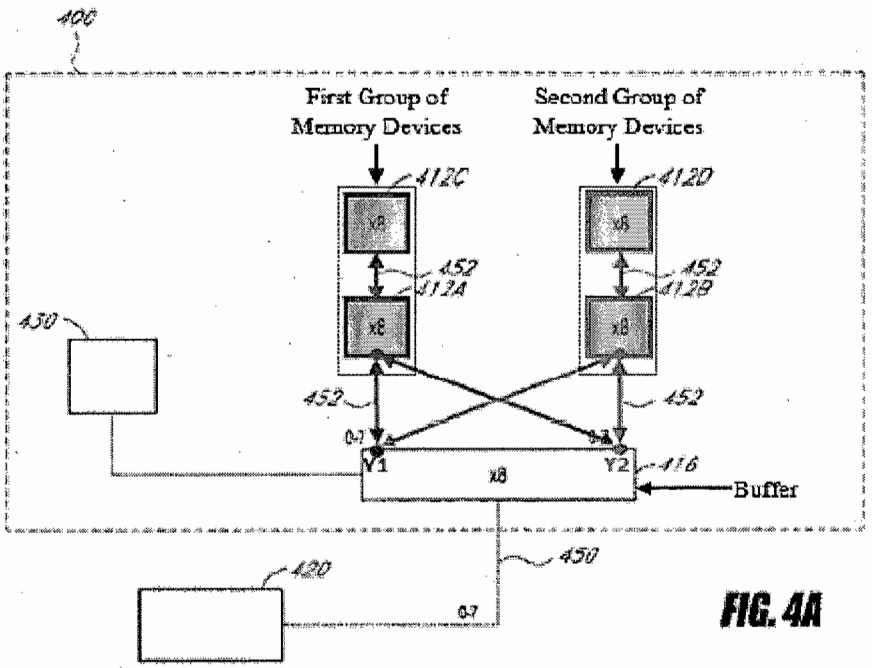


FIG. 4A

(CRMB at 17.) Netlist states clearly, "[t]hus, the examiner's rejection was specifically tied to the recitation of multiple 'groups' of memory devices all coupled to 'a same set of terminals' of a buffer circuit." (*Id.*) Netlist claims its removal of "groups" of memory devices and "same set of terminals" from the claims during prosecution solved this problem. (*Id.* (citing CIMB, Ex. 4).)

2. Respondents' Position

In their opening brief, Respondents summarize the dispute over this and related claim terms as:

> The parties do not appear to seriously dispute the plain and ordinary meaning of any particular word in the claims by itself — other than the term "produc[e/ing]" discussed above — but the parties vigorously dispute what each claim means as a whole when you put the 500+ words of the claim together.

(RIMB at 33.)

Regarding evidence intrinsic to the '907 patent, Respondents begin with the prosecution history. (*Id.* at 53.) Respondents argue "[t]he prosecution history of the '907 patent—like the prosecution history of the parent '185 patent and the grandparent '870 patent – shows that the

claimed invention is limited to a 'fork in the road' layout." Respondents point to the '907 patent Applicant's filing of a terminal disclaimer to evidence "a strong clue" the '907 patent lacked a patentable distinction over the prior '185 and '870 patents. (*Id.* at 54 (citing *SimpleAir, Inc. v. Google LLC*, 2018 WL 1247003 at *6 (Fed. Cir. 2018).) Respondents then point to the since-cancelled claim 36 which, in Respondents' view, was directed to a "straight line embodiment" in order to capture Respondents' accused products. (*Id.* (citing RIMB, Ex. 11 at 371).) Respondents observe, as described in Netlist's brief, that the rejection was for lack of written description of such an embodiment. (*Id.*)

Following the notice of allowance, Respondents note the Applicant further amended the claims and argue the amendments look to the "fork in the road" approach described in the specification for support, using the following table:

Amendment	Support
the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective *n*-bit section of the each *N*-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the *M* sets of *n* data lines and via the set of *n* module data lines	As shown in FIGS. 5 and 6, and discussed in paragraphs [0065]-[0072], the logic 502 generates control signals Enable Y1, Enable Y2, Enable D, and Select Y1/Y2 in response to the module control signals (e.g., Module Controls D->Y1), to allow data D->Y1 to be communicated between the memory controller and the respective one or more of the first memory devices. As shown in FIG. 4A or 4B, each buffer circuit 416 communicates an 8-bit section of each N-bit wide data signal.

(*Id.* at 56 (citing RIMB, Ex. 11 at 430).) Respondents add that the paragraphs cited as support in the above excerpt, [0065]-[0072], also discuss the "fork in the road" concept. (*Id.* (citing RIMB, Ex. 11 at 31-32; '907 patent at 17:63-18:2, 18:10-16).)

For the particular claim limitation at issue here, Respondents argue it requires a "fork in the road layout"—when read in context with the surrounding claim language and other intrinsic

evidence. (*See id.* at 66.) Respondents dismiss Netlist's "straight line" approach for several reasons. In particular, Respondents argue the language "'a set of' permits *multiple* elements to be in the set (*e.g.*, *two* 'n module data lines' (452) can be in the set. . . .)" (*Id.* (referring to *SanDisk Corp. v. Kingston Tech. Co.*, 695 F.3d 1348, 1360 (Fed. Cir. 2012)) (emphasis in original).)

Respondents then point to the '907 patent specification to argue the claimed "second memory device" is 412B, as in Figure 4A, rather than 412C, as in Netlist's interpretation. (*Id.* at 68 (citing '907 patent at 15:39-51, 15:65-16:16).) Respondents also contend Netlist's interpretation excludes the preferred embodiment of the patent, which is "rarely, if ever, correct." (*Id.* (citing *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013).) According to Respondents:

> In the '907 patent, the "n data lines" are identified as 450, and the "n module data lines" are identified as 452, as shown in the annotated version of Figure 4A above. *See also* '907 patent, Ex. 9 at 14:44–:49. Importantly, as shown in the annotated version of Figure 4A, there are ***two*** "n module data lines" (452) in the preferred embodiment—one for each fork in the road—directly contrary to Netlist's contention that "the set of n module data lines" in Figure 4A would be limited to just ***one*** line 452 that connects the "first" (412A) and "second" (412**C**) memory devices in a "straight line.

(*Id.* at 68-69 (emphasis in original).)

Turning back to prosecution history, Respondents dispute the effect of the Applicant's examples of support it provided for amendments made after the first notice of allowance—*i.e.*, the excerpt promoted by Netlist. (*See id.* at 69-70.) Respondents first argue "an obscure statement like this during prosecution 'often lacks the clarity of the specification and thus is less useful for claim construction purposes.'" (*Id.* (citing *Phillips*, 415 F.3d at 1317).) Respondents then observe that the Examiner "never stated that he agreed with Netlist's interpretation of the claim," and argue he generally believed the claims to require a "fork in the road" consistent with the earlier prosecution disclaimer from the '185 patent. (*See id.* at 70-71.)

Finally, Respondents dispute the utility or clarity of Netlist's definition of "rank" in its proposed construction. (*Id.* at 71.) Respondents also disagree it follows from the claim language or patent specification, "which permits reading and writing from more than one rank of memory at the same time." (*Id.* at 71-72 (citing '907 patent at 15:3-6).)

In their reply brief, Respondents frame the issue for this limitation as:

> Netlist contends that the claim language of Term No. 1 ***negates*** the "fork in the road" configuration and ***requires*** the "straight line" configuration, *see* Netlist Br. at 15–23, while SK hynix and the Staff contend that Term No. 1, by itself, ***permits*** the "fork in the road" configuration (while other claim language, such as the "do not…receive" language of Term No. 2, ***requires*** the "fork in the road" configuration, consistent with the specification and prosecution history), *see* SK hynix Br. at 65–72; Staff Br. at 14–40.

(RRMB at 10.)

Regarding Netlist's "n set of module data lines" argument, Respondents respond that it "by itself, does not require either the 'fork in the road' construction or the 'straight line' construction; it is broad enough, by itself, to *permit* either construction." (*Id.* at 11 (emphasis in original).) Respondents continue, "[t]hus, to resolve whether the claim requires a 'fork in the road' or a 'straight line,' it is necessary to consider the rest of the claim language and the teachings of the specification . . . which Netlist never does." (*Id.* (citing CIMB at 16-23).)

Regarding that post-allowance prosecution history excerpt which Netlist's uses to show first and second memory devices are 412A and 412C, respectively, Respondents reproduce the excerpt and state:

Cl #	Amendment	Support
4 12	each respective buffer circuit being coupled to a respective set of the *M* sets of *n* data lines, to respective one or more of the first memory	As shown in FIGS. 4A and 4B, memory device 412A (or memory devices $412A_1$ and $412A_2$) (respective one or more of the first memory devices) and memory device
	devices via a set of *n* module data lines, and to respective one or more of the second memory devices via the set of *n* module data lines	412C (or memory devices $412C_1$ and $412C_2$) (respective one or more of the second memory devices) are coupled to the buffer circuit 416 via a same set of 8-bit data lines 452.

> *See* Ex. 11, '907 file history at 429–30 (red underlining added); Netlist Br. at 18–21. This statement during prosecution is at best ambiguous because "a same set of ***8-bit data lines 452***," by its plain terms, requires the "set" to have ***multiple*** "data line***s*** 452" (plural), with each data line 452 being "8-bit" wide, contrary to Netlist's position that the claimed "set" is limited to a ***single*** 8-bit data line 452. Indeed, Figure 4A (referenced in this statement) shows a "set" that includes ***two*** data lines 452, each of which is 8-bits wide ("0-7"). *See supra* p. 11 (drawing a red circle around the two 8-bit data lines 452); Ex. 9, '907 patent at at 13:35–:36. Thus, the "***set*** of 8-bit data line***s*** 452" — plural — referenced in this statement could encompass ***both*** lines 452 in Figure 4A (circled in red above on page 11) meaning this claim language, by itself, is broad enough to encompass 412**B** as the "second" memory device (consistent with the "fork in the road" interpretation proposed by SK hynix and the Staff).

(*Id.* at 12-13.) Respondents then argue this "obscure" excerpt does not overcome the general "fork in the road" requirement required by the claims as a whole. (*See id.* at 13.) Respondents add, considering the exact words of Netlist's proposed construction, that "rank" is not recited in the claims at all and should be rejected. (*Id.* at 14.)

3. Staff's Position

In its opening brief, the Staff generally does not believe the intrinsic evidence allows for the breadth of Netlist's proposed construction, on this term and those disputed claim terms related to it. (SIMB at 9-11.) The Staff states, "the claims of the '907 patent should be construed to require a memory buffer that selectively allows and inhibits communication between the memory

controller and selected and unselected memory devices, as opposed to encompassing configurations where the memory controller concurrently connects and communicates with all memory devices." (*Id.* at 12.)

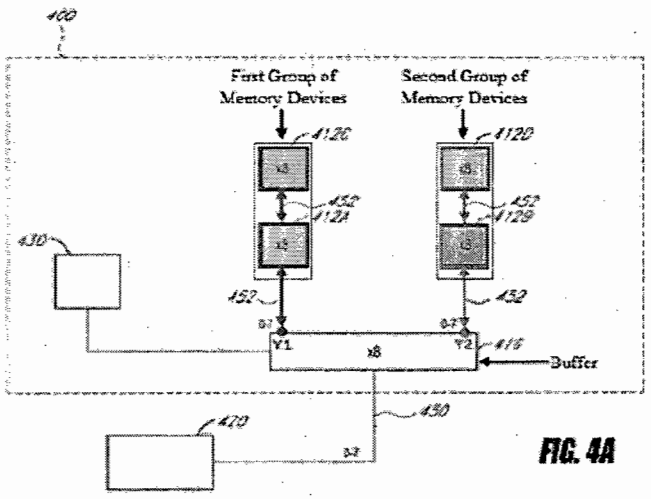
The Staff's brief discusses a range of other terms under the heading of this term at issue here. (*See, e.g.*, *id.* at 15 (discussing memory devices "selected" or "unselected," and "output or receive" or "do not output or receive").) In relevant part, the Staff argues the term should be construed "such that the first memory devices and second memory devices are on separate data lines from the memory controller." (*Id.* at 16.) The Staff continues:

> The alternative structure proposed by Complainant, where the first and second memory devices are on a shared data line to the memory controller, encompasses data from the memory controller's read/write command being communicated to both the first and second memory devices. Thus, the claims themselves support requiring separate data lines to the first and second memory devices, such that the second memory devices do not receive the communication from the memory controller.

(*Id.*) Staff also argues that Netlist's shared data lines interpretation is, contrary to Netlist's assertion, not disclosed in the '907 patent specification (*id.* at 17 (citing summary determination briefing)) and a POSITA would consider separate data paths to be a distinguishing feature of the invention (*id.* at 18 (citing '907 patent at 10:35, 11:20-48, Fig. 3A)). The Staff also describes Netlist's approach , where the first and second memory devices are on shared lines, as resulting in "dummy" buffers which do not select between first and second memory devices to communicate with (in violation of other, yet-to-be-discussed, claim language). (*See id.* at 20-21.)

Regarding the prosecution history, and the Examiner's rejection over claim 36 which involved groups of memory devices and terminals, the Staff contends the Applicant (Netlist):

> [I]n explaining a rejection by the examiner during prosecution of the '907 patent, the Complainant itself described Figure 4A as follows:



'907 patent, Figure 4A (annotated)
Different "***Groups***" Couple to Different "***Terminals***"

(*Id.* at 23 (citing summary determination briefing); *see also id.* at 27-29.) The Staff argues that this disclosure would not lead a person of ordinary skill to review this record and conclude the now-claimed "first memory devices" and "second memory devices" were anything other than what is shown in the above figure, as connected with separate data lines to separate terminals on buffer circuit 416. (*See id.* at 23-24 (citing '907 patent at 16:1-16); *see also id.* at 29-31.)

In its reply brief, the Staff confirms its view that, for the '907 patent, "the disputed terms are not suitable for construction in isolation of the other terms." (SRMB at 10.) Nevertheless, the Staff urges that Netlist's "set of n module data lines" antecedent basis-argument should be rejected. (*Id.* at 11.) The Staff contends "general claim construction rules provide that in a comprising claim 'a' followed by 'the' is interpreted as 'one or more.'" (*Id.*) The Staff reasons, "[b]ecause the claims allow for more than 'n module data lines,' the Staff submits that the more logical interpretation is to align the claims with how the invention is disclosed in the intrinsic evidence (*i.e.* the entirety of the patent figures)." (*Id.*)

The Staff also warns that Netlist's construction would encompass the prior art distinguished in the '907 patent's specification and prosecution history. (*See generally id.* at 11-12, 15-21.) The Staff further contends that Netlist's caselaw support regarding antecedent basis is an unreported Federal Circuit opinion that was focused on a claim preamble, and thus, not helpful to the issue at hand. (*Id.* at 22.) Next, the Staff argues the more general plural rule should apply, where "'subsequent use of definite articles 'the' or 'said' in a claim to refer back to the same claim term does not change the general plural rule, but simply reinvokes that non-singular meaning.'" (*Id.* (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 723 F.3d 1351, 1356 (Fed. Cir. 2000); *Baldwin Graphics Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 3142-43 (Fed. Cir. 2008)).) Generally, "the Staff submits that the intrinsic evidence supports interpreting the claims as encompassing one or more 'n module data lines,' which encompasses the invention described in the specification of a selective memory buffer having separate data paths to the first and second memory devices, such that unselected memory devices can be excluded from data transmissions from the memory controller." (*Id.* at 25.)

4. Analysis

For this limitation, I find there to be no substantive dispute as to what these claim terms mean. Netlist effectively argues this limitation means "both the claimed first and second memory devices are connected to a buffer circuit via the same set of the claimed module data lines." (CIMB at 16.) Respondents dispute this relationship between first and second memory devices—*but not because of this particular claim language*:

> In short, the claim language "set of n module data lines," by itself, does not require either the "fork in the road" construction or the "straight line" construction; it is broad enough, by itself, to permit either construction. Thus, to resolve whether the claim requires a "fork in the road" or a "straight line," it is necessary to consider the rest of the claim language and the teachings of the specification . . . which Netlist never does. . . .

(RRMB at 11.) The Staff similarly argues that it is *other* claim language which demands the first and second memory devices not be on the same set of data lines. (*See* SIMB at 15-16 (discussing how Netlist's interpretation vitiates the "output or receive / do not output or receive" language); SRMB at 10 ("the disputed terms are not suitable for construction in isolation of the other disputed terms").)

It seems to me that Respondents' and the Staff's briefing thus strays from the task at hand—which is to construe the following limitations:

Claim 1	Claim 16
each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines	each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines

I find as a simple matter of logic and plain and ordinary meaning that these limitations mean the respective first and second memory devices are coupled to each respective buffer circuit by the same set of *n* module data lines—exactly as written.

As explained above with respect to "output or receive / do not output or receive," claims 1 and 16 are unique through their recitation of the formula "[a] memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n" in their preambles. ('907 patent at cls. 1, 16.) This "N=M×n" formula for overall data bandwidth results in *n* representing an integer value of data lines—and not how many bits a single data line carries.

Thus, when it comes to a buffer circuit coupled "to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via *the set* of n module data lines" (emphasis added), I find antecedent basis principles dictate the first and second memory devices are both connected to the buffer circuit through the same set of *n* module data lines (where *n* is a number of data lines in the set) —exactly as Netlist contends. (CRMB at 13-14 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008)).) I also agree with Netlist that when *n* is a number of data lines, Respondents' "fork in the road" results in reading the limitation as "set of *2n* module data lines." (*See* CRMB at 10-14.) This contradicts the plain meaning of the claim.

Therefore, I construe "each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines" to mean exactly what it says—the respective first and second memory devices are both connected to their respective buffer circuit through the same set of *n* (as a number of) module data lines.

C. "the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines"

The term "the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines" appears in asserted claim 1 of the '907 patent. This claim reads:

1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, **the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines**, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the

each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

(emphasis added).

The constructions proposed by the parties for the term are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
"based on control signals (*e.g.*, direction of data, timing) from the module control circuit, each of the M buffer circuits permits the transmission of (N/M)-bits of data by driving data to/from the one or more DRAM devices in the N-bit wide active rank via the set of (N/M) module data lines (data lines on the memory device side of each buffer circuit) from/to the memory controller via a respective set of (N/M) data lines on the N-bit wide memory controller data bus"	Plain and ordinary meaning, with the same understanding as stated for term 1 above [*i.e.* "when considered with the surrounding language of the respective claim, the resulting physical arrangement of the elements of the claim (when given their plain and ordinary meaning) is a 'fork in the road' layout"].	"buffer circuit including logic …allowing communication" should be given the same construction as the 1023 investigation because the same disclaimer applies to the '907 patent, otherwise the claim lacks written description support the remainder of the term should be construed according to the plain and ordinary meaning, which is the buffer circuit initiates the action of data to be communicated from the memory controller through the M sets of n data lines (*i.e.* lines from memory controller to buffer), through the buffer, and through the set of n module data lines (*i.e.* lines from buffer circuit to memory devices) to first memory device (*i.e.* the first and second control signals are derived from a single the read/write command – so both should direct data to the same memory device, which is the first memory device in the context of the claim)

1. Netlist's Position

In its opening brief, Netlist claims its construction is supported by the intrinsic evidence "which expressly contemplates controlling data flow according to timing and direction-determinant control signals." (CIMB at 29-30 (citing '907 patent at Figs. 5, 6, 10:34-41, 15:52-64).) Netlist also claims the specification's description of a Column Address Strobe (CAS) latency value supports its construction. (*Id.* at 30 (citing '907 patent at 15:52-64).)

Netlist moves on to Respondents' and Staff's interpretation, where "the buffer circuit 'selectively' transmits data to only the first memory devices and not the second memory devices, where the word 'selectively' does not appear in the claims, expressly or by implication." (*Id.* at 31.) Netlist claims this interpretation imports limitations "neither present nor required by the '907 patent claims." (*Id.*) More specifically, Netlist contends "[t]he buffer circuit of the '907 patent claims is not required to implement the "selective allowance" and "selective isolation" functionality of the '185 patent." (*Id.*)

In its reply brief, Netlist argues Respondents' interpretation is, by Respondents' own admission, based on other claim language taken as a whole, and not the actual language at issue for this limitation. (CRMB at 29 (citing RIMB at 73).) Netlist views Respondents' discussion of dependent claim 2 as evidence of the weakness of their argument, and, ultimately, not persuasive because claim 2 is directed to the memory devices and not the buffer circuits. (*Id.*) Netlist repeats its overall position that:

> Failing to identify anything in actual claim language that requires any sort of "selective" discrimination, Respondents and Staff also attempt to argue that Netlist's "invention" as a whole is limited to "selective buffer circuits." This position is also unsupported by the specification or prosecution history of the '907 patent.

(*Id.*) Netlist claims it was the '185 patent's recitation of "*selectively* isolate" and "*selectively* allow" in its claims that resulted in the non-infringement determination in the 1023

Investigation—a term noticeably absent from the claims of the '907 patent. (*See id.* at 29-30; *see also id.* at 30-31.)

Netlist also contends that Respondents are judicially estopped from "equat[ing] buffer circuits that merely 'allow' communication with buffer circuits that 'selectively allow' communication." (*Id.* at 30 (citing *Sandisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1290 (Fed. Cir. 2005); *New Hampshire v. Maine*, 532 U.S. 742, 750-51 (2001)).) Netlist adds, even if not estopped, "their position is wrong because the specification of the '907 patent discloses multiple embodiments. These embodiments include those that do not require a "fork in the road," but instead implement the 'straight line' embodiment as discussed [] above." (*Id.*)

Netlist then discusses the supposed disclaimer from the '907 patent's parent, the '185 patent, prosecution history. (*See id.* at 31-34.) In short, Netlist argues that the '185 patent was allowed over prior art Rajan because of its buffer circuits which both receive control signals and selectively allow or isolate in response to those control signals—not just the "selective" language. (*See id.*) Netlist repeats its overall position that "nothing in the plain language of the claims, the prosecution history, or the 1023 ID could justify importing the word 'selective" into the claims of the '907 patent." (*Id.* at 34.)

2. Respondents' Position

In their opening brief, Respondents immediately point out "[t]he Staff agrees with SK hynix that this claim language is consistent with the 'fork in the road' layout shown above. . . ." (RIMB at 73.) Respondents argue that Netlist's interpretation, delineating between "selectively allowing" and merely "allowing," "ignore the other 400+ words of the claim, which create the 'fork in the road.'" (*Id.*)

Respondents continue to argue "Netlist's 'straight line' interpretation would render parts of this claim language superfluous" which is improper. (*Id.* (citing *Akzo Nobel Coatings, Inc. v. Dow*

Chem. Co., 811 F.3d 1334, 1340 (Fed. Cir. 2016)).) Respondents reason this is so because when the first and second memory devices are on a shared data line, data is communicated to both devices at the same time—hence, no need for the claim to recite, as it does, the "*one or more of the first* memory devices" language. (*Id.* at 73-74.) Respondents also view Netlist's construction as improperly allowing mere direction and timing control to satisfy the limitation. (*Id.* at 74.) Respondents observe that during prosecution of the '907 patent, Netlist depended on the following specification excerpt to support the "allowing" claim language:

> During the second time period 602, the control circuit 430 supplies control signals to the control logic circuitry 502 to enable the first tristate buffer 504 and to disable the second tristate buffer 506 and the read buffer 509. Thus, during the second time period 602, data bits pass from the data lines 518 to the first terminal Y1 and on to the memory devices 412A, 412C. . . .
>
> During the third time period 603, the control circuit 430 supplies control signals to the control logic circuitry 502 to enable the second tristate buffer 506 and to disable the first tristate buffer 504 and the read buffer 509. Thus, during the third time period 603, data bits pass from the data lines 518 to the second terminal Y2 and on to the memory devices 412B, 412D.

(*Id.* at 74 (citing '907 patent at 17:63-18:2, 18:10-16).) Respondents conclude to criticize Netlist's construction for "literally just rewrite[ing] all of the language, with neither justification for the wholesale rewrite of the claim language nor explanation for what is intended by all of the different words." (*Id.* at 75.)

In their reply brief, Respondents explain:

> Netlist asserts that Term No. 3 negates the "fork in the road" configuration, *see* Netlist Br. at 28–32, while SK hynix and the Staff agree that Term No. 3 — when read in the context of the surrounding claim language, as well as the specification and prosecution histories — requires the "fork in the road" configuration where 412**B** is the "second" memory device (and precludes the "straight line" configuration where 412**C** is the "second" memory device), see SK hynix Br. at 72–75; Staff Br. at 44–48.

(RRMB at 27-28.) Respondents dispute Netlist's assertion that certain passages of the '907 patent show that memory devices 412C are the "second memory devices." (*Id.* (referring to '907 patent at 10:34-41, 14:38-43, 15:19024, 15:52-64, 17:5-12, Fig. 5).) Rather, according to Respondents, these passages and figure "say[] the opposite, namely that 412C is one of the 'first' memory devices:"

> The ranks of memory devices 412 are likewise divided into two groups with one group associated with path A and one group associated with path B. As shown in FIG. 3A,[8] ***rank A and rank C are in the first group***, and ***rank B and rank D are in the second group***. Accordingly, the memory devices 412A, 412C of rank A and rank C are connected to the data transmission circuits 416 by a first one of the two data paths, and the memory devices 412B, 412D of rank B and rank D are connected to the data transmission circuits 416 by a second one of the two data paths.

(*Id.* at 28 (citing '907 patent at 15:39-51 (emphasis added by Respondents), 15:65-16:16).) Respondents add that "the specification uses the word 'allowing' (not just 'selectively allowing') to describe the 'fork in the road' configuration." (*Id.* at 29 (citing '907 patent at 15:65-16:11).)

3. Staff's Position

In its opening brief, the Staff explains:

> As discussed in detail in the Staff's Response to Respondents' MSD, the claims of the parent patent adjudicated in the 1023 investigation, and also in the '907 patent all require a memory buffer. Staff's Response to Respondents' MSD at 28-35. Thus, in line with the invention's memory buffer as disclosed in the specification (*i.e.* divorces communication between selected and unselected devices), which coincides with the prosecution history disclaimer found in the 1023 investigation, the "buffer circuit having logic" in the claims of the '907 patent should have the same limited scope.

(SIMB at 45.)

With respect to Netlist's construction, the Staff argues "[t]he evidence does not support Complainant's position that a person of ordinary skill in the art would understand that a broader 'dummy' buffer is claimed," where "dummy" refers to a buffer which is non-selective of the

memory devices coupled to it. (*Id.*) To the contrary, according to the Staff, the specification "expressly describes a 'smart' buffer circuit having logic that selects between two data paths, *i.e.*, enable Y1, enable Y2, Select Y1/Y2." (*Id.* at 46 (citing '907 patent at Fig. 5).) The Staff adds "[t]hese disclosures in the specification should be given additional weight because during prosecution the patentee expressly pointed to these disclosures (*i.e.* enable Y1, enable Y2, Select Y1/Y2) as support for the ['allowing'] claim limitation." (*Id.* (citing "FH at 430").)

The Staff contends "a person of ordinary skill in the art is entitled to rely on such representations" (*id.*) and Netlist's construction actually reads out the "logic" portion of the limitation (*id.* at 47). Put another way, the Staff reasons "a person of ordinary skill in the art would not think that any generic combination of memory buffers and module control signals fall within the scope of the claims." (*Id.*)

In its reply brief, the Staff argues "[e]ven where the specification broadly discloses a device, the Federal Circuit has construed the claim's [sic] to exclude features that the patentee used to distinguish prior art." (SRMB at 16-17 (citing *O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1581 (Fed. Cir. 1997)).) The Staff contends this is a problem because "Complainant's claim interpretation combines a prior art memory module that has two memory devices on shared data lines, and a prior art module control circuit that sends chip-select signals to targeted memory devices to perform the read or write operation." (*Id.* at 17.) The Staff continues, "under Complainant's proposed constructions, the claimed memory device configuration, module control circuit sending chip-select signals, and non-selective memory buffer are all described as known art in the specification." (*Id.* at 18.)

4. Analysis

Here, I find a similar situation to the "set of *n* module data lines" discussion where Respondents avoid offering a construction for this actual limitation as opposed to showing why

this limitation is merely compatible or "consistent" with a "fork in the road" understanding of the claims. (*See* CRMB at 29; RIMB at 73 ("[t]he Staff agrees with SK hynix that this claim language is consistent with the 'fork in the road' layout . . .").)

To the extent Respondents and Staff argue this particular claim limitation requires "selectively" "allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller" (*i.e.*, a "fork in the road"), I disagree. There are no words in this limitation, in a plain and ordinary sense, to require this. I also disagree that a failure to read in "selectively" somehow renders "one or more of the first" language superfluous, as Respondents contend:

> Thus, under Netlist's interpretation, the reference to the "first" memory device in the claim language would be superfluous, because the data would be communicated to ***all*** of the memory devices. Netlist's interpretation would rewrite the claim language to be: "the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective ~~one or more of the first~~ memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines."

(RIMB at 73-74 (strike out and emphasis in original).) The present circumstances are not the same as in *Akzo*, cited by Respondents for this point, where the claim term "collection" in "pressurized collection vessel" was imparted meaning so as to avoid the result of any "pressurized vessel" constituting a "pressurized collection vessel." *Akzo*, 811 F.3d at 1340 ("The district court's construction of 'accumulation,' on the other hand, gives the term 'collection' proper meaning in context).) Here, there is meaning to explicitly reciting that it is the first memory devices which are allowed communication—other memory devices that may exist may not be allowed that communication *or* may not be tied to logic at all. Even then, the principle applied in *Akzo* is that

constructions which render other claim language superfluous "are disfavored;" not prohibited. *Id.* (citing *Merck & Co. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005); *Power Mosfet Techs., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1410 (Fed. Cir. 2004)).

I do acknowledge, however, that this limitation *as it appears in claim 1* would not seem to add much to the apparatus as it would be assumed that, when working with a device having first memory devices, that some manner of logic or circumstance would allow the first memory devices to communicate with the system memory controller; *i.e.*, to perform their known role. I also acknowledge that an apparatus which responds to a signal with logic to "allow" a circumstance *suggests* that the logic might respond to a different signal differently and perhaps not "allow" that circumstance. Neither of these possibilities, however, are a reason to read in "selectively" into the simply written language of "allowing communication."[1] With respect to the Staff's concern that a failure to read in "selectively" treads upon the prior art (*see* SRMB at 18, 45 (discussing "dummy" buffer)), I expect that to be explored fully in the invalidity context and will not inoculate the claim against it now, again, because the limitation expressly does not include "selectively" as was included in the '185 patent (*see id.* at 45 ("as explained in the 1023 investigation, a prior art reference claimed exactly this type of 'dummy' buffer chip, and the patentee distinguished the invention's memory buffer on the basis that it is selective.'")).

With that said, I do not find it is appropriate to construe the limitation exactly as Netlist has proposed either, in lieu of how it is written. Netlist has, as Respondents argue, "rewrit[ten] all of the language, with neither justification for the wholesale rewrite of the claim language nor explanation for what is intended by all the different words." (RIMB at 75.) Thus, I only find that

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[1] I note also that other claims, such as claim 30 and 58 are not as simple and perhaps come closer to reflecting Respondents' "fork in the road" within the buffer circuit (*See, e.g.*, '907 patent at cls. 30 (reciting data paths being configured differently), 58 (reciting data paths configured differently).)

this limitation as found in claim 1 does not require "selectively allowing communication" or a "fork in the road" as Respondents and Staff propose. In light of the parties' briefing, there is no need to construe it further.

D. "produc[e/ing]"

The term "produc[e/ing]" appears in asserted claims 1, 16, 43, 58 of the '907 patent.[2] These claims read:

> 1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
>
> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to **produce** first module control signals and second module control signals in response to the set of input address and control signals;
>
> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
>
> M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further

[2] "Producing" actually only appears in claim 30 of the '907 patent, which is no longer asserted by Netlist.

configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

....

16. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to **produce** first module control signals and second module control signals in response to the set of input address and control signals;

a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices

via the set of n module data lines, the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines, wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

43. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices;

a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to **produce** output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to **produce** a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or

receive any data associated with the memory read or write command;

a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.

....

58. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices including first memory devices and second memory devices;

a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller

via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to **produce** first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to **produce** a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;

a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein the each respective buffer circuit is further

> configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and
>
> a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

(emphasis added).

The constructions proposed by the parties for the term are as follows:

Netlist's Construction	**Respondents' Construction**	**Staff's Construction**
Plain and ordinary meaning (*e.g.*, processing and outputting one set of control signals for the memory devices and one set of control signals for the buffer circuits based on a received set of address and control signals).	Create, *i.e.*, bring into existence	Create new signal (*i.e.* more than pass through)

1. Netlist's Position

In its opening brief, Netlist states its position clearly as "the term 'produc[e/ing]' should be afforded its plain and ordinary meaning as 'processing and outputting one set of control signals for the memory devices and one set of control signals for the buffer circuits based on a received set of address and control signals.'" (CIMB at 32.) Netlist characterizes Respondents' and the Staff's

constructions as "illogical" and contends "this claim term requires no particularized construction." (*Id.* at 33.) Netlist adds, "Respondents' proposed construction adds nothing of value in understanding the claim term" because this "means that the module control circuit creates control signals from nothing [which] is contrary to the claim language and specification." (*Id.* at 33-34.)

More specifically, in Netlist's view, the "in response to" claim language means "[t]he produced control signals are thus necessarily based on the received address and control signals. Consequently, they are not created from nothing." (*Id.* at 34.) Netlist then cites specification examples that supposedly "disclose the concept of the control circuit producing, *i.e.*, processing and outputting, one set of control signals for the memory devices based on a received set of address and control signals." (*See id.* at 34-35 (citing '907 patent at 8:14-17, 10:24-34, 15:52-64).)

In its reply brief, Netlist states "[t]his word 'produce' requires no construction" and should be given its plain and ordinary meaning. (CRMB at 34.) Netlist argues Respondents' and the Staff's constructions read out the "in response to" language from elsewhere in the claim. (*Id.* (citing *Thorner*, 669 F.3d at 1366).) Netlist perceives the "in response to" language as meaning the module control signals "produced" are "necessarily based on the received address and control signals; they are not all required to be 'new signals' created from nothing as Respondents argue." (*Id.* at 35.)

Netlist then criticizes Respondents for incorporating "cherry-picked limitations" taken from the '386 patent specification, which is incorporated by reference into the '907 patent, as opposed to starting with the '907 patent's actual claim language. (*See id.*) Netlist repeats its view that under that language:

> The claim recites that the module control circuit receives an input: a set of [X] (*i.e.*, [address and control signals]). In response to this input, it produces an output: a set of ([1st] and [2nd]) (*i.e.*, [first

> module control signals] and [second module control signals]). In other words, [X]→([1st]+[2nd]). The [1st] portion of this output (the first module control signals) is sent to the memory devices and the other portion of this output, [2nd] (the second module control signals), is sent to the buffer circuits.

(*Id.* at 35-36.) According to Netlist, "[t]he construction urged by Respondents would require that every constituent signal in the output signal set be a brand-new signal," or, put another way, "if any portion of [X] is in either [1st] or [2nd], the limitation could not be satisfied." (*Id.* at 36.) Netlist argues this is not correct for several reasons. (*Id.*)

First, Netlist contends "the specification teaches use cases where at least one of the input signals of [X] is 'registered' by the module control circuit and then output to the memory devices." (*Id.* (citing '907 patent at 10:29-32).) Second, Netlist contends dependent claim 2, which recites "module control circuit is configured to *generate* the second chip-select signals based on the set of input address and control signals," demonstrates "produce" means something different from "generate." (*Id.* at 36-37 (citing *Cave Consulting Grp., LLC v. OptumInsight, Inc.*, No. 2017-1060, 2018 U.S. App. LEXIS 7432, at *16 (Fed. Cir. Mar. 21, 2018) (slip op.)).) Third, Netlist argues dependent claims 41, 46, and 49 (promoted by Respondents) do not overcome the above evidence in that they discuss "data signals" and not "module control signals." (*See id.* at37-38.) On this point, Netlist reasons:

> The claimed "data signals" in the context of a different component of the claimed device (the buffer circuit) are treated differently by the patent than the "control signals" in the context of the relevant component (the module control circuit). As such, limitations directed to the data signals of claims 41, 46 and 49 cannot restrict the interpretation of claim 1[a]'s use of the term "produce."

(*Id.* at 38.)

Netlist then turns to the '386 patent and understands Respondents to argue "that one or more of the characteristics of the examples of control circuits from the '386 patent limit the

meaning of 'produce.'" (*Id.* at 39.) Netlist counters, "[w]hile the specification of the '907 patent incorporates by reference the disclosures of other patents, including the '386 patent, this bedrock principle that limitations from the specification must not be read into the claims holds true." (*Id.*) To wit, Netlist points out that disclosure in the '907 patent specification which states the control circuits disclosed in the '386 patent are mere examples which may serve for certain embodiments of memory modules disclosed in the '907 patent. (*Id.* (citing '907 patent at 10:24-44); *see also id.* at 42-43.) To Netlist, this falls short of the clear and unmistakable disclaimer needed to limit claims based on the specification. (*Id.* at 39-40 (citing *X2Y Attenuators, LLC v. International Trade Comm'n*, 757 F.3d 1358, 1362-63 (Fed. Cir. 2014).) Netlist adds later, "the '386 patent does not 'provide an example of the details of the functionality of the disclosed control circuit' of the '907 patent." (*Id.* at 42 (citing RIMB at 29).)

Netlist also dismisses the importance of a declaration from one of the '907 patent's inventors referenced by Respondents because of: his status as inventor, the differing claims-at-issue in the declaration, and the use of "produce" as with respect to a commercial product. (*See id.* at 40-41 (citing *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1380 (Fed. Cir. 2000); *Unwired Planet L.L.C. v. Google, Inc.*, 660 F. App'x 974, 984 (Fed. Cir. 2016)); *OSRAM GmbH v. ITC*, 505 F.3d 1351, 1361 n.2 (Fed. Cir. 2007); *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1381 (Fed. Cir. 1998); *NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002)).) Netlist concludes with a discussion of that expert testimony cited by Respondents, and argues it is inapplicable as it was related to a different claim term. (*Id.* at 42.) Similarly, Netlist argues Respondents' use of a dictionary for "produce" should be ignored as "counter to the meaning made clear in the intrinsic record that was more fully addressed both above and in Complainant's Opening Brief." (*Id.* at 43 (citing *Belden Inc. v. Berk-Tek LLC*, 610 F. App'x 997, 1002 (Fed. Cir. 2015) (quoting *Phillips*, 415 F.3d at 1322-23)).)

2. Respondents' Position

In their opening brief, Respondents argue their construction is "[c]onsistent with the express language of the claims and the description of this term in both the specification and prosecution history of the '907 patent." (RIMB at 20.) Respondents continue "[a]n example would be producing additional chip-select signals for the purpose of 'rank multiplication,' as discussed below." (*Id.*) Respondents only mildly object to the Staff's construction as possibly allowing for any act on a signal which is "more than pass through." (*Id.*) Respondents criticize Netlist's construction as simply failing to address the dispute between the parties and improperly replacing "producing" with "processing and outputting." (*Id.*) Respondents make clear that "producing" "should not include within its scope the mere act of processing or passing along existing signals." (*Id.*)

Respondents then discuss a prior Netlist patent, the '386 patent, which is incorporated by reference into the '907 patent specification. (*See id.* at 21-23.) Respondents explain the '386 patent is directed to a feature called "rank multiplication" which "intercept[s] communications between the host computer and the memory devices and 'trick' the host computer into believing there was a single rank of 1Gb of memory, when in reality there were two ranks of (cheaper) 512Mb memory (unbeknownst to the host computer)." (*Id.* (citing '386 patent at 7:24-29, 10:56-11:15).) According to Respondents, one aspect of this feature is the creation of two chip-select signals from one chip-select signal received from the host computer's memory controller. (*See id.* at 22 (citing '386 patent at 12:14-26, 7:64-8:45, 22:21-29).)

Respondents argue the content of the '386 patent shows "produce," as used in the '907 patent claims, refers to "new signals that did not previously exist as an output." (*Id.* at 23.) In particular, Respondents look to dependent claim 2, which reads:

> The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.

(*Id.* at 24 (citing '907 patent at cl. 2).) Respondents argue that the recited "second chip-select signals," as included within the "first module control signals" and "generate[d]" by the module control circuit, indicate "produced" must mean more than "altering or transferring." (*Id.*) Respondents make a similar argument based on the language of dependent claims 41, 46, and 49 (*see id.* at 24-25) and uses of the word "produce" in the '907 patent specification (*id.* at 25 (citing '907 patent at 10:39-41, 15:59-64)). Respondents contrast this with '907 patent excerpts describing acts done on existing signals—*e.g.*, "regenerate," "restore," and "register." (*Id.* at 26-27 (citing '907 patent at 16:56-17:4, 10:29-32).) Respondents claim the '386 patent makes a similar distinction. (*See id.* at 27-28 (citing '386 patent at 5:27-41, 7:52-56, 6:63-7:5, Fig. 1A).)

Respondents conclude by pointing to a declaration of one of the '907 patent inventors, Mr. Lee, for support, wherein the declaration referred to a Netlist ASIC specification sheet to show conception of the "producing" limitation. (*See id.* at 28-29 (citing RIMB, Ex. 11 at 175-222).) Respondents also refer to a Netlist expert declaration from an *inter partes* review proceeding which interpreted "generating a set of output control signals," as in the '386 patent claims, as creating a signal that did not exist. (*Id.* at 29-30 (citing RIMB, Ex. 15 at ¶¶ 22, 34, 37-38).) Respondents claim this is relevant to the "producing" in the '907 patent because the '907 patent "incorporates by reference the '386 patent as the primary example of '*produc[ing]* additional chip-select signals.'" (*Id.* at 30 (citing '907 patent at 10:39-44).)

In their reply brief, Respondents state "even Netlist's own expert admits that remapping, duplicating, regenerating, and other actions—all of which are arguably 'more than pass through'—do not create new signals and thus would not satisfy the proper understanding of 'producing.'" (RRMB at 32 (citing RIMB at 29-30).) Respondents argue Netlist's construction of "processing and outputting" would, on the other hand, be satisfied by remapping, duplicating, regenerating, and similar actions. (*Id.* at 33.) Respondents also view Netlist as ignoring those portions of the '907 patent that use the term "produce" in favor of other portions that use other terms like "transmit" and "register." (*Id.* at 34-35.) Respondents add:

> The only relevant portion of the specification Netlist cites to, *see* Ex. 9. at 15:52–:64, is consistent with SK hynix's proposed construction that "producing" refers to creating new control signals (*e.g.*, for the logic 502 to control the buffer circuit 416, which the system memory controller 420 does not know about). *See* Netlist Br. at 34–35.

(*Id.* at 35.)

Respondents then dispute the idea that their construction requires new signals be created "from nothing." (*Id.*) Respondents acknowledge that the signals "produced" as an output based on "address and control signals" as the input. (*Id.* (citing '907 patent at cl. 1).) Respondents reason "[b]ecause this requirement is already incorporated in the express claim language, it is not necessary for SK hynix's proposed construction to specify these inputs." (*Id.* at 35-36.)

3. Staff's Position

In its opening brief, the Staff cites the '907 patent specification and argues "the term would be understood to mean more than passing through the memory controller signals." (SIMB at 49 (citing '907 patent at 10:24-45).) The Staff adds that it "does not dispute Complainant's proposal that the claimed "first module control signal" and "second module control signal" should both correlate to the same memory controller read/write command referenced in the claim." (*Id.*) In its

reply brief, "[t]he Staff notes that Respondents' only proposed construction for the '907 patent is with respect to the word 'produce,' for which there does not appear to be a substantial dispute between the parties." (SRMB at 10, n.5 (citing CIMB at 14).)

4. Analysis

For this limitation, I agree with the Staff that the parties' dispute is not substantial. Indeed, I find it is largely resolved through the assertion in Respondents' reply brief that their construction does not require the "produced" signal to be created "from nothing," as Netlist understands "from nothing." (*See* RRMB at 35; CIMB at 35.) For example, I do not view Respondents' proposed construction as excluding signals constructed in response to the nature of a previously received signal or signals that incorporate portion(s) of that previously received signal. (*See* CRMB at 35-36.) Rather, I agree with Respondents' explanation that "produced" signals are simply "new signals that did not previously exist as an output." (RIMB at 23.)

This is consistent with the specifications of the '907 patent and U.S. Patent No. 7,289,386 (incorporated by reference for this feature ('907 patent at 10:39-44)) which describe a memory module controller producing control signals which are tailored to the actual number of memory devices on the memory module, as compared to the number of memory devices the external system memory controller believes are present on the memory module. This concept appears in the '386 patent, for example, in the Summary of the Invention, where first and second numbers of memory devices are discussed:

> In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board. The plurality of memory devices has a first number of memory devices. The logic element receives a set of input control signals from the computer system. The set of input control signals corresponds to a second number of memory devices smaller than the first number of memory devices. The logic element generates a set of output control

> signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices.

('907 patent at 2:46-58.) The concept also appears in the table and figures of the '386 patent which explain the creation of signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} in response to previously received signals CS_0 and CS_1:

FIG. 1A

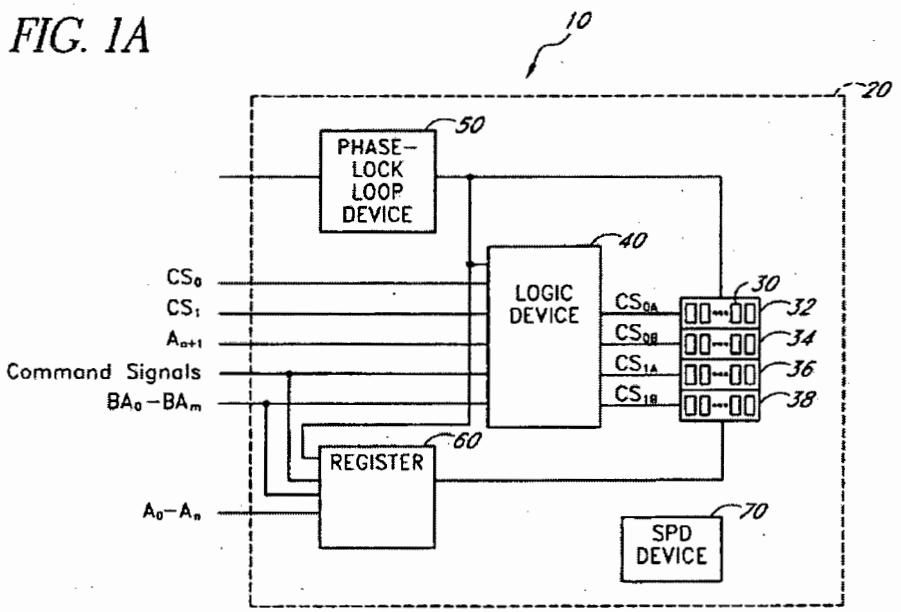

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

('386 patent at Fig. 1A, 8:1-14; *see also* '386 patent at 8:15-9:21.) Each of the above excerpts of intrinsic evidence reflect control signals "produced" in response to other control signals.

To the extent Respondents contend their proposed construction of "create, *i.e.* bring into existence," excludes "remapping, duplicating, regenerating, and other actions" (*see* RRMB at 32), I disagree it should be construed this way.[3] In a plain and ordinary sense, remapping, duplicating, and regenerating are all forms of creating. Indeed, in light of Respondents' argument that "producing" is effectively the same as "generating" (RIMB at 29-30) it is hard to understand how, in a plain and ordinary sense, "regenerating " is not a type of "generating" and therefore also a type of "producing." The same is true for duplicating which, in a plain and ordinary sense, means creating a copy of something—*i.e.*, producing a second identical to a first.

Respondents' evidence to the contrary is an expert declaration arising during an *inter partes* reexamination and opining on the meaning of "generating a set of output signals" as found in the claims of the '386 patent. (*See id.* (citing RIMB, Exs. 15-16).) According to Respondents, that expert declared that none of "remapping," "duplicating," "passing," or "regenerating" a previously existing signal constitutes "generating a set of output signals." (*Id.* at 30 (citing RIMB, Ex. 15 at ¶¶ 15, 22, 38; RIMB, Ex. 16 at ¶¶ 15, 16).)

I decline to give the expert declaration overriding weight for two reasons. First, the utility of the declaration depends on equivalency between "produce" as used in the '907 patent and "generate" in the '386 patent. I find that these terms may very well be equivalent but Respondents' argument to that effect is significantly undercut by their parallel argument that "produce" in the '907 patent (with respect to module control signals) and "produce" in the parent '185 patent (also with respect to module control signals) are somehow of different scope. (RRMB at 33, n. 9 ("Furthermore, the '907 patent uses the term 'produce' in a different, and narrower context than the '185 patent, which is another reason the ID in the 1023 Investigation is

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[3] Respondents reply brief does not mention this aspect of their proposed construction. (*See* RRMB at 32-36.)

not relevant to either claim construction or infringement with respect to the term 'produce' in this investigation.").) To the contrary, as explained by the parties, these patents share a specification, are linked by terminal disclaimer, and wherein the '185 patent claims a memory module controller which "produce[s] module control signals" ('185 patent at cl. 1) the '907 patent claims a memory module control circuit which "produce[s] first module control signals and second module control signals" ('907 patent at cl. 1). If find it hard to believe these two uses of "produce" have different scope while "produce" and "generate" are identical.

Second, I find the expert's opinion is conclusory and conflicts with the intrinsic evidence of the '386 patent. As shown in the '386 patent's TABLE 1, reproduced above, State No. 1 involves a received signal CS_0 in a low, logic 0 state. The "generated" (or "produced" according to Respondents) signal CS_{0A} is also in a low, logic 0 state. CS_{0A} is thus, arguably, a duplication or regeneration of CS_0. The expert declaration disputes this (*see* RIMB, Ex. 15 at ¶ 23) but does so in a completely conclusory manner. I therefore find a conflict between the content of the '386 patent and that expert's opinion. The Federal Circuit has instructed that in such cases of conflict, the extrinsic evidence should be disregarded. *SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1210 (Fed. Cir. 2013) ("In whole, Dr. Salomon's opinions are unhelpful to our analysis here. They are conclusory and incomplete; they lack any substantive explanation tied to the intrinsic record; and they appear to conflict with the plain language of the written description. Without a more detailed explanation of how Dr. Salomon formed his conclusions and why they conflict with the plain language of the specification, we must agree with the district court that Dr. Salomon's testimony deserves no weight.").

Thus, in light of the above, I adopt Respondents' construction as the plain and ordinary meaning where "produce" simply means "create, *i.e.*, bring into existence."

E. "wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more [of the first memory devices / memory devices in the subset of the memory devices] [as well as / and] memory device load associated with the [respective] one or more of the [second / other] memory devices from the memory controller"

The term "wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more [of the first memory devices / memory devices in the subset of the memory devices] [as well as / and] memory device load associated with the [respective] one or more of the [second / other] memory devices from the memory controller" appears in asserted claims 1, 16, 43, and 58 of the '907 patent. These claims read:

> 1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
>
> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
>
> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
>
> M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the

first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, **wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller**; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

....

16. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;

a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being operatively coupled to the memory controller

via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits, **wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller**; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines, wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

43. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices;

a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and

wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit, **wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller**; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.

....

58. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices including first memory devices and second memory devices;

a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;

a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective

one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, **wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller**; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

(emphasis added).

The constructions proposed by the parties for the term are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
"isolate memory devices load" should be given a construction in accordance with the 1023 investigation, which is "electrically separate memory device load" "as well as" / "and" should be construed as having its plain and ordinary meaning of "in addition to." In the context of the claim term, this means the data buffers isolate the load of all of the memory devices, without any selectivity.	"isolate" should be given the same construction as in the 1023 investigation, which is "electrically separate." "as well as" / "and" should be construed in the context of this phrase such that the full term means: "each buffer circuit is configured to isolate (*i.e.*, electrically separate) the [first memory devices / memory devices in the subset of the memory devices] from the memory controller during a read or write command to the [second / other] memory	"isolate" should be given same construction as the 1023 investigation, which is "electrically separate" "as well as" / "and" – capability of isolating first memory device and separately second memory device; construing "as well as" to isolate both lacks written description support, and/or the term

Plain and ordinary meaning as to the rest of the term.	devices, and separately isolate (*i.e.*, electrically separate) the [second / other] memory devices from the memory controller during a read or write command to the [first memory devices / memory devices in the subset of the memory devices]." Plain and ordinary meaning as to the rest of the term.	

1. Netlist's Position

In its opening brief, Netlist begins, "[t]he claim language is clear on its face and the intrinsic evidence supports Netlist's common sense interpretation." (CIMB at 36.) Netlist adds, "[t]he parties agree that the term 'isolate' should be given a construction consistent with the 1023 investigation, which is 'electrically separate;'" and the remainder of the term should be given tis plain and ordinary meaning. (*Id.* (citing CIMB, Ex. 3 at 121; CIMB, Ex. 5, App'x A at 6-7).) Rather, according to Netlist, the parties' dispute lies in: "(1) what is being isolated; and (2) how such isolation must be performed." (*Id.*)

To begin, Netlist argues that the term means what it says—that a memory device load is isolated—as opposed to the memory devices themselves being isolated, which is what Netlist understands Respondents and the Staff to argue. (*See id.* at 37.) Netlist claims the latter approach is contrary to the plain language of the claim term. (*Id.* (citing '907 patent at 19:36-38; 21:36-38; 25:57-59; 27:46-47).) More specifically, Netlist explains "FIG. 5 depicts that the write buffer 503 and read buffer 509 isolate the load of the memory devices from the memory controller." (*id.* at 38 (citing '907 patent at 16:36-44).) Additionally, according to Netlist, these buffers "isolate the loads of all memory devices connected to the disclosed buffer circuit from a memory controller

420 regardless of their terminal connection (*e.g.*, Y1, Y2)." Netlist reasons, "[t]hus, these buffers do not separately (or selectively) isolate the load of different memory devices connected to the same terminal." (*Id.*) Netlist claims Respondents acknowledged this difference during the 1023 Investigation. (*Id.* at 39 (citing CIMB, Ex. 11 at 4-5).) Netlist highlights Respondents contention that different buffers, 504 and 506, also shown in Figure 5, are what achieve the "fork in the road." (*Id.* (citing CIMB, Ex. 11 at 10).)

Beyond this, Netlist contends Respondents are actually judicially estopped from arguing "that isolating memory device loads require selectivity" based on the developments in the 1023 Investigation. (*See id.* at 39-40 (citing *New Hampshire v. Maine*, 532 U.S. 742, 749 (2001)).) Netlist further contends "Respondents are estopped from advancing their argument that isolating memory device load means isolating or selecting memory devices." (*Id.*) Netlist observes that in the 1023 Investigation, Respondents argued:

> Netlist asserts an infringement theory which refers to the load of the memory devices, even though the claim language plainly requires isolating (*i.e.*, electrically separating) the memory devices, not just their load. Indeed, the preferred embodiment in FIG. 5 shows that buffers 503 and 509, which isolate the load of all the memory devices all of the time, without any selectivity. *See* JX-002 at 16:12-20.

(*Id.* at 40-41 (citing CIMB, Ex. 11 at 4-5).) Netlist argues this prior argument prohibits Respondents' current argument—that "the surrounding claim language, the specification, and the prosecution history limit this term to isolating only one of the first and second memory devices at a time." (*Id.* at 41 (citing CIMB, Ex. 5, App'x A at 4).)

Moving on, Netlist considers Respondents to "argue that this term is limited to isolating, or electrically separating, 'only one of the first and second memory devices at the [same] time.'" (*Id.* at 43 (citing CIMB, Ex. 5, App'x A at 4).) Netlist counters that this is factually incorrect and against claim construction principles that give the more weight to the language of the claims, even

over other intrinsic evidence. (*Id.* (citing, *inter alia*, *Interactive Gift Express, Inc. v. Compuserv Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001)).) Netlist also views Respondents, and the Staff, as reading out the "as well as / and" language to introduce a selectivity requirement, when these terms plainly mean "in addition to." (*Id.* at 43-44.)

In its reply brief, Netlist remarks that it intentionally omitted the term "selectively" when it drafted these claims, and yet this is exactly what Respondents and the Staff try to read back in. (CRMB at 44.) Netlist claims, contrary to Respondents' position, that its construction "is the only proposal supported by the intrinsic record, including the language of the claims. . . . The '907 specification makes clear that the data buffers isolate the load of all the memory devices, without any selectivity." (*Id.* at 47 (citing '907 patent at 14:63-15:3, 19:36-38; 21:36-38; 25:58-59; 27:46-47).)

2. Respondents' Position

In their opening brief, Respondents acknowledge, as Netlist did, that "the parties all agree that 'isolate' means 'electrically separate,' as found in the 1023 Investigation." (RIMB at 80 (citing RIMB, Ex. 7 at 121).) In Respondents' view:

> The dispute is whether the remainder of the claim language in Term No. 5 requires the "fork in the road" layout (as SK hynix and the Staff contend), or whether the claim language covers a "straight line" interpretation where the "buffer circuit" merely isolates the ***electrical load*** of all the memory devices but still permits data to be sent concurrently to all of the memory devices (as Netlist contends).

(*Id.* at 80-81 (emphasis in original).) Respondents continue:

> If the claim language, in its entirety, merely stated a "buffer circuit that isolates memory device load," then such language, by itself, would not require the "fork in the road" layout. But that is not the claim language in its entirety. As discussed above with respect to Term Nos. 1–3 and 7, the claims all require the "buffer circuit" to have a "fork in the road" layout, and the language in Term No. 5 is consistent with that requirement. *See supra* pp. 31–79.

(*Id.* at 81.) Respondents further contend that Netlist's "straight line" approach would mean "isolating the electrical load on the data bus would always isolate the electrical load of both the 'first' and 'second' memory devices at the same time." (*Id.*) This, according to Respondents, conflicts with claim construction principles that ordinarily give meaning to all claim terms. (*Id.* (citing *Akzo*, 811 F.3d at 1340).)

In their reply brief, Respondents repeat their position that "Term No. 5—when read in light of Term Nos. 1-3 and 7 above, which all require the 'buffer circuit' to have a 'fork in the road' layout—is consistent with the 'fork in the road requirement and must be interpreted in that context." (RRMB at 37.) Respondents' also repeat their main point of opposition to Netlist's construction—that it renders superfluous much of the claim term "including the requirement that the buffer circuit is 'configured to isolate.'" (*Id.* at 38.) More specifically and with respect to Figure 5 of the '907 patent, Respondents argue:

> Figure 5 shows that the *only* buffers that are configured (via logic circuit 502, shown in purple) are buffers 504 and 506, which create the "fork in the road" layout by allowing data communication along path A to ranks A and C, while isolating ranks B and D (or vice versa). *See* Ex. 9 at 15:65–16:11, 17:57–18:2; *see also id.* at 11:31–:49 (using the term "configurable" repeatedly to describe a buffer circuit that results in "selectively allowing or inhibiting data transmission between the system memory controller 420 and . . . selected memory devices").

(*Id.* at 38-39.) With this perspective, Respondents continue:

> [T]he specification of the '907 patent never identifies data buffer 503 as being configured to perform the required isolation and data buffer 503 therefore does not selectively isolate the load of the memory devices.

(*Id.* at 39.)

Respondents then address Netlist's criticisms of their own construction, and argue that construction does not require separate circuits, "one to isolate a first memory device and another to

isolate a second memory device." (*Id.* at 39.) Rather, Respondents describe, the use of "separately" in their construction aligns with Figure 5 which involves separate data paths to alternatively isolate a first memory device from a second memory device. (*Id.*)

Respondents also address the technical distinction between isolating a memory device and isolating a memory device load. (*See id.* at 40-41.) Respondent argue their construction does not read out "memory device load" because "when a memory device is isolated, any electrical load from that memory device will also necessarily be isolated, as the examiner determined during prosecution of the '907 patent." (*Id.* (citing RIMB, Ex. 11 at 120, 121).) Respondents also point out that it is the "isolation switch" in Netlist's commercial embodiment of the '907 patent, HyperCloud, that creates the "fork in the road" layout—as evidenced by Netlist's use of HyperCloud to show conception during prosecution. (*Id.* (citing RIMB, Ex. 11 at 173, 178, 179, 191-192, 226-228).)

Regarding judicial estoppel, Respondents dispute it applies to their present arguments because, in their view, they argue exactly what had been argued in the prior 1023 Investigation. (*See id.* at 41.) Respondents do clarify, however, they are "not contending that the phrase 'isolate memory device load,' by itself, requires the 'fork in the road' layout. . . . Rather, Term Nos. 1-3 and 7 require a 'fork in the road,' and the language of Term No. 5—as well as SK hynix's proposed construction for Term No. 5—is consistent with the 'fork in the road' requirement . . ." (*Id.*)

3. Staff's Position

In its opening brief, the Staff explains this term "should be construed to require the capability of isolating only unselected memory devices, as opposed to only being capable of isolating both the selected and unselected memory devices." (SIMB at 52.) The Staff repeats its characterization of the buffer circuit in Netlist's construction as a "dummy" buffer circuit because

it does not isolate between selected and unselected memory devices. (*See id.*) This is inaccurate, according to the Staff, because the context of the claims require "isolating the first and second devices individually." (*Id.*) Alternatively, the Staff argues, language such as "do not . . . receive any communication" would be rendered meaningless. (*Id.*) The Staff acknowledges that this claim term "does not expressly state 'selective' isolation," however. (*Id.*)

In its reply brief, the Staff states, generally, "the best method for understanding the claims is to align the meaning of the claim terms with the invention as disclosed—where the memory buffer selectively communicates to selected memory devices." (SRMB at 14.) The Staff continues:

> As discussed above, the specification teaches that the advantage of load-reduction on the memory controller is achieved by having a selective buffer circuit that electrically couples enabled memory devices (*i.e.* those memory devices enabled for the read or write operation), while electrically separating the other unselected memory devices

(*id.* at 15-16);

> The specification refers to "load" in terms of reduction and "memory devices" in terms of isolation. This distinction is relevant to the dispute regarding the term "each respective buffer circuit is further configured to isolate memory device load...," because the parties dispute whether the term is directed to the "load-reduction" versus "memory device isolation." *See* CIB at 38. The Staff's position, which is explained further below, is that there is no disclosure in the specification of how a buffer circuit "isolates" the entire load and still completes the memory controllers' read or writes operation. Accordingly, load reducing by isolating memory devices, as disclosed in the specification, is how a person of ordinary skill in the art would understand the memory buffer of the '907 patent.

(*id.* at 15-16, n.8).

With respect to the claim term at issue here, the Staff explains its interpretation "is based on the specification's description of 'isolating memory devices' to achieve load reduction on the

memory controller." (*Id.* at 30.) The Staff disputes that there is any disclosure in the '907 patent to draw a distinction of isolating memory devices as opposed to memory device load, as Netlist contends. (*See id.*) The Staff contends that Netlist's supposed support from that specification actually describes load reduction and not isolation. (*Id.* (referring to CIMB at 38).) The Staff reasons:

> Because this memory controller still sees one memory device load, this disclosure does not support Complainant's interpretation of electrically separating all memory device load from the memory controller. CIB at 37-38. At best, this section of the specification may describe a memory buffer configured to *reduce* the load from all of the memory devices connected to the memory buffer.

(*Id.*)

The Staff acknowledges "the heard of the problem is that the specification does not explicitly disclose how to concurrently separate all memory device loads. The specification always refers to reducing the memory device loads to that of one memory device." (*Id.* at 31.) Nevertheless, the Staff argues, "Complainant's proposed construction of isolating all memory device loads from the memory controller is illogical because it would prevent the execution of the desired read or write command (*i.e.* 1 out of 9 buffers needed for the 72 bit write operation)." (*Id.*)

4. Analysis

For this claim limitation, all parties agree that "isolate" means "electrically separate." (CIMB at 36; RIMB at 80; SIMB at 51.) I find the parties' dispute centers on the meaning of "as well as" (claims 1, 16) or "and" as it appears in other claims (claims 43, 58).

To Netlist, "as well as / and" means "in addition to" in the sense that both the first memory device load and second memory device load are "isolated" or "electrically separated" from the system memory controller at the same time. Netlist finds support for its interpretation in the specification which explains how buffers 503 and 509, which are not part of Respondents' alleged

"fork in the road," are responsible (or at least involved) in the isolating of load as seen by the system memory controller. (*See, e.g.*, CIMB at 38 (citing '907 patent at 16:36-44).) Netlist contends these write and read buffers 503 and 509 "do not separately (or selectively) isolate the load of different memory devices connected to the same terminal." (*Id.*)

To Respondents and the Staff, "as well as / and" means "or" in the sense that the first memory device load and second memory device load can individually be "isolated" or "electrically separated" from the system memory controller." Respondents curiously do not argue this is in itself a "fork in the road," but rather "when read in light of Term Nos. 1-3 and 7 above, which all require the 'buffer circuit' to have a 'fork in the road' layout – is consistent with the 'fork in the road' requirement and must be interpreted in that context." (RRMB at 37.) The Staff, at times points to the specification at column 14 which discusses how load-reduction is "desirably achieved" by "electrically couple only the enabled memory devices 412 . . . and to electrically isolate the other memory devices 412 from the memory controller." (SRMB at 13 (citing '907 patent at 14:54-62), 29 (citing '907 patent at 14:54-62).)

I agree with both Netlist and the Respondents and Staff here. The plain and ordinary meaning of "as well as" or "and," in light of the specification, could encompass Netlist's or Respondents' understanding. Further, the '907 patent specification discloses *both* as ways to reduce the load of memory devices as seen by the system memory controller. In furtherance of Respondents' construction, the specification states:

> To reduce the memory device loads seen by the system memory controller 420 (*e.g.*, during a write operation), the data transmission circuit 416 of certain embodiments is advantageously configured to be recognized by the system memory controller 420 as a single memory load. This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller 420 (*e.g.*, the one, two, or more memory devices 412 to which data is to be written) and to electrically isolate

> the other memory devices 412 from the memory controller 420 (*e.g.*, the one, two, or more memory devices 412 to which data is not to be written). Therefore, during a write operation in which data is to be written to a single memory device 412 in a rank of the memory module 400, each data bit from the system memory controller 420 sees a single load from the memory module 400, presented by one of the data transmission circuits 416, instead of concurrently seeing the loads of all of the four memory devices 412A, 412B, 412C, 412D to which the data transmission circuit 416 is operatively coupled. In the example of FIG. 3A, during a write operation in which data is to be written to two memory device 412 in two ranks (*e.g.*, memory devices 412A and 412C or memory devices 412B and 412D), each data bit from the system memory controller 420 sees a single load from the memory module 402, which is presented by one of the data transmission circuits 416, instead of concurrently seeing the loads of all of the four memory devices 412A, 412B, 412C, 412D to which the data transmission circuits 416 is operatively coupled. In comparison to the standard JEDEC four-rank DIMM configuration (*see* FIG. 2A and FIG. 2B), the memory system 402 of certain embodiments may reduce the load on the system memory controller 420 by a factor of four.

('907 patent at 14:50-15:3.) This is a clear teaching that electrically coupling (so data will be written) one set of memory devices while electrically isolating (so data will not be written) the other memory devices achieves a single memory device load presented to an external system memory controller.

The file history of the '907 patent (RIMB, Ex. 11) also supports Respondents. During that prosecution, inventors Lee and Bhakta filed declarations of conception to swear behind a prior art reference Wu. (*Id.*, Ex. 11 at 175-310.) These declarations attach Netlist internal memos drafted by Lee and Bhakta describing the LRD/DXD system which demonstrated the alleged conception. (*Id.*, Ex. 11 at 188-250.) One memo is directed to the functionality of the overall ASIC which corresponds to the module controller as claimed in the '907 patent. (*Id.*, Ex. 11 at 189-222.) The other memo focuses more narrowly on the "Isolation Switches (ISwitch)" which correspond to the "M buffer circuits" of the '907 patent. (*Id.*, Ex. 11 at 224-250.) This latter memo in particular

makes clear the ISwitches provide the LRD (Load Reduction DIMM) and DXD (Density Multiplier DIMM) functionality—as controlled by signals sent from the ASIC. (*Id.*, Ex. 11 at 226.) This memo speaks consistently of the LRD (Load Reduction) feature as coming from the ISwitch which "electrically isolates" or "electrically disconnects" un-accessed DRAMS from the data paths that connect to the external system memory controller. (*See* RIMB, Ex. 11 at 226, 238-239.)

The above intrinsic evidence makes it hard to appreciate a difference, as Netlist contends there to be, between electrically isolating memory device load as opposed to electrically isolating the memory devices themselves. (*See* CIMB at 37 ("Respondents and Staff on the other hand, appear to argue that the memory devices themselves, rather than the 'load' must be isolated. This is contrary to the plain and language of the claim term."); *see also* RRMB at 40 ("when a memory device is isolated, any electrical load from that memory device will also necessarily be isolated").)

There is support for Netlist's construction as well, however. The specification states:

> The data transmission circuits 416 present a load on the data lines 518 from the write buffer 503 and the read buffer 509. The write buffer 503 is comparable to an input buffer on one of the memory devices 412, and the read buffer 509 is comparable to an output buffer on one of the memory devices 412. Therefore, the data transmission circuits 416 present a load to the memory controller 420 that is substantially the same as the load that one of the memory devices 412 would present. Similarly, the data transmission circuits 416 present a load on the first and second terminals Y1, Y2 from the multiplexer 508 and the first tristate buffer 504 (on the first terminal Y1) and the second tristate buffer 506 (on the second terminal Y2). The multiplexer 508 is comparable in loading to an input buffer on the memory controller 420, and the first and second tristate buffers 504, 506 are each comparable to an output buffer on the memory controller 420. Therefore, the data transmission circuits 416 present a load to the memory devices 412 that is substantially the same as the load that the memory controller 420 would present.

(*Id.* at 16:36-55.) While this passage does not mention "isolation" or "electrical separation," it does unequivocally state write buffer 503 and read buffer 509 are configured to be comparable to the load of an input buffer on just one of the memory devices 412 so that the load of just one memory device is presented to the system memory controller; *i.e.*, load reduction. This seems compatible with the claim language, "[electrically separate] memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller." ('907 patent at cl. 1.) Moreover, unlike claims 1 and 16 which use "as well as," claims 43 and 58 simply use "and." It is hard to see how a patent drafter, if they wanted to claim isolating the load of both first and second memory devices at the same time, could use a better word than "and." Moreover, "or" would have been the perfect word for claiming alternate or separate isolation of the memory devices—but "or" is not used in any claim for this feature. ('907 patent at cls. 1, 16, 32, 43, 53, 58.)

Thus, I find it reasonable to construe "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller," as in claims 1 and 16, and similar in claims 43 and 58, broadly so that either simultaneous or alternate isolation is covered.

Accordingly, I construe the limitation in claims 1 and 16 as "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the respective one or more of the second memory devices from the memory controller." I construe the similar limitation in claim 43 as "wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or

more memory devices in the subset of the memory devices from the memory controller and to isolate memory device load associated with the one or more of the other memory devices from the memory controller." Finally, I construe the similar limitation in claim 58 as "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the one or more of the second memory devices from the memory controller."

F. "each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective [module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices / one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices], the each respective buffer circuit including data paths and logic that configures the data paths in response to [the set of module control signals / the first set of module control signals] to allow a respective portion of the data associated with the [first] memory read or write command to be communicated between the memory controller and the respective one or more [memory devices in the subset of the memory devices / of the first memory devices] through the each respective buffer circuit[, wherein the logic subsequently configures the data paths in response to the second set of module control signals ...]"

The term "each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective [module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices / one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices], the each respective buffer circuit including data paths and logic that configures the data paths in response to [the set of module control signals / the first set of module control signals] to allow a respective portion of the data associated with the [first] memory read or write command to be communicated between the memory controller and the respective one or more [memory devices in the subset of the memory devices / of the first memory devices] through the

each respective buffer circuit[, wherein the logic subsequently configures the data paths in response to the second set of module control signals …]" appears in asserted claims 43 and 58 of the '907 patent. These claims read:

> 43. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:
>
> memory devices;
>
> a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command;
>
> a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, **wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit**, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and

memory device load associated with the one or more of the other memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.

....

58. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices including first memory devices and second memory devices;

a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input

address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;

a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, **wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit**, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines, wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first

memory devices and the respective one or more of the second memory devices.

(emphasis added).

The constructions proposed by the parties for the term are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
Plain and ordinary meaning, with the understanding as encompassing, at least, the same understanding as stated for term 1 above.	Plain and ordinary meaning, with the same understanding as stated for term 1 [above, *i.e.* "when considered with the surrounding language of the respective claim, the resulting physical arrangement of the elements of the claim (when given their plain and ordinary meaning) is a 'fork in the road' layout"…], except with "first memory devices" replaced by "subset of the memory devices," and "second memory devices" replaced by "other memory devices not in the subset of memory devices," for claim 43.	N/A

1. Netlist's Position

In its opening brief, Netlist explains that it and Respondents agree this term should be given its plain and ordinary meaning. (CIMB at 45.) Netlist adds that its interpretation reads on an embodiment that is expressly claimed, while Respondents' is "contrived and unsupported." (*Id.*)

In its reply brief, Netlist criticizes Respondents for a 200 word construction that really only turns on "what it means to 'configure[] the data paths' in a buffer circuit." (CRMB at 48 (citing RIMB at 76-79).) Netlist asserts, as with most of the disputed limitations, Respondents argue for

their "fork in the road" layout without a connection to actual claim language, while also acknowledging Respondents have cited the "data paths" term for such a connection. (*Id.*) In response, Netlist argues the data paths Respondents identify in Figure 5 as the claimed "data paths" are wrong. (*Id.* at 49.) Rather, Netlist argues there are four data paths in Figure 5—two "write" paths and two "read" paths, as shown below:

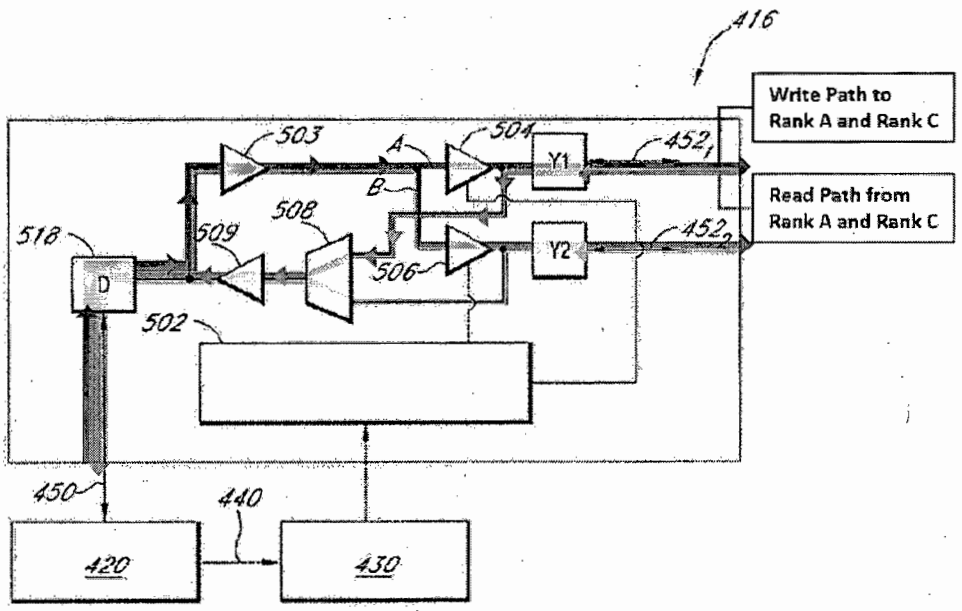


FIG. 5

(*Id.*) Netlist contends "the claimed data paths include both the red write path and the blue read path in the annotated figure above. The claimed data paths are not the two write paths (red and green) that Respondents identify." (*Id.*)

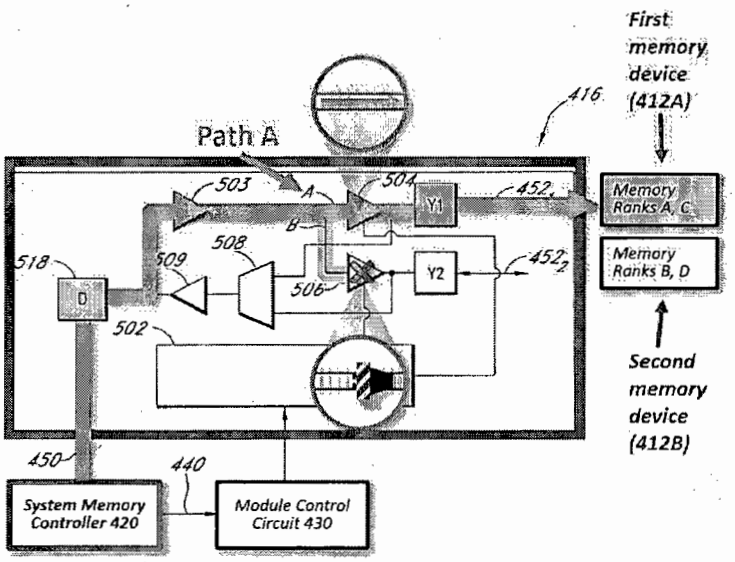
Netlist also addresses the claim language regarding module data lines. (*See id.* at 50.) Netlist explains the limitation which reads:

> [E]ach respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of data lines [450] and respective module data lines that are coupled to respective one or more memory devices in the subset of memory devices and to one or more of the other memory devices [452_1].

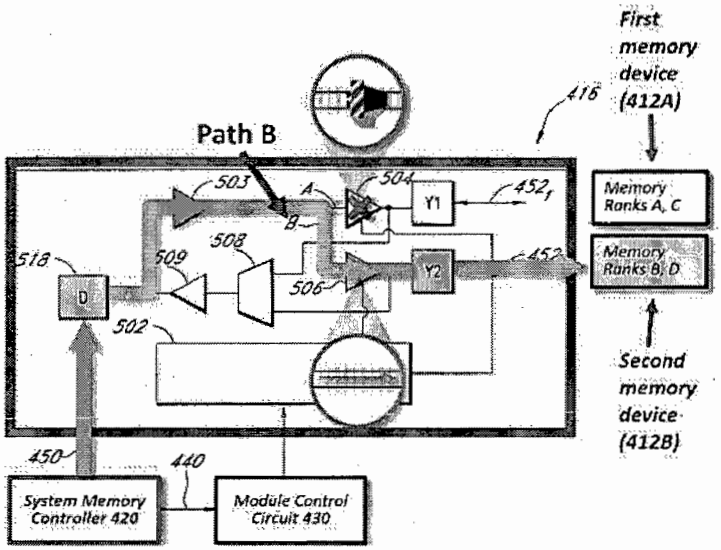
(*id.* (citing '907 patent at 25:44-50) (bracketed numerals added by Netlist)), must mean "the module data lines of claim 43 must be coupled to both the first set of claimed memory devices and to the second set of claimed memory devices" (*id.*). Netlist repeats its reading of the claim as "the claimed 'data paths' are (1) a 'write' path, such as the one annotated in red, and (2) a 'read' path, such as the one annotated in blue"—which does not invoke a "fork in the road." (*Id.*)

2. Respondents' Position

In their opening brief, Respondents again argue this claim language, "when read in the context of the surrounding claim language, as well as the specifications and prosecution histories discussed above," requires the "fork in the road" layout. (RIMB at 76.) Respondents contend that the limitation's use of "data paths" is a direct reference to that portion of the '907 patent specification discussing Figure 5. (*See id.* at 76-77 (citing '907 patent at 15:35-49, 15:65-16:16, 17:6318:2, 18:10-16).) Respondents show their understanding of the "data paths" with the following figures:



(*id.* at 78);



(*id.* at 79).

In their reply brief, Respondents contend this term "provides *additional* reasons (beyond those found in Term No. 2) why claims 43 and 58 require the 'fork in the road.'" (RRMB at 31 (referring to RIMB at 76-79).) Respondents note that adopting their construction for Term No. 2 ("output or receive . . . do not output or receive") resolves this term as well even though Term No. 2 "is not the only reason that claims 43 and 58 require a 'fork in the road.'" (*Id.* at 31-32.) Respondents summarize:

> In particular, the reference in the claim language to "data paths" (plural), and configuring the data paths to "allow" data communication to the "first" memory devices, and then subsequently configuring the data paths to allow data communication to the "second" memory devices, directly ties to the "fork in the road" layout described in the specification and shown in Figure 5. *See id.*

(*Id.* at 32.)

3. Staff's Position

In its opening brief, the Staff notes it does not have a separate position on this claim term—"[a]s noted in the Joint List, the parties do not dispute that the resolution of the issues with respect to Claim 1 would equally apply to claims 43 and 58." (SIMB at 54.)

4. Analysis

At the outset, I disagree with the parties that resolution of the issues in claim 1 ("*n* module data lines) resolves this claim construction issue for claims 43 and 58. As just one example, there is no language in claims 1 or 16 that is comparable to the "configure data paths" language of claims 43 and 58. This is evidenced by the parties' substantive briefing on what is meant by "data paths." (*See* CRMB at 49-50; RIMB at 76-79.)

Further, this limitation is even drafted differently between claims 43 and 58. For example, both claims recite "each respective buffer circuit including data paths and logic that configures the data paths," but only claim 58 recites what the configuration is aimed to do—"allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices" and "to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices." Claim 58 adds that "the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals." Thus, at a minimum, there is reason not to automatically treat claim 58 the same as 43, and neither the same as claims 1 and 16.

With that said, I find both parties have missed the mark with their briefing here. Neither argues for what is meant by a "data path" according to a person of ordinary skill in the art. Rather, the parties dispute which paths shown in Figure 5 of the '907 patent are referred to by the claimed "data paths" in claims 43 and 58. (*See* CRMB at 49-50; RIMB at 76-79.)

I decline to resolve this question as it assumes claims 43 and 58 must match Figure 5 which is an inappropriate starting point for a claim construction analysis. *Superguide*, 358 F.3d at 875 ("The written description, however, is not a substitute for, nor can it be used to rewrite, the

chosen claim language.")). Indeed, the '907 patent specification discloses that the invention can embody variations of Figure 5:

> FIG. 5 schematically illustrates an example data transmission circuit 416 compatible with certain embodiments described herein. In one embodiment, the data transmission circuits 416 includes control logic circuitry 502 used to control the various components of the data transmission circuit 416, which may include one or more buffers, one or more switches, and one or more multiplexers among other components. **The illustrated embodiment of FIG. 5 is 1-bit wide and switches a single data line 518 between the memory controller 420 and the memory devices 412. In other embodiments, the data transmission circuit 416 may be multiple bits wide, for example, 8 bits, and switch a corresponding number of data lines 518.** In a multiple bit wide embodiment, the control logic circuitry 502 may be shared over the multiple bits.

('907 patent at 15:17-31 (emphasis added); *see also* '907 patent at 15:44-51 ("[i]n other embodiments, the driving of write data and merging of read data may be performed over more than two data paths").) Thus, I do not find any actual claim construction issue in the parties' briefs.

To the extent it aids the parties' analysis, however, I do find a certain conflict between Respondents' identification of those two data paths which *must* be the "data paths" referred to in the claims and the claim language itself. Specifically, Respondents' two data paths are only *write* data paths. (*Compare* '907 patent at Fig. 5 with '907 patent at 15:65-16:35.) Yet claim 43 recites the "data paths" are configured so as "to allow a respective portion of the data associated with the memory *read or write* command to be communicated." ('907 patent at cl. 43 (emphasis added).) Claim 58 recites similarly, "to allow a respective portion of the data associated with the first memory read or write command to be communicated . . . to allow a respective portion of the data associated with the second memory read or write command to be communicated." (*Id.* at cl. 58.) The only conclusion to draw from this explicit claim language is that the "data paths" must encompass paths which as a group accomplish writing *and* reading of data to and from memory

devices. This would align with Netlist's identification of four data paths in Figure 5 of the '907 patent—two write paths and two read paths. (*See* CRMB at 49.)

G. "notification signal indicating [at least one / a] status of [the] one or more training sequences"

The term "notification signal indicating [at least one / a] status of [the] one or more training sequences" appears in asserted claim 1, 12, and 21 of the '623 patent. These claims read:

> 1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
>
> a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating **a notification signal indicating at least one status of one or more training sequences** while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
>
> a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.
>
> ....
>
> 12. A memory module to be coupled to a memory controller of a host system, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;

a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode, the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, **the notification signal indicating a status of the one or more training sequences**; and

a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

....

21. A memory module operable in at least a first mode and a second mode, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module

> operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, wherein the PCB is configured to fit into a corresponding slot connector of the host system; and
>
> a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate **a notification signal indicating a status of one or more training sequences** while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

(emphasis added).

The constructions proposed by the parties for the terms are as follows:

Netlist's Construction	**Respondents' Construction**	**Staff's Construction**
"notification signal signaling information about a condition or state of one or more operations related to synchronization"	For all but "one or more training sequences": Plain and ordinary meaning as adopted by the Administrative Law Judge (*e.g.*, "one of ordinary skill in the art arriving at the 'plain and ordinary' meaning of the term 'notification signal' in the context of the '837 patent [and hence the '623 patent] would recognize that it does not utilize polling").	"Notification Signal" - plain and ordinary meaning does not encompass polling. "Indicating at Least One Status" – plain and ordinary meaning, which is conveying information that the memory controller needs and does not already have regarding poignant events (*i.e.* does not encompass signal that passes through memory module and returns to memory controller which utilizes the information to determine a status (*i.e.*

		more than feedback signal). Per the specification, co-extensive with "one or more initialization sequence"

1. Netlist's Position

In its opening brief, Netlist contends its construction should be adopted because "it properly recognizes that 'training' is not equivalent to 'initialization' and is the only construction that is supported by the intrinsic and extrinsic evidence." (CIMB at 48.) Regarding "notification signal," Netlist argues it should be accorded its plain and ordinary meaning—"a signal that notifies"—in light of, *inter alia*, the finding in the 1023 Investigation for the same claim term in the '837 patent. (*Id.* at 49-50.)

Netlist then observes that in the 1023 Investigation, it was determined that, under a plain and ordinary meaning, "notification signal" would be any signal that notifies including in response to polling. (*Id.* at 50.) Netlist also acknowledges, however, that based on the intrinsic evidence and as also determined in that investigation, the term should not encompass polling, *i.e.*, "reading from an addressable status register to determine if the memory subsystem controller has completed the required or requested operation." (*See id.* at 50-51 (citing '623 patent at 4:28-33).) Netlist then cites to Respondents' expert testimony in the 1023 Investigation to support the idea that "reading from a status register is the only form of polling disclosed in the patent's specification." (*Id.* at 51 (citing CIMB, Ex. 7 at 747:4-18; CIMB, Ex. 16 at 72:2-73:8).) Thus, Netlist reasons:

> Accordingly, there can be no dispute that the only operation that applicant disclaimed from the scope of the phrase "notification signal"—which as Chief ALJ Bullock found would otherwise be broad enough to include polling—is reading from an addressable status register to determine if the memory subsystem controller has completed the required or requested operation.

(*Id.* at 52 (citing *Thorner*, 669 F.3d at 1366-67).) Netlist recommends:

> In the event the ALJ finds that the exclusion of "polling" from the meaning of "notification signal" should be made explicit, the ALJ should find—as set forth in the patent's specification and acknowledged by Respondents' own expert—that such "polling" means "reading or querying an addressable status register."

(*Id.*)

Regarding "indicating [at least one / a] status," Netlist argues it should be construed as "signaling information about a condition or state" and notes that Respondents' construction does not even address this language. (*Id.*) Netlist argues the claims and specification "consistently discuss" the claim term "as signaling information about a condition or state of that operation to, for example, a system memory controller of a host computer system." (*Id.* at 53 (citing CIMB, Ex. 2 at 1:55-60; 5:20-26; 7:63-65; 7:65-8:2; 8:2-10; 8:21-22; 10:15-20; 10:36-11:20; 12:43-49).)

At a more technical level, Netlist explains:

> With specific reference to the term "status," there is no requirement that the "status" be indicative of a particular degree of completion of any operation. Rather, the specification clearly contemplates that the "status" can indicate a binary condition or state of an operation. For example, the specification teaches that a "state" (*e.g.*, "status") can be indicated by one of two possible logic levels. Ex. 2, '623 Patent, at 10:36-42. ("the first state of the at least one first output 12 is a first logic level, [and] the second state of the at least one first output 12 is a high impedance state."); *see also id.* at 7:63-65; 7:65-8:2; 8:2-10; 8:48-50; 10:15-20; 10:36-42; 11:13-20; 11:38-48; 11:54-60; 12:41-56.

(*Id.*) Netlist again claims expert testimony from the 1023 Investigation supports this interpretation. (*Id.* (citing CIMB, Ex. 16 at 89:1-5, 166:18-167:5; CIMB, Ex. 7 at 738:15-21, 740:25-741:7, 741:11-25, 742:1-12, 743:9-17, 743:19-744:8, 744:20-745:3, 746:12-23).)

Then, while arguing they need not be considered, Netlist looks to "contemporaneous non-technical dictionaries" for "corroborating definitions consistent with [the] description in the '623

patent." (*Id.* at 54.) For "indicate," Netlist finds a definition of "to serve as a sign, symptom, or token of; signify." (*Id.* (citing CIMB, Ex. 17 at NL1089_00038996-39007).) For "status," Netlist finds a definition, among others, of "information describing the logical state of a point or equipment." (*Id.* (citing, *inter alia*, CIMB, Ex. 18 at NL1089_00039026-38).)

Netlist then discusses the Staff's construction. (*Id.* at 55.) Netlist argues against its adoption because "its further reference to 'more than feedback signal' is unclear and imparts ambiguity into the scope of the claim." (*Id.*) Netlist suggests this detail cannot be gathered from the intrinsic evidence. (*Id.*)

In its reply brief, Netlist confirms that all parties agree "'notification signal' excludes 'polling' by reading and querying an addressable status register." (CRMB at 54 (citing RIMB at 16; SIMB at 58-59).) To the extent the Staff finds the excluded subject matter to be larger than this form of polling, Netlist disagrees. (*Id.*) More specifically, Netlist states "Staff argues incorrectly, however, that any 'information that repeatedly shows that an operation is not complete would be considered 'polling,'' and is also excluded from the scope of the claimed 'notification signal.'" (*Id.* (referencing SIMB at 59-60).) Netlist claims the '623 patent specification actually discloses that a "notification signal" may comprise an indication that an operation is still running and therefore not yet complete. (*Id.* at 54-55 (citing '623 patent at 7:61-65).) Netlist contends Respondents agree with this (*id.* (citing RIMB at 17)) and that the same was determined in the prior 1023 Investigation (*id.* (citing CRMB, Ex. 35 at 95)). Thus, Netlist reasons, "notification signal" should not be limited to notifications that operations have been completed. (*Id.*)

Moving on, Netlist argues several reasons why the construction should not be construed to exclude feedback signals that merely pass through the memory module. (*Id.*) "First," according to Netlist, "Respondents and Staff do not point to any evidence to support their contention." (*Id.* at 55-56 (citing SIMB at 59; RIMB at 18).) To the contrary, Netlist quotes the '623 patent

specification with "[c]ertain embodiments described herein . . . [provide] a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller." (*Id.* at 56 (citing '623 patent at 3:43-48) (emphasis added by Netlist).)

Second, according to Netlist, the interpretation wrongly relies on extrinsic evidence of accused product technical documentation from the 1023 Investigation. (*Id.*) Setting that impropriety aside, Netlist argues the 1023 Investigation did not actually determine that "'notification signal' . . . necessarily excludes a signal that traverses a feedback path." (*Id.*) Rather, "the 1023 ID only found that the accused 'Alert_n' signal did not provide a status of 'initialization.'" (*Id.* (citing, *inter alia*, CRMB, Ex. 35 at 95-96).)

Moving on to "indicating [at least one / a] status," Netlist argues "Respondents and Staff do not genuinely dispute the propriety of Netlist's construction . . . but instead seek to unduly narrow the term by reading in an extraneous requirement for a status of 'poignant' or 'significant' events." (*Id.* at 57 (referring to SIMB at 57-60; RIMB at 17-18).) Netlist observes that the '623 specification does not use the words "poignant" or "significant," but, to the contrary, explains that the notification signal may indicate an operation is executing or completed. (*Id.* at 58 (citing '623 patent at 7:61-65, 8:2-6).) Netlist suggests that adding "significant" or "poignant" only serves to introduce further ambiguity. (*See id.* at 59.)

Netlist finally asserts that Respondents and the Staff mischaracterize its construction. (*Id.*) According to Netlist, it does not read "status" out of the claim, but rather, uses the plain and ordinary meaning of the term "evidenced by the patent's intrinsic record, and the well-known meaning of these words as readily demonstrated by dictionary definitions." (*Id.*) Again, as Netlist contends, "indicate" means "signify" and "status" means "information describing the logical state of a point or equipment" or "the condition at a particular time of a system or system component." (*Id.* (citing CIMB, Ex. 17 at 705; CIMB, Ex. 18 at 1044).)

2. Respondents' Position

In their opening brief, Respondent contend this claim term (that language apart from "training sequences") is due its plain and ordinary meaning—a meaning which excludes "polling." (RIMB at 16.) Respondents point to those statements in the '623 patent specification which contrast a notifying method of handshaking with a polling method. (*See id.* at 16-17 (citations omitted).) Respondents also provide several specification excerpts as examples of the "status" which is so indicated. (*See id.* at 17 (citing '623 patent at 7:58-8:6, 9:34-40).)

Respondents also state they agree with the Staff in that "to indicate status, the notification signal must be conveying information that the memory controller needs and does not already have regarding poignant events." (*Id.* at 18.) As an example of what would *not* be covered, Respondents describe "a signal provided by a memory controller that passes through a memory module and returns to the memory controller which then utilizes the information to determine a status." (*Id.* (citing RIMB, Ex. 7 at 95-96).)

On the other hand, Respondents view Netlist's construction as improperly reading "status" out of the claim. (*Id.*) Effectively, Respondents disagree that "status" can be substituted with "condition or state" because, for example, the '623 patent specification does not use these terms. (*See id.*)

In their reply brief, Respondents accuse Netlist of "essentially reduc[ing] the limitation 'signal indicating . . . status' to just 'signal,' albeit in a convoluted manner." (RRMB at 42.) Apart from this substantive dispute, Respondents also argue Netlist should be precluded from arguing its "condition or state" construction for two reasons. (*See id.* at 44.) First, Respondents argue the Commission in the prior 1023 Investigation already effectively construed this term, against Netlist—and thus, assumedly, issue preclusion applies. (*See id.* (citing RIMB, Ex. 7 at 85, 95-96; RRMB, Ex. 57 at 1).) Second, and in a similar vein, Respondents argue Netlist had the

opportunity to argue its current proposed construction in the 1023 Investigation, but did not, thereby waiving its ability to do so now. (*See id.* at 44-45.)

Moving back to the substance, Respondents flatly argue Netlist's construction renders the term meaningless by conflating "signal" with "indicating status." (*Id.* at 45.) More specifically, Respondents take the position that Netlist's invocation of "status" as, potentially, one of two possible logic levels (*id.* (citing CIMB at 53)), covers any digital signal because "[*a*]*ll* digital signals have a binary state of high or low (*id.* (citing RRMB, Ex. 58 at 157, 159)). Respondents continue, "[m]oreover, whether a signal is binary (*i.e.*, 'one of two possible logic levels') does not mean it 'indicates . . . status.'" (*Id.* at 46 (citing RIMB, Ex. 7 at 95-96).)

Respondents then state flatly, "[n]o intrinsic evidence supports Netlist's proposed construction." (*Id.* at 46.) Rather, according to Respondents, "throughout the specification, the '623 patent makes clear that "indicating . . . status" means that the signal is *indicative* of the *status* of the sequence, not merely *signaling* some information about the condition or state of the sequence." (*Id.* (citing '623 patent at 7:58-8:6, 9:34-40).) Respondents do acknowledge, however, that "a particular 'status' may very well be 'indicated' to the memory controller by driving the 'output' to a particular 'logic level.'" (*Id.* at 47.) Nevertheless, Respondents maintain "[t]hat a signal simply takes a high or low state, does not mean that it necessarily indicates a status, as the Commission held with respect to the same training sequences accused here." (*Id.* at 47-48 (citing RIMB, Ex. 7 at 95-96; RRMB, Ex. 57 at 1).)

Respondents then contend that Netlist has offered a contrasting construction in a parallel district court proceeding. (*Id.* at 48.) According to Respondents:

> On June 16, 2016, Netlist asserted in district court that "at least one notification signal to the memory controller *indicating at least one status* of the at least one initialization sequence" means "a signal providing notification to the memory controller *indicating whether a certain task, such as a training task* requested by the system

> memory controller, of at least one initialization sequence, *has been completed or is still being executed*" for the '837 patent. Ex. 59, Netlist's Amended Opening Claim Construction Brief, Case 8:16-cv-01605, Dkt 139 at 20-22 (emphasis added). Thus, in the 1023 Investigation, Netlist asserted plain and ordinary meaning for this phrase based on the intrinsic evidence, and in the companion district court case, Netlist asserted this phrase meant "*indicating whether certain task, such as a training task has been completed or is still being executed.*"

(*Id.*)

Respondents then consider extrinsic evidence, and dispute that their own expert admitted "status" can be binary. (*See id.* at 49.) Rather, Respondents argue their expert "testified that the Alert_n signal, which always will be high or low, does not indicate any status." (*Id.* (citing RRMB, Ex. 61 at Q239-240).) Respondents also criticize Netlist for relying on "truncated portions of dictionary definitions" and argue that "extrinsic evidence 'may not be used to 'contradict claim meaning that is unambiguous in light of the intrinsic evidence.'" (*See id.* at 50 (citing CIMB at 54; *Summit 6, LLC v. Samsung Elec. Co., Ltd.*, 802 F.3d 1283, 1290 (Fed. Cir. 2015).)

3. Staff's Position

In its opening brief, the Staff argues "Complainant's proposed constructions are designed to manufacture a material difference between the claims adjudicated in the 1023 investigation and claims asserted in this investigation." (SIMB at 56.) For the claim term at issue here, the Staff considers the findings in the 1023 Investigation to be informative. (*Id.* at 58.) The Staff argues "the 1023 ID's finding that 'polling' is not within the scope of 'notification signal' should apply for the reasons stated therein." (*Id.* at 58-59.) In the Staff's view, the '623 patent specification describes "notifying" as "sending a signal upon completion, and is distinguished from the inefficiencies of 'polling,' which includes intermittent reading of a register." (*Id.* at 59 (citing '623 patent at 4:25-55).) The Staff adds:

> More specifically, the specification supports construing the limitation to exclude feedback signals that merely pass through the memory module. *See* 1023 ID at 96. Instead, the specification explains that the "notification signal" conveys information that the memory controller needs and does not already have regarding significant events (*e.g.* completion of requested operation), and is distinguished from where a memory controller inefficiently and repeatedly reads a register prior to the significant event.

(*Id.* at 59-60.) The Staff contends that Netlist's construction, through its use of "condition or state" to define "status," may improperly cover "polling." (*Id.* at 60.) The Staff asserts "[a]s discussed in the specification passage cited above [('623 patent at 4:25-55)], information that repeatedly shows that an operation is not complete would be considered 'polling.'" (*Id.*)

In its reply brief, the Staff views Netlist as arguing that the terms "indicate . . . status" should receive a different meaning than the same words were given in the 1023 Investigation. (SRMB at 35-36 (citing, *inter alia*, CIMB at 55).) The Staff also views Netlist as agreeing "notification signal" does not include polling. (*Id.* at 37-38 (citing CIMB at 50-51).) The Staff also, however, argues "'indicating a status' would be understood to mean the notification signal conveys to the memory controller a significant event in the operation, which is how the specification differentiates 'notifying' from 'polling.'" (*Id.* at 40-41 (citing '623 patent at 4:25-55).) The Staff also views Netlist's construction as redundant by its substitution of "signaling information" for "indicate a status," as the literal claim language already recites "a notification signal." (*See id.* at 42.)

4. Analysis

For this claim term, I find the plain and ordinary meaning controls and, based on the intrinsic evidence, that plain and ordinary meaning is quite broad. Taken together, the parties' proposed constructions involve several issues.

First, I agree with all of the parties that the claim term does not encompass polling—by its plain language. The '623 patent describes polling:

> In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). . . . Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

('623 patent at 4:28-47.) This explanation is simply incompatible with the '623 patent claims' recitation of a module controller generating a notification signal and transmitting that notification signal to the memory controller of the external host system via an edge connection on the memory module. (*See, e.g.*, '623 patent at cl. 21.)

Second, I disagree with Respondents and Staff that the "status" can only relate to poignant or significant events. The '623 patent specification does not describe, imply, or suggest any delineation between significant or insignificant states such that some would be a "status" and some are not. Rather, this interpretation seems to be an attempt to read in the overall purpose of the invention into the claims:

> In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling

> generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.
>
> Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory sub system controller.

('623 patent at 4:27-56.) Put another way, the '623 patent describes its notification signal invention as advantageous because it avoids wasting the external memory controller's (MCH) time in reaching out to the module controller to determine if initialization or training sequences are complete when those sequences have not been completed. The '623 patent continues:

> For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a "Wait" state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the "Wait" state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

(*Id.* at 8:30-45.)

Reading this aspect of the invention into "notification signal indicating [at least one / a] status of [the] one or more training sequences" is inappropriate, however. The '623 patent's specification is clear that the notification signal can also communicate that an initialization or training sequence is in a state of "execution" in addition to "completion:"

> The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module **10**, such as a training task requested by the system memory controller **14**. In certain embodiments, the notification circuit **20** can be configured to drive the at least one output **12** to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

('623 patent at 7:58-8:10.) For what it is worth, this "execution" versus "completion" dichotomy also appears in the claims of family member patents to the '623 patent:

> 2. The memory module of claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.
>
> 3. The memory module of claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

(U.S. Patent No. 8,489,837 at cls. 2, 3);

> 2. The memory module of claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.
>
> 3. The memory module of claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

(U.S. Patent No. 9,311,116 (the "'116 patent") at cls. 2, 3).

Regarding the Staff's argument on "more than a feedback signal" so that the construction should "exclude feedback signals that merely pass through the memory module" (SIMB at 59), I agree with Netlist that this detail cannot be gathered from the specification and further ambiguities are introduced as to how a feedback signal would pass through the memory module. Indeed, the only time the '623 patent specification mentions "feedback" is in passing:

> Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

('623 patent at 3:43-48.)

Accordingly, I find intrinsic evidence supports Netlist's construction, wherein "notification signal" does not encompass polling and "indicating [at least one / a] status of [the] one or more training sequences" is not limited to indicating the completion of sequence.

H. "one or more training sequences"

The term "one or more training sequences" appears in asserted claims 1, 3, 5, 11, 12, 13, 21, 23, and 29 of the '623 patent. These claims read:

> 1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
>
> a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of **one or more training sequences** while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
>
> a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory

module operates in the first mode and the notification signal while the memory module is in the second mode.

. . . .

3. The memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the **one or more training sequences**.

. . . .

5. The memory module of claim 1, wherein the **one or more training sequences** are executed by the module controller in response to a command or a signal received from the memory controller of the host system.

. . . .

11. The memory module of claim 1, wherein the module controller implements the **one or more training sequences** in response to a signal or a command received from the memory controller of the host system.

12. A memory module to be coupled to a memory controller of a host system, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;

a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode, the module circuit causing the memory module to enter a second mode in response to a command from the memory controller

of the host system, the module circuit generating a notification signal in response to **one or more training sequences** while the memory module is in the second mode, the notification signal indicating a status of the **one or more training sequences**; and

a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

13. The memory module of claim 12, wherein the memory module executes the **one or more training sequences** in response to a signal or a command from the memory controller of the host system.

. . . .

21. A memory module operable in at least a first mode and a second mode, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, wherein the PCB is configured to fit into a corresponding slot connector of the host system; and

a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, the module controller being further configured to

> cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of **one or more training sequences** while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.
>
> . . . .
>
> 23. The memory module of claim 21, wherein the memory module executes the **one or more training sequences** in response to a command or a signal received from the memory controller of the host system.
>
> . . . .
>
> 29. The memory module of claim 21, wherein the module controller is further configured to implement the **one or more training sequences** in response to a signal or a command received from the memory controller of the host system.

(emphasis added.)

The constructions proposed by the parties for the terms are as follows:

Netlist's Construction	Respondents' Construction	Staff's Construction
"one or more operations related to synchronization"	"a type of initialization sequence that trains without correcting errors"	Per the specification, co-extensive with "one or more initialization sequence"

1. Netlist's Position

In its opening brief, Netlist views the dispute over this term as whether "one or more training sequences" is co-extensive with "at least one initialization sequence." (CIMB at 56.) Netlist argues it is not because, *inter alia*, "the '623 patent specification contains clear statements that the inventor intended for 'one or more training sequences' to be a discrete part of an overall initialization sequence, not coterminous with an initialization sequence." (*Id.*)

Netlist claims intrinsic evidence supports its construction. (*Id.* at 57.) Specifically, Netlist cites that portion of the '623 patent specification which reads, "[i]n one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences." (*Id.* at 57-58 (citing '623 patent at 6:53-58, 7:3-14; *see* '623 patent at 4:40-44, 12:37-40).) Netlist argues the specification's use of "*e.g.*" is not definitional. (*Id.* at 58 (citing *Interval Licensing LLC v. AOL, LLC.*, 766 F.3d 1364, 1373-74 (Fed. Cir. 2014)).) Netlist also looks to deposition testimony from the 1023 Investigation from Respondents' expert witness to support the idea that "not all initialization sequences include training sequences." (*Id.* (citing CIMB, Ex. 16 at 95:4-98:7).) In light of this, Netlist reasons "[t]he intrinsic record supports Netlist's contention that 'an initialization sequence' is not coterminous with 'one or more training sequences.'" (*Id.* at 59.)

Netlist then addresses extrinsic evidence with the acknowledgement that the '623 patent specification "does not include (and need not have included) an express definition for either [training or initialization sequence]." (*Id.*) Netlist explains:

> These were commonly used terms at the time of the '623 patent, as evidenced by technical dictionaries and the testimony of Respondents' own expert.
>
> A person of ordinary skill in the art would understand (1) "training" to generally mean "synchronizing" and, in contrast, (2) "initializing" to generally mean "set[ting] a variable, register, or other storage location to a starting variable." Technical dictionaries at the time of the '623 patent, as well as the testimony of Respondents' technical expert in the 1023 Investigation, support this understanding.

(*Id.* at 59-60 (citing, *inter alia*, *Phillips*, 415 F.3d at 1317-18; *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008).) To this end, Netlist identifies the definition of "training" from an IEEE Standard Dictionary of Electrical and Electronics Terms as "the process of synchronizing the receiver circuit of a line to the incoming data stream during initialization." (*Id.* (citing CIMB, Ex. 18 at 1127).) Netlist notes the same dictionary defines "initialize" as "to

set a variable, register, or other storage location to a starting variable." (*Id.* (citing CIMB, Ex. 18 at 523).) Netlist reasons, "[i]n this way, a component can perform training (synchronization) procedures and then perform initialization (*e.g.*, by setting a correct variable or parameter)." (*Id.*)

Netlist then points to Respondents' expert's deposition testimony where he described a training sequence as "a process you go through where you try to tune the timing of the signals in order to provide optimum performance." (*Id.* at 61 (citing CIMB, Ex. 16 at 49:3-12).) Netlist also concludes the parties agree that "sequences" generally means "operations." (*Id.* (citing CIMB, Ex. 18 at 970; CIMB, Ex. 19 at 473).) Thus, according to Netlist, one of ordinary skill would understand "training sequences" to be "one or more operations related to synchronization." (*Id.* at 62.)

In its reply brief, Netlist repeats its argument and collection of evidence that "training sequence" is not coterminous with "initialization sequence." (*See* CRMB at 61.) Netlist adds that "training" is not a type of "initialization," and discusses at length its views on the determinations made in the prior 1023 Investigation. (*See id.* at 62-67.) In relevant part, Netlist argues that investigation confirmed Netlist's contention that "an 'initialization sequence' may include, but does not necessarily include, a 'training sequence.'" (*Id.* at 64.)

Netlist then addresses other of Respondents' criticisms. (*See id.* at 67-68.) Netlist disputes the importance of the lack of "synchronization" in the '623 patent specification. (*Id.* at 67.) Netlist argues, "there is no requirement in the law that a claim construction must use only words found in the patent's specification." (*Id.* (citing *Helmsderfer*, 527 F.3d at 1382).) Then, Netlist points to the focus of the '623 patent on "synchronous dynamic random access memory elements," and a dictionary definition of "synchronous" as "a mode of transmission in which the sending and receiving terminal equipment are operating continuously at the same rate and are maintained in a desired phase relationship by an appropriate means." (*Id.* (citing CRMB, Ex. 41 at 1075).) Netlist

argues "[a] POSITA understands that such 'appropriate means' for achieving such 'synchronous' behavior includes 'training,' *i.e.*, training is the mechanism to achieve such synchronization." (*Id.* at 68.) Netlist continues, "[t]he '623 patent specification was not required to recite such material that would have been understood by a person of ordinary skill in the art." (*Id.* (citing *Innova/Pura Water*, 381 F.3d at 1116).)

Lastly, Netlist disputes that it has disclaimed any scope of "one or more training sequences" through its submissions as part of *inter partes* review. (*Id.*) Specifically, in Netlist's view, it's submission only stated why Respondents' "argument is illogical, not that 'training' has the particular meaning Respondents have advocated to the PTO—but did not press in this Investigation until now." (*Id.* at 70.) Regardless, Netlist argues, "[t]he notion that 'training' could occur in one mode of operation to 'prevent errors' in another mode of operation is entirely consistent with the '623 patent specification and Netlist's proposed construction." (*Id.* at 71.)

2. Respondents' Position

In their opening brief, Respondents argue the term should be given its plain and ordinary meaning "consistent with the specification of the '623 and '837 patents and their prosecution history (and CALJ Bullock's findings in the 1023 Investigation) *save one disclaimer*." (RIMB at 9 (emphasis added).) Respondents observe that the word "training" appears ten times in the shared specification of the '837 and '623 patents. (*Id.* (citing '623 patent at Abstract, 1:55-60, 2:30-34, 3:5-13, 4:20-26, 4:40-44, 6:50-65, 7:3-14, 7:65-8:10, 8:25-29).) Respondents argue "[t]he only take away of note is that the patents consider 'training' a type of 'initialization.'" (*Id.* at 9-10.)

Respondents contend Netlist "agreed that a 'training sequence' was a type of 'initialization sequence' and needed no construction" in the 1023 Investigation. (*Id.* at 10. (citing RIMB, Ex. 55 at 77).) Respondents point to infringement contention filings from that investigation for support,

as well as determinations made by the Commission. (*See id.* at 10-11 (citing RIMB, Ex. 50 at 6-7, 17; RIMB, Ex. 55; RIMB, Ex. 7 at 90-91).) Respondents restate their position that "a 'training sequence' is a type of initialization sequence." (*Id.* at 12.)

Moving to Netlist's construction, "one or more operations related to synchronization," Respondents describe this as an "attempt[] to rewrite the claims apparently to run away from the non-infringement holding in the 1023 Investigation based on the '837 patent limitation 'notification signal . . . indicating at least one status of the at least one initialization sequence.'" (*Id.* (citing RIMB, Ex. 7 at 93-96).) Respondents note the '623 patent specification does not use the term "synchronization." (*Id.*)

Respondents move on to what they view as an explicit disclaimer made during an *inter partes* review of the '623 patent. (*Id.* at 13.) Specifically, Respondents argue Netlist disclaimed the scope of "training sequences" in an effort to distinguish the "Hazelzet" reference (U.S. Pub. No. 2008/0098277). (*Id.* at 13-14 (citing RIMB, Ex. 51; RIMB, Ex. 52 at 10-12).) Respondents highlight the following statements:

> To be sure, Hazelzet's UE (uncorrectable error) signal and ECC (error correction code) MODE are concerned in some way about errors, but a POSITA knows that these error correction teachings reflect the fact that Hazelzet's design expects errors. (Ex. 2001, Murphy Decl., ¶ 34.) In direct contrast, Hynix's "training" avoids errors. Extending Hynix's "avoid errors" statement (a) logically, Hynix's "training" connotes preventative preparation against future error "during normal operation," but a POSITA knows that error correction connotes corrective recovery from past error. Preventing error is not correcting error. (*Id.*)
>
> ...
>
> If anything, Hynix and Dr. Alpert's statement (a) puts a spotlight on the flaw in their technological proposal that a POSITA would easily notice: the technical design purpose of Hynix's "training" is to "avoid errors," but that is distinct from the fundamental technical design purpose of Hazelzet's ECC MODE UE signal (Hynix's "notification signal") being usage to correct errors. (Ex. 2001,

> Murphy Decl., ¶ 36.) Again, avoiding error is not correcting error. As Hazelzet's ECC MODE UE signal is clearly designed for an original technical purpose of usage in error correction, Hynix simply talking about a different technical purpose of training [*i.e.*, avoiding errors] does not make it obvious to re-purpose Hazelzet's ECC MODE UE signal into Hynix's "training" of "avoid[ing] errors during normal operation."

(*Id.* at 14 (citing RIMB, Ex. 52 at 10-12) (emphases removed).) Respondents contend that these statements, regardless of whether they are adopted by the PTAB, function as clear and unmistakable prosecution disclaimer. (*Id.* at 14-15 (citing *Aylus Networks, Inc. v. Apple, Inc.*, 856 F.3d 1353, 1360 (Fed. Cir. 2017); *Revolution Eyewear, Inc. v. Aspex Eyewear, Inc.*, 175 F. App'x 350, 356 (Fed. Cir. 2006); *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 994–95 (Fed. Cir. 2003); *Laitram Corp. v. Morehouse Indus.*, 143 F.3d 1456, 1462 (Fed. Cir. 1998)).)

In their reply brief, Respondents clarify the effect of Netlist's alleged disclaimer as resulting in a construction of "a type of initialization sequence that trains without correcting errors." (RRMB at 55.) Respondents also dispute that "training sequence" has any kind of "unique definition," as promoted by Netlist. (*See id.* at 56.) Respondents argue:

> But the law is clear that, while a patentee can act as his or her own lexicographer, he or she must define that term in the specification "with reasonable clarity, deliberateness, and precision" and must also "'set out his uncommon definition in some manner within the patent disclosure' so as to give one of ordinary skill in the art notice of the change" in meaning. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (quoting *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992)). Netlist cannot come close to satisfying that standard here.

(*Id.* at 56.) Respondents contend the entirety of Netlist's alleged intrinsic evidence is the patent's disclosure that an initialization sequence can include training sequences. (*Id.* at 57 (citing CIMB at 56-59).) Respondents point out that this is an admission there is no intrinsic evidence for Netlist's "unique definition." (*Id.*) Respondents also point out that in the prior 1023 Investigation, Netlist argued "'initialization sequence' was a well-known term with a plain and

ordinary meaning to which the specification of the '837 patent (and thus the '623 child patent) imparted no special meaning." (*Id.* (citing RRMB, Ex. 62 a 330).) Respondents thus argue that it is "implausible" to believe "initialization sequence" has a plain meaning unchanged by the specification while "training sequence" "is used in the specification in such a way to impart a 'unique definition.'" (*Id.* at 58.) Respondents add that Netlist also failed to allege the "unique definition" for "training sequence" in the pending *inter partes* review proceeding which focuses on this claim term. (*Id.* at 58, n. 12.)

Respondents then move to Netlist's cited extrinsic evidence and argue that the definitions have limited value because Netlist does not actually adopt any of them over its own "unique definition." (*See id.* at 59.) Respondents allege Netlist has engaged in picking-and-choosing words from each of the definitions to create its own, which is not favored by the law. (*Id.* at 59-60 (citing *Phillips*, 415 F.3d at 1322).) Similarly, Respondents dispute that their expert's deposition supports Netlist's construction; but, instead, was discussing functionality in the accused products which should not be considered in claim construction. (*Id.* at 60 (citing *Vita-Mix Corp. v. Basic Holdings, Inc.*, 581 F.3d 1317, 1324 (Fed. Cir. 2009); CIMB at 55).) Again, Respondents view Netlist's proposed construction as "intended to circumvent the Commission's decision in the 1023 Investigation." (*Id.*)

3. Staff's Position

In its opening brief, the Staff argues flatly that "one or more training sequences" is co-extensive with the "at least one initialization sequence" claim term from the '837 patent at issue in the 1023 Investigation. (SIMB at 56-57 (citing '623 patent at 6:50-60, 7:5-15).) The Staff adds:

> To the extent a construction is required, the specification supports the 1023 ID's findings that correlate "one or more training sequence" to "at least one initialization sequence." Further, the specification supports the ID's analysis that "notification signal

> indicating a status" must be more than intermittent reading of a register, which is distinguished by the specification as "polling."

(*Id.* at 64.) The staff repeats the same position in its reply brief. (*See generally* SRMB at 43-44.)

4. Analysis

For this limitation, I find an overall lack of intrinsic evidence to explain the meaning of "training sequences." Neither it nor "initialization sequence" are given any technical definition in the '623 patent specification apart from referring to "initialization sequence (*e.g.*, comprising one or more training sequences)" ('623 patent at 6:55-57), or "initialization sequence (*e.g.*, one or more training sequences)" (*id.* at 7:7-8). This is acknowledged by all parties. (CIMB at 59; RIMB at 9-10; SRMB at 43.)

The '623 patent also introduces a "training *mode*" in its claims to characterize the second mode of the memory module which is not the normal operational mode. ('623 patent at cls. 4, 14, 22.) This is interesting because the specification never uses this term, opting instead for "initialization mode," which it uses twenty-four times to refer to the same mode—that which is not the normal operational mode. ('623 patent at 5:13-26, 6:50-65, 7:34-47, 8:30-33, 8:46-53, 8:54-9:16, 9:55-61, 10:7-11, 12:6-23, 12:33-37, 12:41-43, 12:57-63, 12:66-13:5, 13:30-36.) No prior family members use "training mode" in their specifications or claims either. (*See generally* '837 patent; '116 patent.) I find this sudden and complete switch suggests interchangeability between "initialization" and "training" as far as the invention of the '623 patent is concerned. In total, the intrinsic evidence communicates that "training" and "initialization" are, broadly, those processes and operations the memory module undergoes when it is not in normal operational mode to prepare for operational mode.

As Netlist argues, however, I find this ambiguity invites consideration of extrinsic evidence to determine what "training sequence" would mean to a person having ordinary skill in

the art. *See generally Phillips*, 415 F.3d at 1317-1318. Indeed, this is exactly where Netlist's "operations related to synchronization" construction comes from—an IEEE dictionary (CIMB, Ex. 18); a transcript of a deposition from one of Respondents' experts from the 1023 Investigation (*Id.*, Ex. 16); and that expert's report from the same investigation (*Id.*, Ex. 24). Of these, I find the IEEE dictionary to be reliable and probative of the issue.

The IEEE definition reads:

> **training (1)** The process of synchronizing the receiver circuit of a linc to the incoming data stream during initialization.
> (C/MM) 1596-1992
> **(2) (Training_Up, Training_Down)** A link control signal indicating that the sending entity is either requesting or giving permission to train (initialize) the link.
> (C/LM) 802.12-1995

(CIMB, Ex. 18.) While not cited by Respondents, I find this definition is consistent with their Exhibit 61, which is an expert witness statement from the prior 1023 Investigation. At Question 96, the witness refers to a JEDEC standard which "defines 'training' of the memory controller in Section 2.14 of the RCD02 standard (or Section 2.12 of the RCD01 standard)." (RRMB, Ex. 61 at Q96.) Later on, the witness quotes the JEDEC DDR4 RCD01 and RCD02 definition as "assist the memory controller in aligning the incoming command/address and column address signals optimally to the input clock signal. . . ." (*Id.*, Ex. 61 at Q104.)

I understand "aligning signals to a clock signal" from the JEDEC standard and "synchronization" from the IEEE dictionary to be analogous concepts. Taken together, I find this extrinsic evidence supports Netlist's construction of "one or more operations related to synchronization" as a plain and ordinary meaning to those having ordinary skill in the art. Tellingly, Respondents do not offer their own extrinsic evidence in opposition. Instead, they argue the IEEE definition "is not Netlist's definition, rendering the dictionary meaningless."

(RRMB at 59.) I disagree that the dictionary is meaningless because of Netlist's failure to adopt it *verbatim*—but I do observe that there are details in the definition, and in the JEDEC definition, which are left out of Netlist's construction without explanation. Accordingly, I find a modified version of Netlist's construction is appropriate.

With respect to Respondents' construction which excludes "correcting errors" from the process of training, I do agree that Netlist's response to Respondents' *inter partes* review petition instructive and valuable, as intrinsic evidence under *Aylus*, 856 F.3d at 1360. (RIMB, Ex. 52.) I ultimately find Netlist's explanation of this issue more persuasive, however. Netlist merely pointed out how "[prior art] Hazlezet's error correction functionality does not square with Respondents' characterization of 'training.'" (CRMB at 70.) This does not amount to a "clear and unmistakable" of disclaimer required to exclude training which corrects errors from "training sequence."

In sum, I find the intrinsic evidence ambiguous and the extrinsic evidence persuasive towards a plain and ordinary meaning of "training sequence" as "one or more operations related to synchronization of a receiver circuit to an incoming data signal."

VI. CONCLUSIONS OF LAW

In accordance with the foregoing, the parties' disputes are resolved as follows:

Term	Determination
"output or receive ... data" / "do not output or receive any data" ('907 patent at cls. 1, 16, 43, 58)	means "transmit or acquire / do not transmit or acquire" and does not require a "fork in the road"
"[M buffer circuits / each respective buffer circuit] being [operatively] coupled to . . . [a] respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines" ('907 patent at cls. 1, 16)	means the first and second memory devices are both connected to the buffer circuit through the same set of *n* (as a number of) module data lines
"the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines" ('907 patent at cl. 1)	does not mean "*selectively* allowing communication" or a "fork in the road"
"produc[e/ing]" ('907 patent at cls. 1, 16, 43, 58)	means "create, *i.e.*, bring into existence"
"wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more [of the first memory devices / memory devices in the subset of the memory devices] [as well as / and] memory device load associated with the [respective] one or more of the [second / other] memory devices from the	as in claims 1 and 16, means "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the respective one or more of the second memory devices from the memory

memory controller" ('907 patent at cls. 1, 16, 43, 58)	controller" as in claim 43, means "wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices from the memory controller and to isolate memory device load associated with the one or more of the other memory devices from the memory controller" as in claim 58, means "each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices from the memory controller and to isolate memory device load associated with the one or more of the second memory devices from the memory controller"
"each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective [module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices / one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices], the each respective buffer circuit including data paths and logic that configures the data paths in response to [the set of module control signals / the first set of module control signals] to allow a respective portion of the data associated with the [first] memory read or write command to be communicated between the memory controller and the respective one or more [memory devices in the subset of the memory devices / of the first memory	the recited "data paths" must encompass paths which as a group accomplish writing *and* reading of data to and from memory devices

devices] through the each respective buffer circuit[, wherein the logic subsequently configures the data paths in response to the second set of module control signals …]" ('907 patent at cls. 43, 58)	
"notification signal indicating [at least one / a] status of [the] one or more training sequences" ('623 patent at cls. 1, 12, 21)	"notification signal" does not encompass polling and "indicating [at least one / a] status of [the] one or more training sequences" is not limited to indicating the completion of a sequence
"one or more training sequences" ('623 patent at cls. 1, 3, 5, 11, 12, 13, 21, 23, 29)	means "one or more operations related to synchronization of a receiver circuit to an incoming data signal"

Within seven (7) days of the date of this order, the parties shall jointly submit: (1) a proposed public version of this order with any proposed redactions bracketed in red; and (2) a written justification for any proposed redactions specifically explaining why the piece of information sought to be redacted is confidential and why disclosure of the information would be

likely to cause substantial harm or likely to have the effect of impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions.[4]

SO ORDERED.

Thomas B. Pender
Administrative Law Judge

[4] Under Commission Rules 210.5 and 201.6(a), confidential business information includes:

> information which concerns or relates to the trade secrets, processes, operations, style of works, or apparatus, or to the production, sales, shipments, purchases, transfers, identification of customers, inventories, or amount or source of any income, profits, losses, or expenditures of any person, firm, partnership, corporation, or other organization, or other information of commercial value, the disclosure of which is likely to have the effect of either impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions, or causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained, unless the Commission is required by law to disclose such information.

See 19 C.F.R. § 201.6(a). Thus, to constitute confidential business information the disclosure of the information sought to be designated confidential must *likely have the effect of* either: (1) impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions; or (2) *causing substantial harm* to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained.

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **Order No. 17** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on SEP 05 2018.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT NETLIST, INC.	
James M. Wodarski, Esq. **MINTZ LEVIN COHN FERRIS** One Financial Center Boston, MA 02111	( ) Via Hand Delivery (X) Express Delivery ( ) Via First Class Mail ( ) Other: _____
FOR RESPONDENTS SK HYNIX, INC., SK HYNIX AMERICA, INC. & SK HYNIX MEMORY SOLUTIONS, INC.	
Michael R. Franzinger, Esq. **SIDLEY AUSTIN LLP** 1501 K Street N.W. Washington, D.C. 20005	( ) Via Hand Delivery (X) Express Delivery ( ) Via First Class Mail ( ) Other: _____

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	Investigation No. 337-TA-1089

NOTICE OF COMMISSION DETERMINATION TO REVIEW AND VACATE AN INITIAL DETERMINATION, AND TO REMAND THE INVESTIGATION TO THE ADMINISTRATIVE LAW JUDGE

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review and vacate an initial determination ("ID") contained in Order No. 13, issued by the presiding administrative law judge ("ALJ") on April 12, 2018.

FOR FURTHER INFORMATION CONTACT: Robert Needham, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 708-5468. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, SW., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. ("Netlist") of Irvine, California. 82 FR 57290-91. The complaint, as supplemented, alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain memory modules and components thereof that infringe certain claims of U.S. Patent Nos. 9,606,907 ("the '907 patent") and 9,535,623 ("the '623 patent"). *Id.* The Commission's notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (together, "SK hynix"). *Id.* at

57291. The Office of Unfair Import Investigations ("OUII") is also participating in this investigation. *Id.*

On February 20, 2018, SK hynix moved for a summary determination of noninfringement of every asserted claim in this investigation based on claim preclusion and issue preclusion in view of the Commission's final determination in *Certain Memory Modules and Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-1023 ("the 1023 Investigation"). The 1023 Investigation determined that SK hynix did not infringe certain claims of the parent patents of the '907 and '623 patents, and SK hynix argued that claim preclusion and issue preclusion compelled a finding that SK hynix did not infringe the asserted claims of the '907 and '623 patents in this investigation.

On March 5, 2018, Netlist opposed the motion. That same day, OUII filed a response supporting a finding of noninfringement by reason of issue preclusion, but opposing a finding of noninfringement by reason of claim preclusion. On March 14, 2018, OUII filed a supplemental brief, and Netlist and SK hynix filed replies to the supplemental brief. On March 22, 2018, Netlist moved for leave to file a sur-reply to SK hynix's reply.

On April 12, 2018, the ALJ issued the subject ID, granting a summary determination that SK hynix does not infringe any asserted claim by reason of issue preclusion. The ID does not construe any claim limitation, but concludes that the scope of relevant limitations of the asserted claims of the '907 and '623 patents are identical to the scope of corresponding relevant limitations of parent patents asserted in the 1023 Investigation. The ALJ also denied, as an order, the motion with respect to claim preclusion.

On April 23, 2018, Netlist petitioned for review of the ALJ's findings on issue preclusion, and SK hynix filed a contingent petition for review of the ALJ's findings on claim preclusion. On April 30, 2018, Netlist and SK hynix opposed each other's petitions. That same day, OUII filed a response in opposition to both petitions.

Having examined the record of this investigation, including the ID, the petitions for review, and the responses thereto, the Commission has determined to review and vacate the ID. The Commission finds that the ALJ erred by finding that SK hynix did not infringe the asserted claims of the '907 and '623 patents without first resolving the parties' relevant claim construction disputes. The Commission therefore remands the investigation to the ALJ for further proceedings.

The Commission rejects SK hynix's contingent petition as procedurally improper. The denial of a motion for summary determination is made in an order, 19 CFR 210.42(c), which is not immediately reviewable by the Commission, 19 CFR 210.43(a)(1).

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. 1337), and in part 210 of the Commission's Rules of Practice and Procedure (19 CFR part 210).

By order of the Commission.

Lisa R. Barton
Secretary to the Commission

Issued: May 29, 2018

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **Inv. No. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on 5/29/2018

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Complainants Netlist, Inc.:

James M. Wodarski
MINTZ LEVIN COHN FERRIS GLOVSKY AND POPEO PC
One Financial Center
Boston, MA 02111

☐ Via Hand Delivery
☒ Via Express Delivery
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On Behalf of Respondents SK Hynix Inc., SK Hynix America Inc., and SK Hynix memory solutions Inc.:

Michael R. Franzinger
SIDLEY AUSTIN LLP
1501 K Street, N.W.
Washington, DC 20005

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☒ Via Express Delivery
☐ Via First Class Mail
☐ Other:_____

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of CERTAIN MEMORY MODULES AND COMPONENTS THEREOF	Investigation No. 337-TA-1089

REMAND ORDER

The Commission instituted this investigation on December 4, 2017, based on a complaint filed by Netlist, Inc. ("Netlist") of Irvine, California. 82 Fed. Reg. 57290-91. The complaint, as supplemented, alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain memory modules and components thereof that infringe certain claims of U.S. Patent Nos. 9,606,907 ("the '907 patent") and 9,535,623 ("the '623 patent"). *Id.* The Commission's notice of investigation named as respondents SK hynix Inc. of the Republic of Korea; SK hynix America Inc. of San Jose, California; and SK hynix memory solutions Inc. of San Jose, California (together, "SK hynix"). *Id.* at 57291. The Office of Unfair Import Investigations ("OUII") is also participating in this investigation. *Id.*

On February 20, 2018, SK hynix moved for a summary determination that it did not infringe any asserted claim in this investigation based on claim preclusion and issue preclusion resulting from the Commission's final determination in *Certain Memory Modules and Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-1023 ("the 1023 Investigation"). The '907 and '623 patents asserted in this investigation claim priority to patents with claims that SK hynix was found not to infringe in the 1023

Investigation. SK hynix thus argued that the Commission's findings in the 1023 Investigation create claim preclusion and issue preclusion that compels a finding that SK hynix does not infringe the asserted claims of the '907 and '623 patents.

On March 5, 2018, Netlist opposed the motion. That same day, OUII filed a response supporting a finding of noninfringement by reason of issue preclusion, but opposing a finding of noninfringement by reason of claim preclusion. On March 14, 2018, OUII filed a supplemental brief, and Netlist and SK hynix filed replies to the supplemental brief. On March 22, 2018, Netlist moved for leave to file a sur-reply to SK hynix's reply.

On April 12, 2018, the ALJ issued an initial determination granting a summary determination that SK hynix does not infringe any asserted claim by reason of issue preclusion. The ALJ did not construe any claim limitation, but concluded that the claims asserted here were sufficiently similar to the claims in the 1023 Investigation such that issue preclusion applied. The ALJ also denied the motion with respect to claim preclusion in an order.

On April 23, 2018, Netlist petitioned for review of the ALJ's findings on issue preclusion, and SK hynix filed a contingent petition for review of the ALJ's findings on claim preclusion. On April 30, 2018, Netlist and SK hynix opposed each other's petitions. That same day, OUII filed a response in opposition to both petitions.

A tribunal must conduct relevant claim construction in order to issue a summary determination of noninfringement. *See Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1288 (Fed. Cir. 2009) ("Evaluation of a summary judgment of noninfringement requires two steps: claim construction . . . and a comparison of the properly construed claims to the

accused product"). That claim construction must resolve the parties' disputes over the scope of the claim terms. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.").

Here, the ID found that SK hynix did not infringe the "output or receive / do not output or receive" limitations of the '907 patent, and the "a notification signal [. . .] indicating a [or at least one] status of one or more training sequences" of the '623 patent. The parties' claim construction briefing, however, shows that the parties have disputes over the proper construction of those limitations. The ALJ was therefore required to construe claim terms to resolve those disputes prior to ruling on the infringement or noninfringement of those limitations and whether issue preclusion applies. Because the ALJ did not do so, the Commission reviews and vacates the ID's summary determination that SK hynix does not infringe the asserted claims, and remands the investigation to the ALJ for further proceedings, including resolving the parties' claim construction disputes.

Accordingly, upon consideration of this matter, the Commission hereby ORDERS that the investigation be remanded to the ALJ to (1) consider the parties' claim construction arguments and make appropriate findings resolving their claim construction disputes, and (2) continue the investigation. Notice of this Order shall be served on the parties to this investigation.

By order of the Commission.

Lisa R. Barton
Secretary to the Commission

Issued: May 29, 2018

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF **Inv. No. 337-TA-1089**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **ORDER** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on 5/29/2018

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Complainants Netlist, Inc.:

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On Behalf of Respondents SK Hynix Inc., SK Hynix America Inc., and SK Hynix memory solutions Inc.:

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☐ Via First Class Mail
☐ Other:_____

Public Version

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN MEMORY MODULES AND COMPONENTS THEREOF**	**Inv. No. 337-TA-1089**

ORDER NO. 13: INITIAL DETERMINATION GRANTING RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NON-INFRINGEMENT

(April 12, 2018)

TABLE OF ABBREVIATIONS	
1023 Investigation	*Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023
1023 ID	Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond (Nov. 14, 2017)
'185 patent	U.S. Patent No. 8,516,185
'907 patent	U.S. Patent No. 9,606,907
'837 patent	U.S. Patent No. 8,489,837
'623 patent	U.S. Patent No. 9,535,623
Resp1	MEMORANDUM IN SUPPORT OF RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NON-INFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION of February 20, 2018
Resp2	REPLY IN SUPPORT OF RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NON-INFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION of March 14, 2018
Resp3	RESPONDENTS' OPPOSITION TO COMPLAINANT'S MOTION FOR LEAVE TO FILE A SUR-REPLY TO RESPONDENTS' REPLY BRIEF AND COMMISSION INVESTIGATIVE STAFF'S SUPPLEMENTAL RESPONSE BRIEF of March 22, 2018
Netlist1	COMPLAINANT'S MEMORANDUM OF POINTS AND AUTHORITIES IN RESPONSE TO RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NON-INFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION (MOTION NO. 1089-006) of March 5, 2018
Netlist2	COMPLAINANT'S REPLY BRIEF TO COMMISSION INVESTIGATIVE STAFF'S RESPONSE TO RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NON-INFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION (MOTION NO. 1089-006) of March 14, 2018
Netlist3	COMPLAINANT'S [PROPOSED] SUR-REPLY TO RESPONDENTS' REPLY BRIEF AND COMMISSION INVESTIGATIVE STAFF'S SUPPLEMENTAL RESPONSE BRIEF (MOTION NO. 1089-006) of March 22, 2018

Staff1	COMMISSION INVESTIGATIVE STAFF'S RESPONSE TO RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NONINFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION (Mot. Dkt. No. 1089—006) of March 2, 2018
Staff2	COMMISSION INVESTIGATIVE STAFF'S MOTION FOR LEAVE TO SUPPLEMENT ITS RESPONSE TO RESPONDENTS' MOTION FOR SUMMARY DETERMINATION OF NONINFRINGEMENT OF U.S. PATENT NOS. 9,535,623 AND 9,606,907 ON THE BASIS OF CLAIM PRECLUSION AND ISSUE PRECLUSION (Mot. Dkt. No. 1089—006) of March 14, 2018

I. INTRODUCTION

On February 20, 2018, respondents SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc. ("Respondents" or "SK hynix") filed a motion "for summary determination that its standard-compliant DDR4 RDIMM and LRDIMM memory modules[1] do not infringe" the asserted patents in this investigation. (Motion Docket No. 1089-006.) Respondents' motion included a statement of undisputed facts ("Respondents' SUF") and generally argues that claim preclusion and issue preclusion principles based on a prior investigation between the same parties, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (hereafter the "1023 Investigation") require this finding of non-infringement. (Resp1 at 1.)[2] Respondents propose the motion, if granted, would terminate the investigation in its entirety. (Mot. at i.) Respondents' memorandum in support of this motion is referred to herein as "Resp1."

On March 5, 2018, the Commission Investigative Staff ("Staff") responded to Respondents' motion and supported the motion with respect to issue preclusion, but not claim preclusion. (*See* Staff1 at 1-2.) This response from the Staff is referred to herein as "Staff1."

Also on March 5, 2018, complainant Netlist, Inc. ("Netlist") responded and opposed Respondents'' motion. This opening submission from Netlist is referred to herein as "Netlist1." Generally, Netlist argues the present investigation involves different issues preventing either form of preclusion, and further, that a decision on issue preclusion would be premature given that claim construction has yet to occur. (*See* Netlist1 at 1.) Netlist included a response to

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[1] RDIMM means "registered dual in-line memory modules" and LRDIMM means "load-reduced dual in-line memory modules." (1023 ID at 4.)

[2] The Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond (Nov. 14, 2017) from the 1023 Investigation is referred to herein as the "1023 ID."

Respondents' SUF ("Responsive SUF") and its own "Additional Statement of Material Facts" ("ASMF") with the opposition.

On March 14, 2018, all parties to the investigation filed unopposed motions for leave to file additional responses. (Motion Docket Nos. 1089-009, -011, -012.) Each motion argued good cause supported the requested leave, at least in part, to discuss a Federal Circuit decision regarding claim preclusion which had issued two days earlier, *SimpleAir, Inc. v. Google LLC,* 2016-2738, March 12, 2018 (Fed. Cir. 2018). Each of these motions for leave (Mot. Dkt. Nos. 1089-009, -011, -012) is GRANTED and the attached responses have been considered. These second round responses are referred to herein as "Resp2," "Netlist2," and "Staff2."

On March 22, 2018, Netlist filed a third response with attached motion for leave (Mot. Dkt. No. 1089-013), which Respondents opposed on the same day. While I generally agree with the argument contained within Respondents' opposition, Netlist's requested leave (Mot. Dkt. 1089-013) is GRANTED in light of the case dispositive nature of the original motion. This third response from Netlist is referred to herein as "Netlist3," and the corresponding opposition from Respondents as "Resp3."

For the reasons articulated below, Respondents' motion for summary determination of non-infringement (Mot. Dkt. No. 1089-006) is GRANTED on the basis of issue preclusion. Given the similarity between the claim terms at issue in this investigation and those which were dispositive of infringement in the 1023 Investigation, and that the accused products and parties are exactly identical, the same non-infringement determination is required. Hence, there is nothing left for me to decide.

II. STANDARDS OF LAW

Commission Rule 210.18 provides that "[a]ny party may move … for a summary determination in its favor upon all or any part of the issues to be determined in the investigation."

19 C.F.R. § 210.18(a). Summary determination "shall be rendered if pleadings and any depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to summary determination as a matter of law." 19 C.F.R. § 210.18(b).

In evaluating a motion for summary determination I must evaluate the evidence "in the light most favorable to the party opposing the motion." *See, e.g.*, *Certain Personal Computers and Digital Display Devices*, Inv. No. 337-TA-606, Order No. 20 at 2 (Jan. 11, 2008). Nevertheless, the non-moving party "has the burden to submit more than averments in pleadings or allegations in legal memoranda. Mere denials or conclusory statements are insufficient." *Certain Magnetic Response Injection Systems and Components Thereof*, Inv. No. 337-TA-434, Order No. 16 at 5 (Sept. 26, 2000) (citations omitted). This means the "[the non-moving party] must do more than simply show there is some metaphysical doubt as to the material facts" to avoid summary determination. *Certain Electronic Devices, Including Mobile Phones, Portable Music Players, and Computers*, Inv. No. 337-TA-701, Order No. 58 at 4, 10, 15 (quoting *Matsushita Elec. Indus. v. Zenith Radio Corp.*, 475 U.S. 574, 586 (1986)); *accord Certain Electronic Devices with Image Processing Systems, Components Thereof, and Associated Software*, Inv. No. 337-TA-724, Order No. 29 at 3, 16-17 (Mar. 11, 2011) (non-reviewed).

To obtain relief in a Section 337 investigation, a complainant, in a patent-based case, must prove "[t]he importation into the United States, the sale for importation, or the sale within the United States after importation by the owner, importer, or consignee, of articles that infringe a valid and enforceable United States patent . . . or are made, produced, processed, or mined under, or by means of, a process covered by the claims of a valid and enforceable United States patent." 19 U.S.C. § 1337(a)(1)(B).

Literal infringement is a question of fact. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). Literal infringement requires the patentee to prove that the accused device contains each and every limitation of the asserted claim(s). *Frank's Casing Crew & Rental Tools, Inc. v. Weatherford Int'l, Inc.*, 389 F.3d 1370, 1378 (Fed. Cir. 2004). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

"Under the doctrine of claim preclusion, 'a judgment 'on the merits' in a prior suit involving the same parties or their privies bars a second suit based on the same cause of action.'" *SimpleAir, Inc. v. Google LLC*, 884 F.3d 1160, 1165 (Fed. Cir. 2018) (citing *Lawlor v. Nat'l Screen Serv. Corp.*, 349 U.S. 322, 326 (1955)). A "cause of action is defined by the transactional facts from which it arises, and the extent of the factual overlap." *Senju Pharm. Co. v. Apotex, Inc.*, 746 F.3d 1344, 1349 (Fed. Cir. 2014) (citing *Acumed LLC v. Stryker Corp.*, 525 F.3d 1319, 1323-1324 (Fed. Cir. 2008)). For purposes of claim preclusion, the scope of a prior cause of action is determined "pragmatically, giving weight to such considerations as whether the facts are related in time, space, origin, or motivation, whether they form a convenient trial unit, and whether their treatment as a unit conforms to the parties' expectations or business understanding or usage." *Acumed*, 525 F.3d at 1324 (internal citation omitted).

In the patent infringement context, "[c]laim preclusion will generally apply when a patentee seeks to assert the same patent against the same party and the same subject matter." *Senju Pharm. Co.*, 746 F.3d at 1349 (citing *Kearns v. Gen. Motors Corp.*, 94 F.3d 1553, 1557 (Fed. Cir. 1996)); *see Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1341 (Fed. Cir. 2012) (holding two claims which were "not materially different" do not create a new cause of action). "While 'ordinarily' different patents will raise different causes of action . . . that factor is not dispositive and does not substitute for the transactional approach consistently followed by

the [Federal Circuit]." *SimpleAir*, 884 F.3d at 1166 (internal citations omitted). "Where different patents are asserted in a first and second suit, a judgment in the first suit will trigger claim preclusion only if the scope of the asserted patent claims in the two suits is essentially the same." *Id.* at 1167. "[T]he claim preclusion analysis requires comparing the patents' claims along with other relevant transactional facts," even though a terminal disclaimer "is a strong clue" that the subsequent patent lacks a patentable distinction over the former. *Id.* at 1168.

Issue preclusion is also known as "collateral estoppel" and "like the related doctrine of *res judicata*, serves to 'relieve parties of the cost and vexation of multiple lawsuits, conserve judicial resources, and, by preventing inconsistent decisions, encourage reliance on adjudication.'" *United States v. Mendoza*, 464 U.S. 154, 158 (1984) (citing *Allen v. McCurry*, 449 U.S. 90, 94 (1980)). "Under the doctrine of issue preclusion, also called collateral estoppel, a judgment on the merits in a first suit precludes relitigation in a second suit of issues actually litigated and determined in the first suit." *In re Freeman*, 30 F.3d 1459, 1465 (Fed. Cir. 1994). The Federal Circuit has explained:

> Indeed, for us not to adopt the same claim construction in a case such as this, in which the construction of the claim term in question was a necessary predicate to the determination of a prior litigation before this court and is evident from the face of the intrinsic record without resort to expert testimony, would run counter to the Supreme Court's guidance on stare decisis in *Markman*: "treating interpretive issues as purely legal will promote (though it will not guarantee) intrajurisdictional certainty through the application of stare decisis." *Markman*, 517 U.S. at 391, 116 S.Ct. 1384.

Miken Composites, L.L.C. v. Wilson Sporting Goods Co., 515 F.3d 1331, 1338, n.* (Fed. Cir. 2008). Accordingly, "where a determination of the scope of patent claims was made in a prior case, and the determination was essential to the judgment there on the issue of infringement, there is collateral estoppel in a later case on the scope of such claims, *i.e.*, the determined scope

cannot be changed. *Molinaro v. Fannon/Courier Corp.*, 745 F.2d 651, 655 (Fed. Cir. 1984). Issue preclusion differs from claim preclusion in that "claim preclusion forecloses successive litigation of the same cause of action whether or not relitigation of the cause of action involves the same issues as the earlier suit." *SimpleAir*, 884 F.3d at 1165 (citing *New Hampshire v. Maine*, 532 U.S. 742, 748-9 (2001)).

With that said, "[t]ribunals have discretion to decide whether a particular case is appropriate for application of issue preclusion." *Certain 3G Mobile Handsets and Components Thereof*, Inv. No. 337-TA-613 (remand), Comm'n Op. at 26 (Sep. 21, 2015) ("*3G Mobile Handsets*") (citing *A.B. Dick Co. v. Burroughs Corp.*, 713 F.2d 700, 7012 (Fed. Cir. 1983); *Certain Semiconductor Integrated Circuits Using Tungsten Metallization and Products Containing Same*, Inv. No. 337-TA-648, Comm'n Op. at 3 (Feb. 18, 2009) ("*Semiconductor Integrated Circuits*"). The Commission has identified a four factor test for the application of issue preclusion:

> Under Federal Circuit law, the doctrine of issue preclusion can be applied only if: (1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) the plaintiff had a full and fair opportunity to litigate the issue in the first action.

Semiconductor Integrated Circuits, Inv. No. 337-TA-648, Comm'n Op. at 2-3 (citing In re Freeman, 30 F.3d at 1465).

"[T]o apply issue preclusion to a claim interpretation issue decided in a prior infringement adjudication, 'the interpretation of the claim had to be the reason for the loss [in the prior case] on the issue of infringement.'" *In re Freeman*, 30 F.3d 1459, 1466 (Fed. Cir. 1994) (quoting *Jackson Jordan, Inc. v. Plasser American Corp.*, 747 F.2d 1567, 1577 (Fed. Cir. 1984)). "Only a final judgment holds sway in an analysis of whether issue preclusion applies, even if the

final judgment is reached first in a later filed case." *3G Mobile Handsets*, Inv. No. 337-TA-613 (remand), Comm'n Op. at 29 (citing *Chicago, R.I. & P. Ry. V. Schendel*, 270 U.S. 611, 615-17 (1926)). With respect to identify of issues, the Federal Circuit has held "[c]omplete identity of [patent] claims is not required to satisfy the identity-of-issues requirement for claim preclusion." *Soverain Software LLC v. Victoria's Secret Direct Brand Mgmt., LLC*, 778 F.3d 1311, 1319 (Fed. Cir. 2015) (citing *Ohio Willow Wood Co. v. Alps S., LLC*, 735 F.3d 1333, 1342 (Fed. Circ. 2013)). Rather, "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342.

III. DISCUSSION

a. Claim Preclusion

i. Respondents' Contentions

In their opening memorandum, Respondents explain that:

> In a prior investigation initiated by Netlist, Inc., ("Netlist"), Inv. No. 337-TA-1023 (the "1023 Investigation"), the Commission held that the accused products of SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc. (collectively, "SK hynix") do not infringe two Netlist patents, U.S. Patent No. 8,489,837 (the "'837 patent") (Ex. 2) and U.S. Patent No. 8,516,185 (the "'185 patent") (Ex. 3). Now, in this investigation, Netlist asserts two children of the '837 and '185 patents—U.S. Patent No. 9,535,623 (the "'623 patent") (Ex. 4) and U.S. Patent No. 9,606,907 (the "'907 patent") (Ex. 5)—against the same products that were accused in the 1023 Investigation, and based on the same theory of standard-compliance infringement.

(Respl at 1.) Respondents contend that Netlist "concedes that 'certain issues in this 1089 investigation may be substantially similar to those addressed in the 1023 investigation.'" (*Id.* at 2 (citing Netlist Case Management Statement (Jan. 23, 2018)).) Thus, in Respondents view, "[c]laim preclusion bars this second investigation initiated by Netlist, involving the same parties,

because the accused products are the same and asserted patents are not materially different." (*Id.* (citing *Senju Pharm.*, 746 F.3d at 1348–49).) Thus, according to Respondents, I should terminate this investigation "because Netlist is seeking to relitigate the same cause of action that the Commission rejected in the 1023 Investigation." (*Id.* at 8.)

Respondents argue the first two elements of claim preclusion are indisputably met, "[t]he Commission has affirmed the ID in the 1023 Investigation and the parties to the 1023 Investigation and this investigation are the same." (*Id.* at 8-9; *see id.* at 10 (referencing RDIMM and LRDIMM memory modules).) Respondents claim "[t]he sole remaining element—whether the two investigations involve the 'same cause of action'—also is satisfied here." (*Id.* at 9.) Respondents argue "[t]his investigation also involves 'the same patent rights' as those previously asserted in the 1023 Investigation." (*Id.* at 10 (referring to *Senju Pharm. Co.*, 746 F.3d at 1350).) Respondents then discuss the holdings in the district court decision *Simple Air, Inc. v. Google Inc.*, 204 F. Supp. 3d 908 (E.D. Tex. 2016) and *XY, LLC, et al. v. Trans Ova Genetics, LC*, No. 17-cv-0944-WJM-NYW, 2018 WL 367416, at *10 (D. Colo. Jan. 11, 2018) as examples of courts barring patentees from asserting child patents against defendants who successfully defended claims of infringement under the parent patents. (*See id.* at 10-12.)

Respondents argue "[j]ust as in *Simple Air* and *XY, LLC*, Netlist has asserted child patents against the same defendant and same accused devices. . . . These patents share a specification with the earlier-asserted patents and are subject to terminal disclaimers." (*Id.* at 12 (citing 1023 ID at 4-5; Netlist Complaint at 1; '623 patent; '837 patent; '185 patent; '907 patent; Mot., Ex. 10 at 173, 310; Mot. Ex. 13 at 80-85).) Respondents then argue how the "relevant claims are substantially the same" and compare the: (1) "notification signal indicating . . . status" limitations found in the '837 patent and '623 patent; and (2) a "fork in the road" concept allegedly found in both the '185 and '907 patents. (*Id.* at 12-13 (internal citations omitted).)

Respondents then reason "[f]or both parent-child pairs, therefore, the child patent's claims are not 'materially different' from the parent's claims." (*Id.* at 13 (citing *Aspex Eyewear, Inc.*, 672 F.3d at 1341).)

Overall, according to Respondents, "when the shared applications and specifications, the terminal disclaimers, and the substantially similar claims are considered together, there can be no dispute that the two patents asserted here constitute the same invention disclosed by their parents," and "[t]hese rights cannot be reasserted against SK hynix here." (*Id.* at 13-14 (citing *Antares Pharma, Inc. v. Medac Pharma Inc.*, 771 F.3d 1354, 1358 (Fed. Cir. 2014)).) To do otherwise, Respondents assert, "would permit Netlist to 'bring multiple successive time-consuming, resource-draining attacks' against SK hynix—just the sort of abuse that claim preclusion is designed to prevent." (*Id.* at 14 (citing *XY, LLC*, 2018 WL 367416, at *6).)

Respondents add that, based on Notice of Allowance dates, Netlist could have asserted the '623 and '907 patents in the 1023 Investigation, but declined to do so. (*See id.* at 14-15.) Respondents feel that their inclusion would have made a "convenient trial unit" given their similarity to the parent patent (*id.* at 15 (citing *Acumed*, 525 F.3d at 1324)) and that Netlist's withholding them indicates a decision to "stockpile" to support a second lawsuit (*id.*). Finally, Respondents urge that the *Kessler* doctrine, which "reinforces the preclusion principles by ensuring that once a product has been found not to infringe, that product cannot be subject to 'repeated harassment' by the patentee," also bars Netlist's claims. (*Id.* at 16 (citing *Brain Life, LLC*, 746 F.3d at 1055–57; *SpeedTrack, Inc. v. Office Depot, Inc.*, 791 F.3d 1317, 1325 (Fed. Cir. 2015)).)

In Respondents' second submission, they discuss the Federal Circuit's recent opinion in *SimpleAir, Inc. v. Google LLC*, 2018 WL 1247003, 884 F.3d 1160 (Fed. Cir. Mar. 12, 2018). (Resp2 at 1-2) Respondents interpret the Federal Circuit's holding as "claim preclusion bars the

assertion of patent claims—regardless of how recently the patent issued—that are 'essentially the same' or 'patentably indistinct from' a previously asserted patent claim." (*Id.* (citing *SimpleAir*, 2018 WL 1247003 at *4-7).) Respondents consider *SimpleAir* as disposing of Netlist's principle argument—that "different patents necessarily confer a different cause of action." (*Id.* at 2 (citing Netlist1 at 23-33).)

Respondents then repeat their assertion that under a "transactional facts" test for claim preclusion, and contrary to Netlist's position, "there are no material differences [within either pair of related patents] that could give rise to different transactional facts and a different cause of action." (*Id.* at 3 (referring to *SimpleAir*, 2018 WL 124700, at *3–4).)

For the '837 and '623 patents, Respondents point out:

> The '623 and '837 patents issued from a common application, have the same specification, and the same inventor. Ex. 2, '837 patent at Face; Ex. 4, '623 patent at Face. Both patents claim priority to the same provisional application. Ex. 2, '837 patent at Face; Ex. 4, '623 patent at Face.
>
> . . . .
>
> Furthermore, Netlist filed a terminal disclaimer when prosecuting the '623 patent, disclaiming any term of the '623 patent beyond the expiration date of the '837 patent.

(*Id.* at 4.) Respondents look to *SimpleAir* to conclude that the existence of such a terminal disclaimer is a "strong clue" that the child "lacked a patentable distinction over the parent." (*Id.* (citing *SimpleAir*, 2018 WL 124700, at *6).) Respondents continue, "all that separates the '623 patent from the '837 patent are a few snippets of claim language" and "the fine differences here, standing alone, do not permit a patentee to escape claim preclusion." (*Id.* at 5.) Respondents acknowledge that "the 'claim preclusion analysis requires comparing the patents' claims *along with other relevant transactional facts*.'" (*Id.* at 5 (citing *SimpleAir*, 2018 WL 124700, at *6).)

Put it another way, Respondents reason "[i]f everything else about the patent is the same, and the scope of the claim is not substantially different, claim preclusion should attach." (*Id.*)

Regarding the claims of each patent, Respondents point to the "same 'notification signal … indicating at least one status' limitation." (*Id.* at 5-6).) With respect to any alleged difference behind the term "training" ('623 patent) as compared to "initialization" ('837 patent), Respondents defer to their discussion of issue preclusion. (*See id.* at 6.)

For the '185 and '907 patents, Respondents point out:

> The '907 and '185 patents issued from a common application, have the same specification, and the same inventors. Ex. 3, '185 patent at Face; Ex. 5, '907 patent at Face. Both patents claim priority to the same original application. Ex. 3, '185 patent at Face; Ex. 5, '907 patent at Face. As with the '623 patent, the '907 patent also is subject to a terminal disclaimer based on its parent.

(*Id.* at 6.) Regarding the claims of each patent, Respondents explain that "[a]lthough the '907 patent contains claim language that varies from the '185 patent, the '907 patent's claims still delineate the same basic 'fork in the road' requirement." (*Id.*) Respondents suggest that, for claim preclusion, "the question is whether the asserted claim arises from a 'common nucleus of operative facts'" (*id.* at 7 (citing *Gillig v. Nike, Inc.*, 602 F.3d 1354, 1361 (Fed. Cir. 2010))) and "Netlist has not shown how the '907 patent's different claim language amounts to an entirely different set of operative facts sufficient to justify a second round of litigation" (*id.*).

Finally, Respondents revisit the notion that Netlist "*could have asserted*, or could have tried to assert, the '623 and '907 patents in the 1023 Investigation is another reason to apply claim preclusion in this Investigation." (*Id.* at 7.) Respondents point to Netlist's attempt to add a patent in this investigation in an effort to undermine Netlist's response that "under the heightened standards for amendments in the ITC [it] would not have been permitted" to add the '623 and '907 patents to the 1023 Investigation. (*Id.* (referring to Netlist1 at 27).)

Respondents also revisit the applicability of the *Kessler* doctrine as a bar to Netlist's claims, "[t]o the extent the ALJ determines that neither claim preclusion nor issue preclusion bars Netlist's instigation of this repetitious investigation." (*Id.*)

ii. Netlist's Contentions

In its initial opposition to Respondents' motion, Netlist contends:

> Indeed, these patents did not issue until well after the 1023 Investigation instituted. Moreover, these patents recite different claim language than the patents litigated in the 1023 Investigation, and the material differences in claim scope present new issues for adjudication that were neither decided nor essential to the judgment in the 1023 Investigation.

(Netlist1 at 1.) Netlist continues "[b]eyond its lack of legal support, the Motion is an intentionally premature and hasty attempt to secure a non-infringement determination based on a series of mischaracterizations and an insufficient and incomplete administrative record." (*Id.* at 1-2.)

With respect to claim preclusion, Netlist initially takes the position that "claim preclusion cannot apply based on controlling Federal Circuit precedent. The Federal Circuit has squarely held that patents issued after the filing date of initial suit—like the '907 and '623 patents here—need not be added to that suit." (*Id.* at 2; *see also id.* at 5 (citing *Gillig v. Nike, Inc.*, 602 F.3d 1354, 1363 (Fed. Cir. 2010)).) Moreover, according to Netlist, "the Motion seeks to circumvent bedrock Federal Circuit law and the procedural schedule by skipping the first step of the two-step infringement inquiry—claim construction" because "a proper construction of the new claims—which Respondents want to avoid—will demonstrate that claims of the '623 and '907 patents have a different meaning and scope than the patents litigated in the 1023 Investigation." (*Id.*)

More specifically, Netlist claims "[f]or at least three reasons, Respondents' primary argument for disposing of this case, claim preclusion, is wrong on the law and the facts." (*Id.* at 23.) Netlist's first reason is that "under established precedent, after-acquired causes of action cannot be claim precluded." (*Id.* (citing *Lawlor*, 349 U.S. at 328; *Gillig*, 602 F.3d at 1363).) Netlist explains "claim preclusion does not apply to the '623 and '907 patents because no rights in those patents existed until well after the 1023 Investigation was instituted." Regarding actual dates, Netlist observes the '623 patent issued on January 3, 2017 which was just before contentions were due in the 1023 Investigation; whereas the '907 patent issued on March 28, 2017 which was just before the close of expert discovery. (*Id.* at 24.) Netlist argues, emphatically, "under controlling and unequivocal precedent, claim preclusion cannot apply to the '623 and '907 patents. Therefore, Netlist had no obligation to seek leave to amend its Complaint in the 1023 Investigation to add the '623 and '907 patents." (*Id.* at 25.) Netlist contends "*res judicata* does not punish a plaintiff for exercising the option not to supplement the pleadings with an after-acquired claim." (*Id.* (citing *Gillig*, 602 F.3d at 1363; *Florida Power & Light Co. v. United States*, 198 F.3d 1358, 1361 (Fed. Cir. 1999)).) Netlist attacks the district court decision in *XY, LLC* as "decid[ing], on policy grounds, that the Federal Circuit must not have meant what it said," as opposed to Respondents' characterization of "flow[ing] directly from the Federal Circuit's precedents." (*Id.* at 26-27 (referring to Resp1 at 11; *XY, LLC*, No. 17-cv-0944-WJM-NYW, 2018 WL 367416, at *14-16).) Regardless, Netlist believes that it would not have been allowed to add the '623 and '907 patents to the 1023 Investigation "under the heightened standard for amendments in the ITC." (*Id.* at 27 (referring to 19 C.F.R. § 210.14(b)).) "In any event," Netlist continues, "Netlist had not obligation" to do this and for this reason alone Respondents' claim preclusion arguments should fail. (*Id.* at 28.)

Netlist's second reason is that "because each patent gives rise to its own cause of action, resolution of a claim involving one patent does not preclude a claim based upon a different patent." (*Id.* at 23 (citing *Kearns*, 94 F.3d at 1556; *PPC Broadband, Inc. v. Corning Gilbert, Inc.*, No. 5:13-cv-538, 2014 U.S. Dist. LEXIS 33979 at *5 (N.D.N.Y. Mar. 17, 2014)).) Netlist explains, very simply, "claim preclusion does not apply because the 1023 Investigation adjudicated different patents." (*Id.*) Netlist dismisses Respondents' assembled case law on this point as each "involved a subsequent case asserting the same patent as a previous case." (*Id.* at 29-30 (referring to *Senju*, 746 F.3d 1344; *Aspex Eyewear*, 672 F.3d 1335; *Acumed*, 525 F.3d 1319; *Brian Life, LLC v. Elekta Inc.*, 746 F.3d 1045, 1053 (Fed. Cir. 2014); *Young Eng'rs, Inc.*, 721 F.2d at 1315; *Kessler v. Eldred*, 206 U.S. 285 (1907)).)

Regarding the *SimpleAir* district court decision, Netlist describes it as "not controlling and is not good law." (*Id.* at 30-31.) Netlist states flatly "[n]o Federal Circuit precedent suggests that one patent can claim-preclude another. Nor has there been any precedent that a continuation patent is precluded after adjudication of the parent." (*Id.* at 31.) Regarding the impact of the terminal disclaimers filed during prosecution of the '623 and '907 patents, Netlist claims "[t]erminal disclaimers relate to validity, not infringement. Specifically, they relate to obviousness during patent prosecution, and are not an admission regarding any similarity of claim terms" and "have no bearing on claim construction." (*Id.* at 32-33 (citing *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1382-83 (Fed. Cir. 2003)).) Netlist continues to claim that the prosecution history of the '907 patent, in particular, involved the removal of claim limitations which "necessarily broadens claim scope for the purposes of infringement" and the disclaimer of the parent '185 patent "is not evidence of the scope of claim terms that appear in its progeny." (*Id.* at 33 (citing *ResQNet.com, Inc.*, 346 F.3d at 1382-83).)

Netlist's third reason is "the 1023 Investigation was based upon a different set of transactional facts because 'each patent creates a unique set of 'transactional facts' for purposes of claim preclusion.'" (*Id.* at 24 (citing *Trading Techs. Int'l, Inc. v. BCG Partners, Inc.*, No. 10-cv-715, 2011 U.S. Dist. LEXIS 81640, at *22 (N.D. Ill. July 26, 2011)).) Netlist contends "[i]n alleging that the claims are substantially the same, Respondents do not compare the claims, but instead focus only on single claim element from each patent." (*Id.*) Netlist continues "remarkably, the claim elements they do choose to discuss are materially different from those in the 1023 Investigation" and identifies "training sequence" and "initialization sequence" for the '623 patent; "selectively allowing" and "allowing" for the '907 patent. (*See id.* at 34-35.) In Netlist's view "[t]hese differences create different transactional facts, and as such, claim preclusion cannot apply."

In its second submission, Netlist writes "Staff appears to contend that judicial estoppel prevents Netlist from asserting infringement of the '907 and '623 patents in the 1089 Investigation. Netlist respectfully disagrees that such estoppel can apply." (Netlist2 at 12.) For the '907 patent, Netlist reasons that "[j]udicial estoppel is only applicable if the argument made in a previous proceeding was successful, and Netlist did not successfully argue that the '185 patent claims covered a 'straight line' configuration in the 1023 Investigation." (*Id.* at 13 (citing *New Hampshire v. Maine*, 532 U.S. at 750-1).) For the '623 patent, Netlist believes Staff misinterprets the cited passage of the 1023 ID which would have invoked judicial estoppel. (*See id.*)

In its third response, Netlist addresses the Federal Circuit's opinion in *SimpleAir*, which "vacated a district court order dismissing a complaint as barred by claim preclusion and the *Kessler* doctrine, and remanded for further proceedings." (Netlist 3 at 1 (citing *SimpleAir, Inc. v. Google LLC*, No. 2016-2738, 2018 U.S. App. LEXIS 6104, *22 (Fed. Cir. Mar. 12, 2018)).)

Netlist views that decision as "admonish[ing] the district court for failing to perform the proper analysis under the circumstances, namely a detailed comparison of the claims between the subject patents." (*Id.* (citing *SimpleAir*, 2018 U.S. App. LEXIS 6104, *22)).) Netlist also views that decision as "distinguish[ing] claim prelusion regarding reexamined patents from those involving continuation patents like those at issue here." (*Id.* at 2.) More specifically, Netlist argues "[t]he court concluded that, unlike cases involving reexamined patents, claim preclusion based upon continuation patents requires the moving party 'to make a detailed comparison of the claims.'" (*Id.* (citing *SimpleAir*, 2018 U.S. App. LEXIS 6104, *10-11).)

With this principle in mind, Netlist criticizes Respondents as failing to make a sufficient comparison of the claims between the patents in the 1023 Investigation and those presently asserted. (*Id.* at 3.) Netlist argues Respondents' claim of "[each set of] patents are the same in all material respects" is "exactly the sort of cursory approach that the Federal Circuit rejected in *SimpleAir*." (*Id.* (referring to Resp2 at 4, 6; *SimpleAir*, 2018 U.S. App. LEXIS 6104. at *4-5).) Netflix provides two tables showing the comparison that Respondents allegedly failed to perform, which are reproduced below:

U.S. Patent No. 8,489,837; Claim 1	**U.S. Patent No. 9,535,623; Claim 1**
1. A memory module comprising: at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode; a controller circuit configured to cause the memory module to enter the initialization mode; and a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence; and wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.	1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising: a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at

U.S. Patent No. 8,489,837; Claim 1	U.S. Patent No. 9,535,623; Claim 1
	least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

(*id.* at 3-4);

U.S. Patent. No. 8,516,185 (Claim 1)	U.S. Patent. No. 9,606,907 (Claim 1)
A memory module comprising: a plurality of memory devices; a controller configured to receive control information from a system memory controller and to produce module control signals; and a plurality of circuits configured to receive the module control signals, each circuit of the plurality of circuits having a first bit width and operatively coupled to at least two corresponding memory devices of the plurality of memory devices, the at least two corresponding memory devices each having a second bit width smaller than the first bit width, each circuit of the plurality of circuits comprising at least one write buffer and at least one read buffer and configured to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals, and to selectively isolate at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals, wherein each circuit of the plurality of circuits is operable, in response to the module control signals, to actively drive write data from the system memory controller to the at least one selected memory device of	A memory module having a width of n bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising: a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals; a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each n-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command; M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data

U.S. Patent. No. 8,516,185 (Claim 1)	U.S. Patent. No. 9,606,907 (Claim 1)
the at least two corresponding memory devices through the at least one write buffer, and to receive and drive read data from the at least one selected memory device of the at least two corresponding memory devices to the system memory controller through the at least one read buffer, wherein the circuits of the plurality of circuits are distributed at corresponding positions separate from one another.	lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each n-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

(*id.* at 4-6).

Netlist uses these tables to show the claims at issue in the 1023 Investigation are not "essentially the same" as those in this investigation. (*Id.* at 3-6.) Netlist disputes that it has any burden to show that the claims are different. (*Id.* at 6 (citing *SimpleAir,* 2018 U.S. App. LEXIS 6104, at *19).) Netlist argues that Respondents have failed to meet their burden with respect to claim preclusion.

iii. Staff's Contentions

In its first response, the Staff takes the position that "Respondents have not shown that the allegations with respect to the Asserted Patents, which issued during the pendency of the 1023 investigation, in their entirety are the same cause of action as the allegations in the 1023 investigation." (Staff1 at 2.) As Netlist did, Staff observes "the majority of cases finding later issued patent claims to be the 'same patent rights' are directed to where claims of the same adjudicated patent are re-issued," and ultimately argues "because claims of the continuation claims are independent patent claims, and because claim preclusion does not necessarily apply to claims arising during the pendency of the first litigation, the Staff submits that it is not clear that claim preclusion should be applied in this investigation." (*Id.* at 37-38.)

Following the *SimpleAir* Federal Circuit decision, the Staff filed a supplement to its earlier response and revisits its initial position on claim preclusion:

> Since filing its response, however, the Federal Circuit has issued *SimpleAir*, which seems to clarify that, for the purposes of determining whether to apply Claim Preclusion, the substantive similarity of the patent claims is more relevant than the timing of the issuance of the continuation patent.

(Staff2 at 2-3.) The Staff notes that "the only disputed factor for applying claim preclusion was whether the allegations in the 1089 investigation satisfy the 'same cause of action' requirement" and argues "the substantive similarity of the patent claims also supports the application of claim preclusion in this investigation." (*Id.* at 3.) The Staff concludes:

> In particular, the Staff compared the claim terms found to be dispositive in the 1023 investigation with claim terms appearing in the claims asserted in the 1089 investigation. The Staff concluded that the claim limitations in the 1089 investigation were materially the same, and accordingly, dispositive for the same reasons as the 1023 investigation.

(*Id.* at 4.)

iv. Analysis

At the outset, I agree with Netlist that Respondents have failed to meet their burden with respect to showing similarity of the claims across the '837 and '623 patents and the '185 and '907 patents. Netlist's tables, reproduced above, are fair representations of the task Respondents needed to undertake in order to show claims are "essentially the same" under *SimpleAir*. 884 F.3d at 1167 ("As the accused activity between two cases must be 'essentially the same' for claim preclusion to apply . . . we adopt that same standard for comparison of the claims between asserted patents as well.").

Just as Netlist observes, "Respondents' initial motion did not provide such a required comparison of the claims" (Netlist3 at 2), opting instead to rest on the existence of common ownership, inventorship, specification, and terminal disclaimers and then a comparison of just a subset of claim terms—specifically, the "notification signal" terms in the '837 and '623 patents, and the terms behind the "fork in the road" concept in the '185 and '907 patents (*see* Resp1 at 12-13; Resp2 at 4-7 (in part, labeling all other claim language in the '623 and '837 patent claims as "fine differences" without explanation)). As shown in the tables above, there is just too much claim language to consider, outside of "notification signal" and the "fork in the road" concepts, before declaring the entire claims are "essentially the same." *SimpleAir*, 884 F.3d at 1167. For this reason alone, Respondents' motion is DENIED with respect to claim preclusion.

b. Issue Preclusion and the '907 Patent

i. Respondents' Contentions

Moving on, Respondents argue issue preclusion is warranted under the '907 patent, and the '623 patent, because "the patents in both investigations involve identical dispositive claim language (in the case of the '623 and '837 patents) or "slightly different language to describe substantially the same invention" (in the case of the '907 and '185 patents)." (Resp1 at 2-3

(citing *Ohio Willow Wood*, 735 F.3d at 1342; *Bourns, Inc. v. United States*, 537 F.2d 486, 493 (Ct. Cl. 1976))).) Respondents conclude "[b]ecause the ALJ found SK hynix's memory modules non-infringing in the 1023 Investigation, those *same* memory modules also must be found non-infringing here." (*Id.* at 3 (emphasis added).)

More specifically, Respondents assert that issue preclusion arises when the issue in dispute was:

> (1) "necessarily decided in the previous proceeding" and is "identical to the one which is sought to be relitigated;"
>
> (2) "the first proceeding ended with a final judgment on the merits;" and
>
> (3) The party against whom issue preclusion is asserted was a "party or in privity with a party" to the earlier proceeding.

(Resp1 at 17 (citing, *inter alia*, *e.Digital Corp. v. Futurewei Techs., Inc.*, 772 F.3d 723, 726 (Fed. Cir. 2014)).) According to Respondents, the only dispute between the parties is the identity of the issues between the 1023 Investigation and this one. (*Id.*) Respondents compare the claims at issue here with those determined by the Federal Circuit to be sufficiently identical in *Ohio Willow Wood* and *Amgen, Inc. v. Genetics Inst., Inc.*, 98 F.3d 1328 (Fed. Cir. 1996), along with several other district court decisions. (*See id.* at 18-19.)

With respect to the '907 patent, Respondents recount the relevant procedural history as:

> In the 1023 Investigation, the ALJ similarly found that SK hynix's memory modules do not infringe the asserted claims of the '185 patent because they do not read on a key limitation in the claims: that the data buffer not transmit data to all memory devices, but instead only to a subset.

(*Id.* at 23 (citing 1023 ID at 122-129).) Respondents continue, "[t]he ALJ agreed with SK hynix that claim 1 of the '185 patent requires a data buffer circuit that is configured in a 'telltale 'fork in the road' layout' whereby the buffer transmits data to one or more memory devices on one data path, while at the same time isolating the other memory devices on another data path." (*Id.*

at 24 (citing 1023 ID at 124-125).) Respondents argue that the '185 patent was amended during prosecution to include the "fork in the road" limitation to avoid prior art (*see id.* at 25-27 (internal citations omitted)) and the absence of a "fork in the road" in the accused devices was fully litigated and necessarily decided in the 1023 Investigation as Respondents only non-infringement defense (*see id.* at 29 (internal citations omitted)).

Turning back to the '907 patent, Respondents note "the '907 patent is a continuation of the application leading to the '185 patent. Both patents belong to the same family and share specifications, inventors, priority dates, and termination dates." (*Id.* at 29-30 (citing '185 patent; '907 patent; Mot., Ex. 10 at 173, 310).) Most importantly, Respondents argue the '907 patent also requires the "fork in the road" layout through the limitations, such as those found in claim 1:

> *the first memory devices* output or *receive each ... data signal* associated with the memory read or *write command while the second memory devices do not* output or *receive any data associated with the memory read or write command*
>
> . . . .
>
> the *each respective buffer circuit including logic* that responds to the second module control signals by *allowing communication of a ... data signal between the respective one or more of the first memory devices and the memory controller*

(*Id.* at 30 (citing '907 patent at cl. 1) (emphasis in original).) Respondents contend "[t]he other independent claims (16, 30, 43, 53, and 58) have similar limitations that effectively require the same thing." (*Id.* at 31.) Respondents reason:

> The 1023 Investigation therefore forecloses Netlist's infringement claim: all of the '907 patent's asserted claims require the "telltale 'fork in the road' layout"—in each claim, the data only goes down one path (*e.g.*, "path A") to one set of memory devices, and not down another path (*e.g.*, "path B") to a different set of memory devices. *See* Ex. 11, '907 patent slides at 9–14. Because the ALJ in the 1023 Investigation already found that SK hynix's modules

> lack this crucial requirement, issue preclusion bars Netlist from relitigating this issue here.

(*Id.*) Moreover, Respondents argue the claim scope supposedly surrendered during the prosecution of the '185 patent (parent to the '907 patent) "cannot simply be reclaimed in a child application or patent." (*Id.* at 32 (citing and then discussing *Hakim v. Cannon Avent Grp., PLC*, 479 F.3d 1313 (Fed. Cir. 2007)).)

In their response to Netlist's opposition, Respondents contend that waiting until after a "full claim-construction briefing and a *Markman* hearing," as Netlist argues, "would waste Commission resources and result in costly and unnecessary discovery and litigation and accomplish nothing because the decisive analysis will be the same." (Resp2 at 9 (referring to Netlist1 at 36-43).) Respondents continue "[t]o the extent the ALJ believes there are claim-construction issues that must be resolved, those issues can be resolved as part of this motion without further delay or further briefing on claim construction." (*Id.*)

Additionally, Respondents assert that Netlist "fails to address the rest of the '907 patent claim language identified in SK hynix's motion that results in the same 'telltale 'fork in the road' layout,' and which was the basis for the non-infringement finding in the 1023 Investigation." (*Id.* at 19 (referencing Resp1 at 23-30).) Respondents also suggest that during the prosecution of the '907 patent, Netlist "linked" the "allowing" claim term to the "fork in the road" description in the shared specification through the following table:

Amendment	Support
the each respective buffer circuit **including logic that responds to the** second module **control signals by allowing communication of a respective *n*-bit section of the each *N*-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the *M* sets of *n* data lines and via the set of *n* module data lines**	As shown in FIGS. 5 and 6, and discussed in paragraphs **[0065]-[0072], the logic 502** generates **control signals Enable Y1, Enable Y2, Enable D, and** Select Y1/Y2 in **response to the module control signals** (e.g., Module Controls D->Y1), to allow data D->Y1 to be communicated between the memory controller and the respective one or more **of the first memory devices. As shown in FIG. 4A or 4B, each buffer** circuit 416 communicates an **8-bit section** of each N-bit wide data signal.

(*Id.* at 21 (citing Mot., Ex. 10 at 430; '907 patent at 17:63–18:2, 18:10–16).) Respondents argue the patent examiner's reasons for allowance also credited a "fork in the road" requirement in the Notice of Allowance. (*See id.* at 22 (citing Mot., Ex. 10 at 440).)

Further, Respondents repeat their position that the scope disclaimer made during the prosecution of the '185 patent "applies with equal force to the claims of the '907 patent." (*Id.* (citing *Hakim*, 479 F.3d at 1315–18).) Respondents suggest that: any attempt by Netlist to dispute disclaimer occurred during the '185 patent prosecution is futile as that was squarely decided in the 1023 Investigation (*id.*); and Netlist's failure to "inform[] the Examiner during prosecution of the '907 patent that he should revisit his prior rejection based on *Rajan* from the prosecution of the '185 patent" means, "under *Hakim*, the prosecution disclaimer from the '185 patent applies to the claims of the '907 patent" (*id.* at 23-24). Respondents also argue a § 112 rejection over a proposed claim that reflected Netlist's "straight-line" embodiment shows "yet another reason why the claims of the '907 patent require a 'fork in the road.'" (*Id.* at 24-25 (citing Mot., Ex. 10 at 391; *UCB, Inc. v. Yeda Research & Dev. Co.*, 837 F.3d 1256, 1261 (Fed. Cir. 2016)).)

Respondents move on to address Netlist's argument regarding "Set of N Module Data Lines" and whether the "first" and "second" memory devices recited in the '907 patent claims correspond to memory devices 412A and 412C. (*See id.* at 25-29 (referencing Netlist1 at 13-15, 49-50).) Respondents argue Netlist's interpretation conflicts with the "do not . . . receive any data" claim limitation and that the proper interpretation, again, is a "fork in the road" where the first and second memory devices are 412A/412C and 412B/412D, respectively. (*See id.* at 26-28 (citing '907 patent at 17:67–18:2, 11:38–49, 15:39–51, 15:65–16:16).) Respondents contend the claim language "a set of" "permits *multiple* elements to be in the set" thereby defeating Netlist's claim that the claim language can only support the "straight-line" interpretation using memory devices 412A and 412C. (*Id.* at 28 (citing '907 patent at Fig. 4A and element 452) (emphasis in original).) Respondents also argue "Netlist's interpretation would exclude the preferred embodiment disclosed in the '907 patent, contrary to Federal Circuit precedent." (*Id.* at 29 (citing *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013)).) Respondents conclude that Netlist's position that the 1023 Investigation was decided in Netlist's favor is "bizarre" given the "no violation" finding. (*Id.* at 29-30.)

ii. Netlist's Contentions

In its opening submission, Netlist views Respondents as:

> [I]gnor[ing] controlling law that different claim terms in different patents are presumed to have different meanings. Respondents instead request that the ALJ summarily determine the opposite—that the claim terms in the '623 and '907 patents have the same meaning as different claim terms in different patents from the 1023 Investigation.

(Netlist1 at 3.) Netlist continues and characterizes Respondents position as:

> [A]rgu[ing] that a buffer circuit that "allows" communication between memory devices and a memory controller (as claimed in the '907 patent) is the same as a buffer circuit that "selectively

> allows" communication (as claimed in U.S. Patent No. 8,410,185 ("the '185 patent") adjudicated in the 1023 Investigation).

(*Id.*) Netlist then claims:

> Contrary to Respondents' arguments, the ID did not find that Netlist disclaimed claim scope such that "allow" and "selectively allow" must mean the same thing. Nor did the ID construe "allow" to require a "fork in the road"—on the contrary, the ID found that Respondents coined the phrase as a shorthand for the "selective" actions claimed in the '185 patent, which are not present in the '907 patent claims.

(*Id.*)

For the both the '907 and '623 patents, Netlist argues that Respondents' motion is ultimately rooted in determining claim scope, and thus premature before the scheduled Markman hearing and associated briefing. (*See id.* at 36-38.) To do otherwise, Netlist warns, is a "hasty approach [which] invites legal error." (*Id.* at 36 (citing *In re Certain Digital Processors & Digital Processing Sys.*, Inv. No. 337-TA-559, Comm'n. Op. 2006 ITC LEXIS 804, at *20-25 (Dec. 08, 2006)); *see id.* at 36-38 (citing *Certain Coenzyme Q10 Products and Methods of Making Same*, Inv. No. 337-TA-790, Order No. 42, 2012 ITC LEXIS 1681, at *5 (June 12, 2012); *Certain Video Analytics Software, Systems, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-795, Order No. 30, 2012 ITC LEXIS 1594, at *2 (July 12, 2012); *Certain Digital Models, Digital Data, And Treatment Plans For Use, In Making Incremental Dental Positioning Adjustment Appliances Made Therefrom, And Methods Of Making The Same*, Inv. No. 337-TA-833, Order No. 27, 2013 ITC LEXIS 294, at *31 (January 27, 2013)).) Netlist claims that "upon a proper construction of the presently asserted claims, there will be no basis for, or merit in, making an argument for issue preclusion." (*Id.* at 36.)

Netlist then draws attention to the "selectively allow" and "selectively isolate" limitations of the '185 patent which were found non-infringed and observes that none of the '907 patent

claims include these phrases. (*Id.* at 39.) Netlist reminds that "there is presumption that different meanings attach to different words when construing claims." (*Id.* (citing, *inter alia*, *Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005)).) More specifically, Netlist provides a table which compares the "selectively allow" and "selectively isolate" limitations from the '185 patent with "allowing" and "causing" limitations in the '907 patent. (*See id.* at 40.) In Netlist's view, "Respondents assert that the claims of the '907 require a 'selective' buffer circuit even though 'selective' appears nowhere in the claims." (*Id.* at 41 (referring to Resp1 at 5, 7).) Netlist argues "Respondents and Staff have yet to disclose in this Investigation, however, how they plan to read the '*selectively* allow' and '*selectively* isolate' limitations into the claims of the '907 patent." (*Id.*)

Moving on, Netlist claims the "actual express claim language of the '907 and '623 refutes an argument that the claims are identical, or 'materially similar,' to the claims asserted in the 1023 Investigation." (*Id.* at 43.) Netlist characterizes the 1023 Investigation as having a "full focus with regard to the '185 patent was data buffer circuits that were required to perform 'selective' allowance and 'selective' isolation" (*id.* (citing 1023 ID at 125) (emphasis in original)) and states "[t]he absence of such 'selective' data buffers in the accused products was the ID's sole basis for finding non-infringement" (*id.* at 43-44 (citing 1023 ID at 122)). In contrast, according to Netlist:

> None of the asserted claims of the '907 patent include data buffer circuits that "selectively allow" or "selectively isolate". Instead, the claims of the '907 patent focus on "allowing" or "causing" communication through a data buffer in a way that is not claimed as selective, while memory devices output or receive data based on control signals from a module control circuit—functionality that in no way implicates "selective" data buffers.

(*Id.* at 44.)

Netlist then disputes the idea that any prosecution history disclaimer from the '185 patent, whether found by the 1023 ID or not, can bind the claims of the '907 patent:

> Respondents take the untenable position that the ID broadly and expansively determined that the patent owner forever disclaimed everything but data buffers configured to "*selectively* allow" and "*selectively* isolate," as claimed in the '185 patent, from the scope of ***every*** other patent in the '185 patent family, including the '907 patent, irrespective of whether those other family members claim "selectively allowing" and "selectively isolating[.]"

(*Id.* at 45.) Rather, according to Netlist:

> The ID only determined that when the applicant amended the claims of the '185 patent to recite (buffer) circuits that "*selectively allow*," the claim language as amended in the '185 patent requires a buffer circuit "to select the memory device . . . to divorce one subset of memory devices from another."

(*Id.* (citing 1023 ID at 126-127).) Netlist argues that the 1023 ID could not have found the patent owner disclaimed anything from the '907 patent because "although a parent patent's prosecution history may inform the claim construction of its descendant, the parent patent's prosecution history is *irrelevant* to the meaning of this limitation because the two patents do not share the same claim language." (*Id.* at 46 (citing *ResQNet.com, Inc.*, 346 F.3d at 1383; *Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1182 (Fed. Cir. 2006)).)

With respect to the *Hakim* case often cited by Respondents, Netlist explains "the patentee disavowed subject matter from the scope of its alleged invention as a whole to avoid an obviousness rejection, and then the claims of a continuation application were allowed, without further prosecution or discussion, for the same reason. " (*Id.* at 47-48 (citing *Hakim*, 479 F.3d at 1317).) Netlist contrasts this with the '185 patent where "there was no clear and unequivocal disclaimer of applicant's invention nor any disclaimer that would extend beyond the scope of the '185 patent itself." (*Id.* at 48 (internal citation omitted).) Netlist claims the patentee "informed the PTO examiner in applicant's remarks that the claims presented in the application

for the '907 patent were broader in scope than those of the '185 patent *by informing the examiner that the claims of the '907 patent mapped to the 'straight line' embodiments disclosed in the specification.*" (*Id.* (emphasis added).)

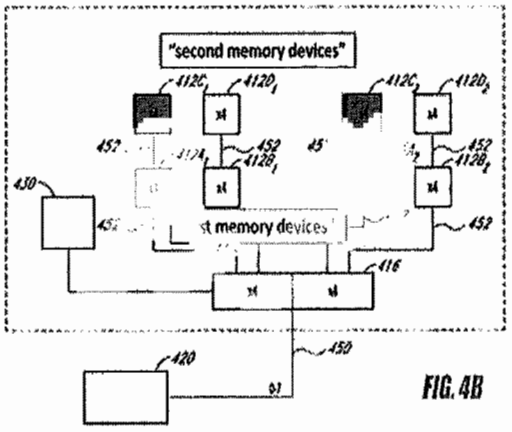
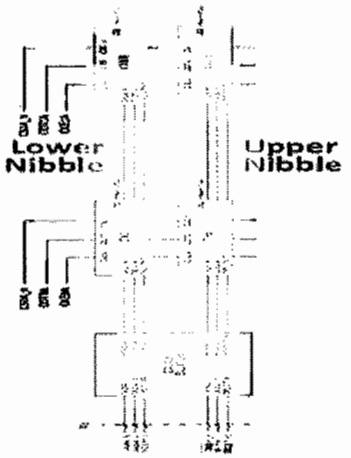
Moving on, Netlist argues flatly that the intrinsic evidence confirms "allow" is different than "selectively allow," and thus different than the "fork in the road" coined by Respondents. (*Id.* at 49.) For support, Netlist looks to Figure 4B of the '907 patent and the following table authored by the applicant during the '907 patent's prosecution:

Cl #	Amendment	Support
4 12	each respective buffer circuit being coupled to a respective set of the *M* sets of *n* data lines, to respective one or more of the first memory devices via a set of *n* module data lines, and to respective one or more of the second memory devices via the set of *n* module data lines	As shown in FIGS. 4A and 4B, memory device 412A (or memory devices $412A_1$ and $412A_2$) (respective one or more of the first memory devices) and memory device 412C (or memory devices $412C_1$ and $412C_2$) (respective one or more of the second memory devices) are coupled to the buffer circuit 416 via a same set of 8-bit data lines 452.

(*Id.* at 50 (internal citation omitted).) Netlist claims extrinsic evidence (expert testimony from the 1023 Investigation) supports the nothing that "allows" or "causes" communication is different from "selectively allows" or "selectively isolates." (*Id.* (internal citation omitted).)

Finally, Netlist argues "Respondents deliberately and expressly distinguished 'allowing' from 'selectively allowing' to achieve the result they sought in the 1023 Investigation . . . . [and] cannot now equate data buffers that 'allow' communication with data buffers that 'selectively allow' communication to make an issue preclusion argument with regard to the '907 patent." (*Id.* at 51 (citing 1023 ID at 122, 124-125).) Netlist goes so far as to claim "Respondents' successful arguments and the ID's corresponding findings in the 1023 Investigation support a finding of infringement of the '907 patent in this Investigation" and points to how elements 412A and 412C from the '907 patent match up with accused product specifications (where the

signal goes to all memory devices on the same Lower or Upper nibble bus") as in the following demonstrative:

"Straight Line" Arrangement	
'907 Patent	**Respondents' Accused Products**
 '907 patent, Figure 4**B** (annotated)	 RDX-1584C.057 (excerpt)

(*Id.* at 52.) Netlist reasons, "[t]his is the same 'allowing communication' claimed in the '907 patent." (*Id.* at 53.)

In its second submission, in response to the Staff, Netlist observes:

> Staff does not support Respondents' primary issue preclusion argument with regard to the '907 patent. Whereas Respondents argue that (i) the prosecution history of the parent '185 patent and (ii) the ID's findings in the 1023 Investigation operate to disclaim and limit the scope of the claims of the child '907 patent (Mot. at 23-31), Staff's view is that "*these two issues, alone, would not support a summary judgment determination of non-infringement of the claims of the '907 patent.*" Staff Br. at 29 (emphasis added); Netlist Resp. Br. at 43-49.

(Netlist2 at 1-2.) While the Staff did ultimately conclude issue preclusion is warranted based on the '907 patent's history, Netlist argues that it has not met the "clear and unmistakable" standard required by law. (*Id.* at 2 (citing *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1063-64 (Fed. Cir. 2016)).) More specifically, Netlist argues neither the "applicant's cancellation of dependent claims directed to "groups" of memory devices that couple to 'a same set of terminals'" nor the

"applicant's identification of *examples* of embodiments that support the '907 patent's claims," as referenced by the Staff, is sufficient to support disclaimer of claim scope. (*See id.* at 3-12.) In Netlist's view, "[w]hat the ['907 patent] independent claims require is a 'straight line' configuration" (*Id.* at 12), and, again, "contrary to Staff's apparent assertion, there is no requirement in the claims or prosecution history of the '907 patent for any type of 'fork' in the road" (*Id.* at 9.)

In its third submission, a response to Respondents, Netlist perceives Respondents as "jettison[ing], for good reason, their claim of clear and unmistakable prosecution history disclaimer," and in its place, according to Netlist, "argu[ing] for the first time in their Reply Brief, that the express claim language of the '907 patent, which requires a first memory device to 'output or receive data' while a second memory devices does 'not output or receive data,' mandates a 'fork in the road' layout and excludes Netlist's 'straight line' embodiment." (Netlist3 at 7 (referring to Resp2 at 26-27).) Netlist claims the previous argument was "dismantled by Staff's and Netlist's Response Briefs." (*Id.*) Netlist then argues, citing a variety of precedent, that "[a]rguments raised for the first time in a reply brief are waived." (*Id.* at 7-8 (internal citations omitted).) Netlist then argues that, regardless, Respondents have cited no intrinsic evidence to support their interpretation of "do not output or receive any data," as well as mischaracterize the extrinsic evidence. (*Id.* at 8 (citing Resp2 at 26-27).)

With respect to the particulars, Netlist argues:

> It cannot be disputed that (i) the '907 patent's specification discloses a "straight line" embodiment and (ii) the Applicant stated expressly during prosecution that the '907 patent's claims are directed to this embodiment. Specifically, and as Netlist has pointed out in its prior briefing, the Applicant identified memory devices 412A and 412C as the claimed first and second memory devices, respectively, which are arranged in a straight line.

(*Id.* at 8.) Thus, Netlist proffers, "Respondents also erroneously interpret the claim language 'output or receive' and 'does not output or receive' as being synonymous with a 'fork in the road.' It is not." (*Id.* at 9 (referring to Resp2 at 26-27).) Netlist states simply "[t]his '907 patent claim language does not require a 'fork in the road.'" (*Id.*)

Netlist argues:

> Starting with the plain language of the claims, the '907 patent is clear that it is only in response to module control signals that the memory devices will output or receive data. That is, that the claimed "first module control signals" cause the first memory devices to output or receive data while the second memory devices do not output or receive data.
>
> . . . .
>
> the '907 specification specifically discloses that such module control signals can be provided to memory devices arranged in a straight line.

(*Id.*)

Critically, Netlist points to three specification excerpts in support of the idea that the '907 patent discloses that "chip-select signals" "cause a single rank of memory devices to receive or output data (*e.g.*, memory devices 412A) and another rank of memory devices (*e.g.*, 412C) to not output or receive data." (*Id.* at 9-10.) Netlist's proposed support is reproduced below:

> During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals."
>
> . . . .
>
> The control circuit 430, 430′ of certain embodiments is configurable to be operatively coupled to control lines 440, 440′ to receive control signals (*e.g.*, bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller 420, 420′.
>
> . . . .

> The control circuit 430, 430′ may produce additional chip-select signals or output enable signals based on address decoding.

(*Id.* at 10 (citing '907 patent at 1:51-55; 10:24-29; 10:39-41) (emphasis in original).)

Netlist continues to claim that the '907 patent "makes clear" that the same "chip-select signals" can select a first rank of memory to receive data while other ranks are not selected to receive data during a write operation—even when the first and other ranks are "located in a 'straight line' on the same data path. (*Id.*) Again, Netlist's alleged support for this assertion is reproduced below:

> Therefore, *during a write operation in which data is to be written to a single memory device 412* in a rank of the memory module 400.
>
> . . . .
>
> Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, *each specific operation is targeted to a specific one of the ranks A, B, C, and D* of a specific memory module 402.

(*Id.* (citing '907 patent at 14:62-63, 17:5-8) (emphasis in original).) Netlist reasons "whether a memory device 'outputs or receives' or 'does not output or receive' data is not a function of, and does not require, Respondents' 'fork in the road.'" (*Id.*) Netlist concludes with citation to the '907 prosecution history where, allegedly, the Examiner found that the claims allowed for chip-select signals to work this way. (*Id.* at 11 (internal citations omitted).)

Netlist then disputes that its expert, Dr. Baker, corroborated Respondents' position through statements made in a patent office proceeding on the '185 patent. (*See id.* at 11-13.) Essentially, Netlist argues the difference in claim terms between the '185 and '907 patents make Dr. Baker's testimony irrelevant, and even then, he "did not comment at all regarding the meaning of the word 'receive' in the context of the '907 patent's claims." (*Id.* at 12) To the contrary, Netlist claims, it is Respondents' expert testimony of "[t]he memory controller also

activates chip select signal CS0A_n so that the memory chips D0 and D5 in the first rank can receive and process the data" which supports finding infringement of the '907 patent. (*Id.* at 12 (emphasis removed).) Netlist explains, again, that "in response to chip-select signals, one memory device on a data path will output or receive data while the other memory device on the same data path will not. This interpretation aligns with Complainant's and Staff's interpretation of the term." (*Id.* at 13.)

iii. Staff's Contentions

As mentioned above, the Staff "supports the motion with respect to a summary determination of non-infringement based on issue preclusion." (Staff1 at 1.) The staff summarizes "that finding infringement of the asserted claims of the Asserted Patents would require re-litigation of essentially the same infringement disputes resolved in the 1023 investigation." (*Id.* at 17 (referring to Restatement (Second) of Judgments § 27, Comment c, at 252–253).) The Staff reasons "by applying the final findings of fact and law from the 1023 investigation, there remains no question of fact that the same Accused Products adjudicated to be non-infringing in the 1023 investigation do not infringe the Asserted Patents in the 1089 investigation." (*Id.*)

With particular respect to the '907 patent, the Staff identifies the issues as "whether the claimed buffer circuit must divorce selected memory devices from unselected memory devices when 'allowing' data transmission" or "whether the claimed memory buffer may allow the data to be communicated to all memory devices - both selected and unselected memory devices." (*Id.* at 18 (citing Resp1 at 23-30; 1023 ID at 127).) The Staff also argues that the prosecution of the '185 patent included a disclaimer on the scope of "data buffers" which limits "memory buffer" in the '907 patent in the same way. (*Id.* at 19 (citing Resp1 at 28-30).) Thus, according to the Staff:

> [T]he 1023 ID's findings require finding no infringement of the '907 patent because the invention's claimed "data buffer" is limited to data buffers that only allow communication to selected memory devices – to the exclusion of others (*i.e.* no recapture of the "memory buffer" claim scope found to be disclaimed in the 1023 ID); and there is no material dispute that the accused buffer circuits allow communication to *all* memory devices. *See* 1023 ID at 125 ("However, in utilizing those directional and timing controls, the DBs assert control over *all* of memory devices of the LRDIMM. This distinction is critical to determining whether the LRDIMM infringe.") (emphasis in original).

(*Id.*)

Moving back to other elements of issue preclusion, the Staff agrees with Respondents that "there can be no reasonable dispute that: (i) the two investigations involve the same parties, (ii) that Complainant had a full and fair opportunity to litigate the issues; and (iii) the non-infringement issue were actually litigated and necessary to the 1023 ID finding of no violation, which the Commission made final." (*Id.* (citing Resp1 at 16-19; 1023 ID at 94, 124-126).) The Staff continues, "there is no material dispute that the relevant infringement disputes for the 1089 investigation involve the same Accused Products and same accused functionality as the 1023 investigation." (*Id.* at 20 (citing Resp1 at 17; Netlist's Response to Public Interest Comments, EDIS Doc No. 629397, at 4).)

With respect to identity of issues, the Staff states "there is no material dispute that the two issues [described above] litigated in the 1023 investigation are identical to issues in the non-infringement dispute in the 1089 investigation." (*Id.* at 28.) Again, Staff argues "that prosecution history disclaimer limits the scope of the inventions' buffer circuit in the claims of the '185 patent should be applied to the infringement analysis in the 1089 investigation" and "the finding that the Accused Products' data buffers allow communication to *all* memory devices should not be re-litigated in the 1089 investigation." (*Id.* at 29.)

The Staff claims that these two issues alone do not support summary determination, but do when combined with the disclaimer finding in the 1023 ID and the disclaimer of the '907 patent regarding "buffer circuits." (*Id.* (internal citations omitted).) In short, Staff explains:

> Because "buffer circuit" in the claims of the '907 patent have the same scope as the "circuit of the plurality of circuits" of the '185 patent, (*i.e.* "data buffer" or "DB" in the 1023 ID), issue preclusion applies and supports finding a summary determination of non-infringement.

(*Id.* at 30.) The Staff then proceeds with an analysis of the '907 patent prosecution history (see *id.* at 32-36) to support the ideas: "for the purposes of the '185 patent, the patentee limited the scope of the invention's buffer circuit to circuits that only allow communication to a subset of memory devices – as opposed to *all* memory devices" (*id.* at 30); and "the patentee never indicated that the claimed 'buffer circuit' in the '907 patent should be broadened to encompass data buffers that transmit to both selected and unselected memory devices" (*id.* at 31). In particular, the Staff points to a rejection for lack of written description over the "shared terminal" claim term (*see id.* at 31-34) and the patentee's explanation of support for "buffer circuit including logic" from the specification (*see id.* at 35-36).

Thus, the Staff argues, under *Hakim*, "the limitations have the same scope, and are not infringed by the Accused Products" (*id.* at 31 (citing *Hakim*, 479 F.3d at 1317)) because "all independent claims require a 'buffer circuit' with logic to allow communication to a subset of memory devices" (*id.* at 37).

iv. Analysis

Under Federal Circuit law, issue preclusion can be applied only if:

> (1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) the plaintiff had a full and fair opportunity to litigate the issue in the first action.

Semiconductor Integrated Circuits, Inv. No. 337-TA-648, Comm'n Op. at 2-3 (citing *In re Freeman*, 30 F.3d at 1465). With respect to the '907 patent, Respondents and the Staff contend that factors (2) through (4) are not in dispute. (*See* Resp1 at 16-17; Staff1 at 21, 28.) Netlist's initial opposition appears to dispute factor (3), essentiality to judgment, based on its section heading (*see* Netlist1 at 43 ("Issue Preclusion Does Not Apply To The '907 Patent Because Whether the Accused Products 'Allow' Communication Between First Memory Devices and the Memory Controller Was Not Essential to the Judgment in the 1023 Investigation")), but the substance of Netlist's opposition is factor (1)—whether or not the issues (*i.e.*, scope of claim terms), are identical. (*See generally id.* at 43-53.)

To begin, below are the findings from the 1023 ID which I find relevant to the pending motion:

> There is only one disputed claim term relevant to the asserted claims of the '185 patent: "selectively isolate." (CIB at 108-109, CRB at 58-59, RIB at 12-14, RRB at 4-5, SIB at 133-136 and SRB at 44-45.) The term "selectively isolate" appears in independent claim 1 from which claims 2, 3, 5, 7, 8 and 10-12 depend.

(1023 ID at 116);

> Second, the express language of independent claim 1 provides that "each circuit of the plurality of circuits...[is] operatively coupled to at least two corresponding memory devices" and that the "at least two corresponding memory devices" are "configured" (i) "*to selectively allow data transmission between the system memory controller and at least one selected memory device*" (which for convenience can be called a "first" memory device) and (ii) "*to selectively isolate at least one other memory device of the at least two corresponding memory devices* from the system memory controller" (which for convenience can be called an "other" memory device(s) different from the "first" memory device). As can be seen from this breakdown, the claim language already embraces the concept of "separating one component from another" as set forth in Respondents' proposed construction. That is, the claim plainly distinguishes the "first" memory device from the "at least one *other* memory device."

(*id.* at 119-120);

> The above-discussed claim language makes clear that the "first" memory device is in communication with the system memory controller while the "other" memory device is "selectively isolated" from the system memory controller. According to the '185 patent, the memory controller of conventional/prior art memory systems sees "all the memory devices" as its load during write operations and that such causes performance deficiencies. (JX-0002 at 4:47-52; 4:65-5:4; 5:41-46; 5:59-65.)

(*id.* at 120);

> Thus, the intrinsic evidence establishes that the term "isolate" refers to "electrically isolating" or "electrically separating."

(*id.* at 121);

> In view of the testimony of Complainant's expert that the LRDIMM include all of the features of independent claim 1 except "Selective Allowance" and "Selective Isolation" features, and there being no clear disagreement by Respondents and Staff as to that fact, the undersigned finds that the LRDIMM includes these features (*i.e.*, all of the features except the "Selective Allowance" and "Selective Isolation" features) of independent claim 1. *See* CX-0004C at Q/A 426-466, 483-502.

(*id.* at 122);

> Independent claim 1 recites, in relevant part, that each of the plurality of circuits is configured "to selectively allow data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals."

(*id.* at 122-123);

> According to Complainant, the accused LRDIMM includes data buffers ("DBs"), and that "the DB controls data transmission according to the direction of data (*e.g.*, read, write) and timing (*e.g.*, rank-specific timing, CAS latency, etc.) and therefore satisfies the 'selectively' requirement of claim 1 in multiple ways." (CIB at 112.) For example, Complainant asserts that in the LRDIMM "the DB performs rank-specific timing adjustment based on which rank (*e.g.*, group) of memory devices is selected to ensure that data will be transmitted to or received from the selected memory devices correctly." (*Id.* at 113 (citing CX-0004C at Q/A 272-85, 475; Subramanian, Tr. at 675:1-685:4).) Complainant

> similarly cites other operations of the DBs of the LRDIMM purporting to demonstrate that the DBs "selectively allow data transmission." (*Id.* at 111-17.)

(*id.* at 123);

> Respondents and Staff disagree that the DBs of the LRDIMM "selectively allow" there to be data transmission. In doing so, they focus on whether the control of the data transmission in the LRDIMM is "selective" as that term should be understood in the context of the '185 patent and, in particular, what exactly is being selected. (RIB at 15-16, RRB at 5-7, SIB at 138-139 and SRB at 45-47.)

(*id.* at 123-124);

> Respondents argue that "the accused DBs in the accused products do *not* selectively allow data transmission to one rank and not the other (instead data is transmitted to *all* ranks, and a prior-art chip select signal from the system memory controller to a given rank of memory tells that rank of memory to listen for the incoming data), and the accused DBs do *not* selectively isolate a given rank from the memory controller on the host computer (instead *all* ranks are isolated)." (RIB at 15 (citing RX-1584C at Q/A 81-92, 104-117; *see also* Brogioli, Tr. 468:15-22, 471:1-7, 472:23-473:7, 474:7-20 (admissions by Brogioli that the DBs send data to *all* ranks of memory, not just selected ranks of memory); *id.* at 485:19-486:2 (admission by Brogioli that "there's no fork in the road" in the accused products); *id.* at 476:23-477:2, 478:17-479:6, 480:21-25, 481:15-20 (admissions by Brogioli that the DBs *always* isolate, they do not selectively isolate)); *see also* RIB at 16 and 18.)"

(*id.* at 124);

> In sum, Respondents and Staff take the position that even if the DBs of the LRDIMM utilize directional and timing controls that are selective, the effect of those "selective" actions does not amount to discriminating between memory modules such that some participate in data transmission to the exclusion of others.

(*id.* at 124);

> Based on Complainant's evidence and arguments, it appears that the DBs of the LRDIMM utilize directional (*i.e.*, read/write) and timing controls to determine the *order* in which data is transmitted as opposed to controlling whether only a selected subset of memory devices participate in that communication to the exclusion of other memory devices.

(*id.* at 125);

> As can be seen, the applicant argued that the distinction with Rajan was not simply related to separating the memory controller and the memory devices by virtue of an intervening component (*i.e.*, a buffer chip). Rather, the applicant argued that the claimed subject matter was distinguishable because it involved allowing only a selected subset of the memory devices—to the exclusion of others—from communicating with the memory controller. Indeed, Complainant's expert (Baker) acknowledged that "[t]he big difference, in simple terms, between Rajan and the '185 [patent] is Rajan is not using the buffers to ***select the memory device***." (Baker, Tr. 1004:17-22 (emphasis added).) Thus, the amendment and accompanying argument made clear that the "selectively allow" and the "selectively isolate" features are related in terms of their ability to choose and treat separately the "first" memory devices from the "other" memory devices with respect to the memory controller. Complainant's evidence, however, fails to establish that the "selective" actions it cites divorce one subset of memory devices from another; rather the evidence of record shows that the cited actions are directed to selecting the order and direction in which *all* of the memory devices collectively operate. (*See* RX-1584C at Q/A 81-92, 104-117.)

(*id.* at 126-127);

> The parties and Staff set forth generally the same arguments and reasoning with respect to the "selective isolation" as they did regarding the "selective allowance" feature. (CIB at 118-120, CRB at 61-62, RIB at 15-16, RRB at 7-8 and SRB at 45-47.) Accordingly, a similar analysis—and outcome—is warranted.

(*id.* at 128);

> As with "selective allowance" Complainant's evidence is again directed to the "rank-specific timing" and how it is used to order the memory modules in electrical relationship to memory controller. (CIB at 118-120.) However, those actions are applied to all of the memory devices, not a selected subset.

(*id.* at 128);

> Thus, by Complainant's own admission the "selective" operational controls of the LRDIMM that it relies upon to establish infringement apply to all of the memory modules and do not selectively differentiate between different subsets thereof such that

> only certain memory devices are separated from the memory controller and others are not.

(*id.* at 128-129).

In light of the parties' arguments and the above excerpts, I find factors (2) through (4) of the issue preclusion test are met. The claim terms of the '185 patent which are alleged to be "identical" to terms in the '907 patent, "selectively allowing" and "selectively isolate," were actually litigated in the 1023 Investigation and essential to the final judgment. (*See* 1023 ID at 89-96.) Additionally, Netlist, as complainant in the 1023 Investigation, had a full and fair opportunity to litigate the meaning and infringement of those claim terms. (*See id.*)

Thus, the resolution of factor (1) will be dispositive of Respondents' motion. While this factor is recited as "the issue is identical to one decided in the first action," the Federal Circuit has explained that "[c]omplete identity of [patent] claims is not required to satisfy the identity-of-issues requirement for claim preclusion." *Soverain Software*, 778 F.3d at 1319. Rather, "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342.

Under this standard, I find no material difference between "selectively allow / selectively isolate" from the '185 patent and the '907 patent's "output or receive / do not output or receive" terms. The Commission has already determined the accused products do not "control[] whether only a selected subset of memory devices participate in that communication to the exclusion of other memory devices." (1023 ID at 125.) Thus, I simply do not see what is left for me to decide. For ease of reference, I present the relevant claim language side-by-side in the following table.

'185 Patent	**'907 Patent**			
Claim 1	*Claims 1, 16*	*Claim 43*	*Claim 53*	*Claim 58*
configured to *selectively allow* data transmission between the system memory controller and at least one selected memory device of the at least two corresponding memory devices in response to the module control signals, and to *selectively isolate* at least one other memory device of the at least two corresponding memory devices from the system memory controller in response to the module control signals,	in response to the first module control signals, the first memory devices *output or receive* each N-bit wide data signal associated with the memory read or write command while the second memory devices *do not output or receive* any data associated with the memory read or write command;	in response to the output address and control signals, the subset of the memory devices *output or receive* the data associated with the memory read or write command while other memory devices not in the subset of the memory devices *do not output or receive* any data associated with the memory read or write command	in response to the output address and control signals, the first memory devices *output or receive* each N-bit wide data signal associated with the memory read or write command while the second memory devices *do not output or receive* any data associated with the memory read or write command	in response to the first output address and control signals, the first memory devices *output or receive* data associated with the first memory read or write command while the second memory devices *do not output or receive* any data associated with the first memory read or write command,

From the above table, I find the language of the '185 and '907 patent claims both recite control signals which, in general terms, allow a first subset of memory devices to communicate data with an external system memory controller *while* preventing a second subset of memory devices from doing the same. I find these terms present a sufficiently identical issue for several reasons.

First, as recited in the claims, both "selectively allow / selectively isolate" and "output or receive / do not output or receive" are triggered by what is essentially the same signal. In

the '185 patent it is called a "module control signal." In the '907 patent it is the same "module control signal" or otherwise called "output address and control signals" ('185 patent at cl. 1; '907 patent at cls. 1, 16, 43, 53, 58; *see also* Netlist3 at 9 ("the '907 patent is clear that it is only *in response to module control signals* that the memory devices will output or receive data")). Yet neither the claims, nor the specifications, identify or suggest any meaningful distinction between "module control signal" and "output address and control signals." To the contrary, both signals are "produce[d]" the same way—by a memory module's controller and based on "control information" or "input address and control signals" provided by an external system memory controller. ('185 patent at cl. 1; '907 patent at cls. 1, 16, 43, 53, 58.)

Second, also as recited in the claims, both "selectively allow / selectively isolate" and "output or receive / do not output or receive" accomplish the same thing—place a first subset of memory devices in data communication with an external system memory computer, and remove a second subset. ('185 patent at cl. 1; '907 patent at cls. 1, 16, 43, 53, 58.) They do this because it reduces the loads seen by the system memory controller (during write operation) and by the memory devices (during read operation). (*Compare* '185 patent at 5:41-46 *with* '185 patent at 16:12-30; compare '907 patent at 5:50-55 with '907 patent at 16:36-55.) The 1023 ID described this as "reduce the load on the memory controller by presenting only the load from specifically coupled and enabled memory devices." (1023 ID at 120-121.) Moreover, there is no evidence, and no party has argued, that a meaningful difference in scope exists between the "data transmission" ('185 patent), "data" ('907 patent), or "data signal" ('907 patent) which is communicated.

Third, along with the causes and effects of the terms are the same, I do not find any evidence showing differences in how they operate—*i.e.*, how the flow of data communication is controlled. These differences would have been an important indicator that claim preclusion

should not apply, *Ohio Willow Wood*, 735 F.3d at 1342-43 ("Since OWW failed to explain how the 'block copolymer' limitation changes the invalidity analysis, OWW has not met its burden of opposing summary judgment based on this distinction."), but here there are none.

Fourth, the 1023 ID resolved the "selectively allow / selectively isolate" issue in terms that arguably resolve whether the same accused products have memory devices which "output or receive" data while other memory devices "do not output or receive" that data. The 1023 ID found that Complainant did not show "a selected subset of memory devices participate in that communication to the exclusion of other memory devices" or "that the 'selective' actions it cites divorce one subset of memory devices from another:"

> Based on Complainant's evidence and arguments, it appears that the DBs of the LRDIMM utilize directional (*i.e.*, read/write) and timing controls to determine the *order* in which data is transmitted as opposed to controlling whether only a selected subset of memory devices participate in that communication to the exclusion of other memory devices.
>
> ....
>
> Complainant's evidence, however, fails to establish that the "selective" actions it cites divorce one subset of memory devices from another; rather the evidence of record shows that the cited actions are directed to selecting the order and direction in which *all* of the memory devices collectively operate.

(1023 ID at 125-127 (emphasis in original).) I see a parallel between outputting or receiving data ('623 patent) and participating in communication of data (1023 ID). This clearly supports an identity of issues between the claim terms.

Finally, I find that even Netlist's "straight line" embodiment still incorporates a "fork in the road" concept because of the explicit "output or receive / do not output or receive" claim language. It is inescapable.

To begin, I agree with Respondents' observation (*see* Resp2 at 19) that while Netlist argues "there is *no requirement* in the claims or prosecution history of the '907 patent for any type of 'fork' in the road" (Netlist2 at 9), they omit discussing the "output or receive / do not output or receive" terms entirely (*see* Netlist1 at 12 (writing "do not output or receive" as in a block quote of claim text); Netlist2 at 1-14 (no mention of "do not output or receive")).

It is not until Netlist's third submission that it addresses "output or receive / do not output or receive" and argues a "chip-select signal" within its "straight line" interpretation is what accomplishes this discrimination:

> The specification also makes clear that the chip-select signals can select a single rank (*e.g.*, first memory devices 412A) to receive data while other ranks (*e.g.*, second memory devices 412C) are not selected to receive data during a write operation, notwithstanding that the memory devices are located in a "straight line" on the same data path.

(Netlist3 at 10.)[3] Netlist's cited specification excerpts, reproduced below, do not say this however:

> Therefore, during a write operation in which data is to be written to a single *memory device 412* in a rank of the memory module 400.
>
> . . . .
>
> Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, *each specific operation is targeted to a specific one of the ranks A, B, C, and D* of a specific memory module 402.

('907 patent at 14:62-63, 17:5-8; *see* Netlist3 at 10.) When read in context, first excerpt is not in reference to chip-select signals but the ability of the data transmission circuit 416 (*i.e.*, buffer

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[3] I also note here the ironic nature of Netlist's position that "Respondents argue, for the first time in their Reply Brief, that the express claim language of the '907 patent, which requires a first memory device to "output or receive data" while a second memory devices does "not output or receive data," mandates a "fork in the road" layout and excludes Netlist's "straight line" embodiment" (Netlist3 at 7) and argument that "[a]rguments raised for the first time in a reply brief, are waived" (*id.*).

circuit) to "electrically couple" and "electrically isolate" memory devices from the system memory controller. ('907 patent at 14:55-62.) The second also does not mention chip-select signals and, when read in context, actually describes data "driven to memory devices 412A and 412C or 412B and 412C depending on which memory devices are active and enabled" *as opposed to* 412A or 412C under Netlist's "straight line" embodiment.

Regardless, Netlist's contention reveals that even in its "straight line" embodiment there is a "fork in the road" for the data flow to go down. In Netlist's own words, "in response to chip-select signals, one memory device on a data path will output or receive data while the other memory device on the same data path will not." (Netlist3 at 13.) Netlist may characterize the memory devices as "on the same data path," but a "fork in the road" still exists for the transmitted and received data to go to some *but not all* of those memory devices—the exact issue litigated to finality in the 1023 Investigation:

> As with "selective allowance" Complainant's evidence is again directed to the "rank-specific timing" and how it is used to order the memory modules in electrical relationship to memory controller. (CIB at 118-120.) However, those actions are applied to all of the memory devices, not a selected subset.
>
> ....
>
> Thus, by Complainant's own admission the "selective" operational controls of the LRDIMM that it relies upon to establish infringement apply to all of the memory modules and do not selectively differentiate between different subsets thereof such that only certain memory devices are separated from the memory controller and others are not.

(1023 ID at 128-129.)

I find the similarity between the '185 and '907 patent claim terms overwhelms other issues contained in the parties' filings. For example, whether the claimed "first memory devices" and "second memory devices" can only be 412A and 412C, as opposed to 412A/412C

and 412B/412D (*see* Netlist1 at 14-16, 49-51; Resp2 at 25-29; Netlist2 at 8-9; Netlist3 at 8; *see generally* Mot., Ex. 10 at 428-434) is of little import because a "fork in the road" for the data flow is still required and that issue has already been resolved. Similarly, whether the applicant disclaimed all "buffer circuits" besides those that "selectively allow[]" or "selectively isolate" during prosecution of the '185 patent; or whether the applicant sufficiently notified the Examiner that it wished to reclaim that scope in the '907 patent (*see* Staff1 at 28-37; Netlist2 at 3-12) does not matter much either. A "fork in the road" is still needed under the "output or receive / do not output or receive" claim language. Whether, on the whole, the '907 patent claims are broader than the '185 patent claims (*see* Netlist1 at 33, 48; Resp2 at 12) is equally unimportant. *Again*, a "fork in the road" dividing two groups of memory devices is still needed due to the "output or receive / do not output or receive" claim language.

I also find the above circumstances line up with the Federal Circuit's rationale in both *Ohio Willow Wood* and *Soverain Software*. In *Ohio Willow Wood*, the court considered two claims which, on their face, looked quite different:

> 1. A tube sock-shaped covering for enclosing an amputation stump, said amputation stump being a residual limb, said covering having an open end for introduction of said residual limb and a closed end opposite said open end, said covering comprising fabric in the shape of a tube sock, said fabric having a coating of a foamed or non-foamed block copolymer and mineral oil gel composition residing on only an interior surface thereof.
>
> . . . .
>
> 1. A cushion liner for enclosing an amputation stump, said liner comprising a fabric covering having an open end for introduction of said stump and a closed end opposite said open end, said fabric coated seamlessly on only an inside surface thereof with a polymeric cushioning gel that substantially conforms to the shape of said amputation stump when said liner is worn; wherein said liner is configured such that said polymeric cushioning gel is in contact with the skin of said amputation stump when said liner is worn by a user thereof.

735 F.3d at 1342. Nevertheless, the court held:

> [T]hese patents use slightly different language to describe substantially the same invention. For example, where the '237 patent recites a "tube sock-shaped covering," an "amputation stump being a residual limb," and "fabric in the shape of a tube sock," the '182 patent analogously recites the same claim scope in the form of a "cushion liner for enclosing an amputation stump, said liner comprising a fabric covering having an open end for introduction of said stump and a closed end opposite said open end." Thus, the mere use of different words in these portions of the claims does not create a new issue of invalidity.

Id. at 1342-43. The court further held that the patentee had failed to show "how the 'block copolymer' limitation changes the invalidity analysis" from the prior adjudicated term "polymeric," and thus had "not met its burden of opposing summary judgment based on this distinction." *Id.* at 1343.

In *Soverain Software*, the Federal Circuit considered whether issue preclusion applied to invalidate a dependent claim whose independent claim had previously been invalidated as obvious. 778 F.3d at 1319-20. The court considered whether the additional limitation supplied by the dependent claim (clarifying that an aforementioned network is "an Internet") would change an invalidity analysis, and held it would not. *See id.* at 1319. The court thus reasoned that "the routine incorporation of internet technology in claim 39 does not change the invalidity analysis." *Id.* at 1320.

I find Netlist is in the same position as the patentees in *Ohio Willow Wood* and *Soverain Software*. "Selectively allow / selectively isolate" and "output or receive / do not output or receive" are different language but they describe essentially the same feature of discriminating between memory devices for data communication. Additionally, I do not find Netlist has shown a meaningful difference in scope that might affect an infringement analysis.

Finally, Netlist's initial argument—that a decision on Respondents' motion is premature before any Markman process is complete (Netlist1 at 36-43)—is not persuasive for the simple fact that a Markman process is not mandatory to a section 337 investigation. Rather, it is a tool I *elect* to use to simplify cases. It therefore makes little sense to say that any determination implicating the meaning of a claim term must necessarily wait until after Markman.

Thus, I find no material difference between "selectively allow / selectively isolate" data transmissions ('185 patent at cl. 1) and "output or receive / do not output or receive" data signals ('907 patent at cls. 1, 16, 43, 53, 58). As the satisfaction of issue preclusion's other factors are met and not in dispute, I GRANT Respondents' motion of summary determination of non-infringement under the '907 patent under issue preclusion.

c. Issue Preclusion and the '623 Patent

i. Respondents' Contentions

In their opening memorandum, Respondents begin with the relevant procedural history of the '837 patent (the parent of the '623 patent) as:

> In the 1023 Investigation, the ALJ found that SK hynix's JEDEC-compliant DDR4 RDIMM and LRDIMM products do not infringe the asserted claims of the '837 patent. Ex. 1, ID at 89–99. As noted, the ALJ's decision rested on a close reading of claim 1 of the '837 patent, which requires a "*notification signal … indicating at least one status* of the at least one initialization sequence." Ex. 2, '837 patent (emphasis added). The ALJ found that this claim is not practiced by SK hynix's memory modules, because the "ALERT_n signal" of the accused standard-essential "Clock-to-CA" training mode in the SK hynix modules is not a notification signal that indicates the status. Ex. 1, ID at 95. Specifically, the ALJ held that the "'ALERT_n signal' generated from the memory module does not indicate a status of the 'Clock-to-CA training mode…." *Id.*

(Resp1 at 20.) In light of this history, and citations to a bevy of filings from the parties from the 1023 Investigation, Respondents claim that infringement of "indicating at least one status" from the '837 patent was fully litigated and "received a full and fair hearing." (*Id.* at 20-21.)

Turning to the '623 Respondents argue:

> The '623 patent is closely related to the '837 patent. As explained above, the two patents share a common application and specification, and the '623 patent is subject to a terminal disclaimer with the '837 patent. *Compare* Ex. 4, '623 patent, *with* Ex. 2, '837 patent; Ex. 13, '623 file history at 80–85. Critically, each and every independent claim in the '623 patent requires a "*notification signal indicating at least one status* of one or more training sequences." *See* Ex. 4 at claim 1 (emphasis added); *see also id.* at claim 12 ("*notification signal indicating a status* of the one or more training sequences"), claim 21 ("*notification signal indicating a status* of one or more training sequences.") (emphases added).

(*Id.* at 21.) Respondents add that "[j]ust as in the 1023 Investigation, Netlist alleges that the ALERT_n signal in SK hynix's memory modules infringes the notification signal limitation in Netlist's patent." (*Id.* at 22 (citing Mot., Ex. 9 at 25).) As a result, according to Respondents, "the 1023 Investigation dictates the outcome here" (*id.*) as "the Commission determined that 'ALERT_n' signals 'do not amount to a status,' as all claims require" (*id.* at 23 (citing 1023 ID at 96).)

Respondents further represent that "[d]uring the meet and confer on this motion, Netlist's only argument against issue preclusion was that the '623 patent requires a notification signal that indicates the status of a "training sequence," but the '837 patent claims require a notification signal that indicates the status of an "initialization sequence." (*Id.*) Respondents call this a "distinction without a difference" (*id.*) in light of the shared specification which, as determined by the 1023 ID, "makes clear that the initialization mode of independent claim 1 can include a training sequence" (1023 ID at 90-91 (referring to '837 patent at 5:44-51).)

In their response to Netlist's opposition, and as mentioned above, Respondents contend that waiting until after a "full claim-construction briefing and a *Markman* hearing," as Netlist argues, "would waste Commission resources and result in costly and unnecessary discovery and litigation and accomplish nothing because the decisive analysis will be the same." (Resp2 at 9 (referring to Netlist1 at 36-43).) For the '623 patent specifically, Respondents urge that the only distinction between the limitation of the '837 patent and the limitation of the '623 patent "is the 'at least one initialization sequence' language compared to the 'one or more training sequences' language." (*Id.* at 10.) Respondents argue this distinction is meaningless for four reasons:

> (1) CALJ Bullock broadly (and correctly) found that the accused ALERT_n signal of the accused products indicates the status of nothing;
>
> (2) CALJ Bullock (correctly) found that there is no material difference between an "initialization" sequence and a "training" sequence;
>
> (3) Netlist itself accused the same functionality of infringing the "initialization" sequence limitation in the 1023 Investigation as it accuses of infringing the "training" sequence limitation in this Investigation; and
>
> (4) even if Netlist did not make the arguments it now makes in the 1023 Investigation, it could have and that is precisely what the doctrine of issue preclusion is designed to prevent.

(*Id.* at 10-11.)

Under the first reason, Respondents reject Netlist's suggestion that "CALJ Bullock found only that the ALERT_n signal does not indicate the status of the Clock-to-CA training mode as a whole." (*Id.* at 11 (referring to Netlist1 at 19-20, 55-56).) In Respondents' view, CALJ Bullock "found that the ALERT_n signal (*i.e.*, accused 'notification signal') does not and cannot indicate 'status' at all" because it consists merely of "feedback signals" which do not become a understandable "status" until after they are received by the memory controller. (*See id.* (citing 1023 ID at 95-96).) Respondents claim "[this] alone should end the matter." (*Id.*)

Under the second reason, Respondents reject the relevancy of Netlist's argument that "initialization sequence" is broader than "training sequence" in such a way as to prevent issue preclusion. (*Id.* at 12.) According to Respondents, the 1023 ID's findings on the nature of the ALERT_n signal as not indicating a "status" "render[s] Netlist's argument about the breadth of the terms a distinction without a difference." (*Id.*) Respondents add that Netlist itself "used the terms interchangeably during the 1023 Investigation." (*Id.* at 12-13 (citing Mot., Ex. 31 at 6-7, 17; Mot., Ex. 37 at 83).) Respondents also dispute that they "relied on the distinction between 'training' and 'initialization' to win a non-infringement finding on the '837 patent" because the position referred to was in the context of a different limitation. (*Id.* at 13-14 (referring to where Clock-to-CA Bus training mode counts as an "initialization mode").) Regardless, Respondents contend "any distinction(s) between 'training' and 'initialization' has been fully litigated and decided in Netlist's favor that initialization includes training." (*Id.* at 14 (citing 1023 ID at 91).)

Under the third reason, Respondents challenge Netlist's idea that "a different question must be answered in the 1089 Investigation; namely whether the 'Alert_n' notification signal provides status information related to 'one or more training sequences' (*e.g.*, 'eye-opening')" (*id.* at 15 (referring to Netlist1 at 55)) and "that it did not have a full and fair opportunity to argue whether the 'ALERT_n signal' in the accused products indicate the 'status' of *subparts* (*i.e.*, "eye opening") of the Clock-to-CA Training Mode" (*id.* (referring to Netlist1 at 58). In Respondents' view, Netlist actually "argued (confusingly at times) *both* that the Clock-to-CA Training Mode was the 'at least one initialization sequence' *and* that various subparts of the Clock-to-CA Training Mode were the 'at least one initialization sequence,' including the "eye-opening." (*Id.* at 16 (citing Mot., Ex. 37 at 83 ("the RCD in each Accused Product executes a number of initialization sequences during Clock-to-CA training mode to determine optimal timing parameters, including sequences to determine the timing of the 'eye opening' and 'eye

closing.'), 87-88).) In sum, Respondents contend "Netlist thus argued that the Alert_n signal indicated the status of the *subparts* of the Clock-to-CA Training Mode (*i.e.*, 'eye opening'), and that those subparts were the at least one initialization sequence" (*id.* (citing Mot., Ex. 37 at 88); *see id.* at 18 (citing Mot., Ex. 16 at 31-33 ("By way of analogy, each individual assertion (HIGH or LOW) of the ALERT_n signal functions much like an interim status report provided in the context of a large project. By providing these periodic status reports (*e.g.*, 'we're at the beginning of the eye-opening,' 'we're working our way through the eye-opening,' 'we're at the close of the eye-opening'), the RCD keeps the memory controller apprised of the status of Clock-to-CA Training Mode, throughout the process")))). Respondents conclude "[j]ust as CALJ Bullock rejected Netlist's 'subparts' as the 'initialization sequence' argument, so did the Commission.'" (*Id.* at 18 (citing Mot., Ex. 32 at 1); *see id.* at 17 (citing 1023 ID at 94-96).)

Under the fourth reason, Respondents argue that setting aside whether Netlist argues "eye-opening" was the "initialization sequence," they had every opportunity to do so in the 1023 Investigation. (*Id.* at 18-19.) Respondents claim "[t]he doctrine of issue preclusion forecloses all arguments in support of an issue, not just the ones that were actually made." (*Id.* at 19 (citing *In re Freeman*, 30 F.3d 1459, 1465 (Fed. Cir. 1994)).)

ii. Netlist's Contentions

In its opening opposition, Netlist view Respondents as taking the positions:

> [T]hat "a notification signal indicating at least one status of one or more training sequences" (as claimed in the '623 patent) is the same as "a notification signal indicating at least one status of one or more initialization sequences" (as claimed in U.S. Patent No. 8,489,837 ("the '837 patent") adjudicated in the 1023 Investigation).
>
> . . . .

> [T]hat the ID equates the "training sequences" claimed in the '623 patent with the "initialization sequences" claimed in the '837 patent.

(Netlist1 at 3.) Netlist claims neither is true. (*Id.*) Rather, according to Netlist:

> The ID merely found that the "initialization mode" of the '837 patent "can include" a training sequence. The ID therefore recognized that initialization can include training sequences, but the training sequences are not initialization. Indeed, Respondents themselves relied on the distinction between "training" and "initialization" to win a non-infringement finding on the '837 patent, so Respondents cannot now argue that they are the same

(*Id.* at 3-4.)

For the '623 patent, Netlist adopts the same premature-before-Markman argument discussed with respect to the '907 patent above. (*See id.* at 36.) More specific to the '623 Netlists states flatly that "a notification signal indicating at least one *status of one or more training sequences*" and "a notification signal indicating at least one *status of one or more initialization sequences*" are "materially different" or "plainly different and distinct." (*Id.* at 42, 43 (emphasis in original).) Netlist claims that even though Respondents and Staff "seek to equate these two phrases," "[h]ow Respondents and Staff seek to equate these different claim terms remain to be seen." (*Id.* at 42.)

Netlist then argues that the "actual express claim language" "refutes" any claim that the claims are "materially similar" to what had been asserted in the 1023 Investigation. (*Id.* at 43.) Netlist accuses Respondents of "repeatedly mischaracterize[ing]" the 1023 ID. (*Id.*)

Netlist disputes that the 1023 ID equated "training" and "initialization." (*Id.* at 53.) Rather, according to Netlist, it was only determined that "the initialization mode of independent claim 1 [of the '837 patent] *can include* a training sequence." (*Id.* (citing 1023 ID at 90-91).) In Netlist's view this indicates the 1023 ID "recognized that 'initialization' and 'training' are different for the reason set forth in the patent's specification, which is that initialization can

include one or more training sequences, but the training sequences are not themselves initialization" (*Id.* at 54.) Netlist continues:

> The ID highlighted the material difference in scope between these terms with reference to the accused products by analogizing the training sequences to "the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake," which are component parts of but not themselves the cake (*i.e.*, the initialization sequence). ASMF No. 78 (ID at 96).

(*Id.*) Netlist further disputes the idea that the 1023 "found that the accused products are incapable of providing *any* status whatsoever." (*Id.*) Netlist attributes this argument to a truncation of the findings in the 1023 ID, which, again, only found that the accused signal was not a "status" of an "initialization sequence"—as opposed to a "training sequence" or anything else. (*See id.* at 54-55.)

Netlist then argues the intrinsic evidence defeats an "identify of issues" between the '623 and '837 patent claims. (*See id.* at 55.) Specifically, Netlist offers the following two tables to allegedly show how "a different question must be answered in the 1089 Investigation:"

Inv. No. 337-Ta-1023		
Claims at issue	**Issue Contemplated**	**Initial Determination Findings**
837 Patent, Claim 1: "notification signal to the memory controller indicating at least one status of the at least one initialization sequence"	Whether Alert_n provides status of entire Clock-to-CA training mode?	The accused notification signal (i.e., the 'ALERT_n signal') . . . does not provide the status of the accused initiation sequence (i.e., the 'Clock-to-CA' training mode) to the memory controller as asserted by Complainant. ASMF No. 71 (ID at 96).

Inv. No. 337-TA-1089		
Claims at issue	**Accused Functionality**	**Initial Determination Findings**
623 Patent, Claim 1: "notification signal indicating at least one status of one or more training sequences"	Whether Alert_n provides status of "one or more training sequences" (*e.g.*, "eye-opening")?	[T]he memory controller utilizes information from the memory module by way of the "ALERT_n signal" (i.e., "eye opening" communications). ASMF No. 75 (ID at 95).

(*Id.* at 54-55.) Netlist alludes, again, to the specifications' teaching that the terms have different scope because "an 'initialization sequence' may include 'one or more training sequences;' not that an 'initialization sequence' is 'one or more training sequences.'" (*Id.* at 56.)

Netlist then claims that "a universe" of extrinsic evidence supports the same understanding. (*Id.*) According to Netlist, that "universe" includes *upcoming* testimony from its expert to show "that a person of ordinary skill in the art would readily understand from the '623 patent's disclosure what the terms 'initialization' and 'training' mean and how the terms are different in relative scope." (*Id.*)

Netlist then addresses how the '623 patent is not actually terminally disclaimed to the '837 patent, but is instead disclaimed to the '116 and '218 patents (two patents within the continuation chain). (*Id.* at 57 (internal citation omitted).) Netlist also disputes that any of its prior arguments that a "status" of a "training sequence" is sufficient to satisfy the "status" of an "initialization sequence" results in collateral estoppel because that argument was rejected by the 1023 ID and therefore not essential to the overall determination. (*Id.* at 58 (citing 1023 ID at 95-96).) Netlist argues, to the contrary, "Respondents prevailed in the 1023 Investigation precisely by convincing the CALJ that status of a training sequence alone was different from and not enough to constitute the claimed initialization sequence." (*Id.*) In Netlist's view it is Respondents that are estopped from arguing "that training sequence and initialization sequence are one and the same." (*Id.*)

Finally, Netlist claims that "Respondents' Argument for Issue Preclusion Contradicts the ID's Factual Findings." (*Id.* at 59 (section heading).) Netlist explains:

> Accordingly, even though the 1023 Investigation adjudicated that the "ALERT_n" signal provides position information regarding the eye opening(s) themselves (*i.e.*, the one or more *training sequences*), the ID found non-infringement of the '837 patent on the basis that "the 'Alert_n signal' generated from the memory

> module" does not provide "status information regarding the *initialization sequence*," *i.e.*, the Clock-to-CA or CA Bus training mode.

(*Id.* at 60 (citing 1023 ID at 95).) Thus, according to Netlist:

> The same ID findings support a finding of infringement of the '623 patent because it does not claim the feature that resulted in non-infringement in the 1023 Investigation, *i.e.*, a "*status of one or more initialization sequences.*" The claims of the '623 patent are directed to the ingredients of the cake, *i.e.*, a "status of one or more training sequences."

(*Id.*)

iii. Staff's Contentions

In its opening submission, and as mentioned above, the Staff "supports the motion with respect to a summary determination of non-infringement based on issue preclusion." (Staff1 at 1.) With respect to the '623 patent, the Staff summarizes:

> Here, all of the independent claims of the '623 patent require "*notification signal...indicating at least one status,*" and Complainant is again alleging that the ALERT_n indicates a status of Clock-to-CA training. *Id.* Accordingly, as opposed to re-litigating the issue of whether the information provided by ALERT_n amounts to a "status" as required by the claims, the Staff supports applying issue preclusion to find that "the 'ALERT_n signal' generated from the memory module does not indicate a status of the 'Clock-to-CA' training mode." Accordingly, there is no infringement of the claims of the '623 patent

(*Id.* at 18 (citing 1023 ID at 94-96).) As with the '907 patent, the Staff takes the position that all other elements of issue preclusion are met, leaving only the identity of issues. (*See id.* at 19, 21.)

Regarding identify of issues, the Staff argues flatly "Because the Common Patent Specification Expressly Discloses 'at least one initialization sequence (*e.g.*, comprising one or more training sequence[s]),' There is No Legal Significance to the Differing Claim Language and Issue Preclusion Should Apply to this 'Identical Issue.'" (*Id.* at 21 (section heading).) Staff

claims "[s]lightly different claim language does not preclude finding of a summary determination of non-infringement based on issue preclusion." (*Id.* at 22 (citing *Aspex Eyewear, Inc.*, 713 F.3d at 1381).) The Staff then points out where, in three places, the shared specification explains an initialization sequence may be, for example, on or more training sequences. (*Id.* at 23-24 (citing '623 patent at 6:50-60, 7:6-7, 7:13-14).) The Staff observes that "the Complainant itself relied upon these portions of the specification to argue the '*notification signal*' claim limitation encompasses Clock-to-CA training sequences, even though the claims of the '837 were directed to '*notification signal... of at least one initialization sequences.*'" (*Id.* at 24 (citing 1023 ID at 90-91).) The Staff concludes by asserting that there is no merit to an argument that Netlist did not have a full and fair opportunity to litigate this issue in the 1023 Investigation (*id.* at 25-26) and Netlist "should be precluded from re-litigating whether the same Clock-to-CA eye-opening boundary information from 'ALERT_n' satisfies the 'notification signal indicating at least one ['status' limitation'" (*id.* at 26 (citing *Astoria Fed. Sav. & Loan Assn. v. Solimino*, 501 U.S. 104, 107 (1991)).)

iv. Analysis

With respect to the '623 patent, Respondents and the Staff contend issue preclusion factors (2) through (4) are not in dispute. (*See* Resp1 at 16-17; Staff1 at 19-20.) Netlist's initial opposition appears to dispute factor (3), essentiality to judgment, based on its section heading (*see* Netlist1 at 53 ("Issue Preclusion Does Not Apply To The '623 Patent Because Whether the Accused Products Provide "a Status of One or More Training Sequences" Was Not Essential to the Judgment in the 1023 Investigation")), but the substance of Netlist's opposition is factor (1)—whether or not the issues (*i.e.*, scope of claim terms), are identical. (*See generally id.* at 53-60.)

To begin, below are the findings from the 1023 ID which I find relevant to the pending motion:

> Complainant also asserts that the "Clock-to-CA" training mode of the accused products is an initialization mode.

(1023 ID at 90);

> With respect to whether the "Clock-to-CA" training is an initialization mode, the undersigned finds that it is. Aside from any potential semantic arguments regarding the relationship between "training" and "initialization," the '837 patent expressly indicates that (i) initialization mode "executes at least one initialization sequence" and (ii) "[t]he at least one initialization sequence (*e.g.*, *comprising one or more training sequences*) may be initiated...." (JX-0006 at 5:44-51 (emphasis added); *see also* CRB at 39.)

(*id.* at 90);

> Thus, the '837 patent makes clear that the initialization mode of independent claim 1 can include a training sequence. Given the absence of any evidence that such scope was surrendered during prosecution, the undersigned can find no basis to so restrict the term "initialization mode" now so as to exclude a training sequence. Given (i) that the evidence shows and there being no dispute that the "ALERT_n" pin is an output and (ii) that the term "initialization mode" can include a training sequence, the undersigned finds that the accused products include this feature of independent claim 1.

(*id.* at 90-91);

> Complainant contends that the Register Clock Driver ("RCD") corresponds to the claimed "controller circuit" and asserts that the RCD causes the memory modules to enter the accused initialization mode (*i.e.*, the "Clock-to-CA" training mode).

(*id.* at 91);

> Complainant contends that the RCD includes an "ALERT_n pin" and that during operation the RCD creates an "ALERT_n signal." Based on this operation, Complainant asserts that the RCD corresponds to the claimed "notification circuit." (CIB at 86.) Complainant further contends that this sequence occurs during the accused initialization mode (*i.e.*, the "Clock-to-CA" training mode). (*Id.*) Complainant also asserts that the "ALERT_n signal" provides notification to the memory controller regarding the status

> of the "Clock-to-CA" training mode and that both the memory controller and memory module remain in the initialization mode until signaled otherwise by the "ALERT_n signal." (*Id.* at 86-88.) Complainant supports this contention by pointing to the fact that "ALERT_n signal" of the accused products "indicates to the memory controller (1) when the 'eye opening' has started, (2) when Clock-to-CA training is seeking the ending boundary of the 'eye opening,' and (3) when the ending boundary of the 'eye opening' has been found." (*Id.* at 86-87.)

(*id.* at 93-94);

> The undersigned agrees with Respondents and Staff that the "ALERT_n signal" generated from the memory module does not indicate a status of the "Clock-to-CA" training mode" and, instead, that only the memory controller provides status information regarding the initialization sequence.

(*id.*at 95);

> In doing so, to be sure, the memory controller utilizes information from the memory module by way of the "ALERT_n signal" (*i.e.*, "eye opening" communications). (RX-1587C at Q/A 238-242.) However, that information is not "status" information pertaining to, for example, whether the initialization sequence has been executed, is currently being execute or is completed. (*See* JX-0006 at 6:51-7:3.) Rather, the information provided by the "ALERT_n signal" signal is aggregated data points (*i.e.*, "LOW' or "HIGH") that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence. (RX-1587C at Q/A 238-242.) Put differently, these feedback signals passing through the memory module do not amount to a "status" until the memory controller utilizes them to make a status determination.

(*id.* at 95-96);

> As such, the accused notification signal (*i.e.*, the "ALERT_n signal") generated from the accused notification circuit (*i.e.*, the RCD) does not provide a status of the accused initiation sequence (*i.e.*, the "Clock-to-CA" training mode) to the memory controller as asserted by Complainant.

(*id.* at 96).

In light of the parties' arguments and the above excerpts, I find factors (2) through (4) of the issue preclusion test are met. The claim terms of the '837 patent which are alleged to be "identical" to terms in the '623 patent, "indicating at least one status of the at least one initialization sequence," were actually litigated in the 1023 Investigation and essential to the final judgment. (*See id.* at 90-96.) Additionally, Netlist, as complainant in the 1023 Investigation, had a full and fair opportunity to litigate the meaning and infringement of those claim terms. (*See id.*) Thus, the resolution of factor (1) will be dispositive of Respondents' motion. As noted above, "[i]f the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity [or infringement], collateral estoppel applies." *Ohio Willow Wood*, 735 F.3d at 1342.

As explained below, I find no material difference between indicating a status of an initialization sequence from the '837 patent and indicating a status of a training sequence from the '623 patent. The 1023 ID already described any alleged difference between the two as "semantic." (1023 ID at 90.) Again, I simply do not see what is left for me to decide given that the Commission has determined with finality that the accused products do not include "notification signals" that indicate the "status" of an "initialization sequence." Nevertheless, I present the relevant claim terms side-by-side in the following table.

'837 Patent	**'623 Patent**
Claim 1 at least one notification signal . . . indicating at least one status of the at least one initialization sequence	*Claim 1* a notification signal indicating at least one status of one or more training sequences
	Claim 12 a notification signal . . . indicating a status of the one or more training sequences;
	Claim 21 a notification signal indicating a status of one or more training sequences

As shown in the table, the '837 patent claims[4] and '623 patent claims both require the exact same "notification signal" which "indicat[es] a status" or "at least one status" of some kind of sequence, either "initialization" or "training." It is undisputed that infringement of the '837 patent turned on its term and I find all the terms present a sufficiently identical issue for several reasons.

First, the Federal Circuit has held that "unless otherwise compelled, that the same claim term in the same patent or related patents carries the same construed meaning." *Omega Eng'g. Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003) (citing *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)). Most of the differences in the collective group are whether "a" or "at least one," is used for "notification signal" and "status." (*See* '837 patent at cl. 1; '623 patent at cls. 1, 12, 21.) These are trivial differences which leaves the only potential difference between "initialization sequence" and "training sequence" to defeat Respondents' motion.

[4] Including claim 1 and claims dependent therefrom.

To that point, I find no intrinsic or extrinsic evidence to suggest "initialization sequence" and "training sequence" are meaningfully different. To the contrary, Respondents and the 1023 ID point out that both the '837 and'623 patent specifications explain an "initialization sequence" may be equivalent to a single "training sequence:"

> In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (*e.g.*, comprising one or more training sequences) may be initiated by the system memory controller 14.

('837 patent at 5:46-51; '623 patent at 6:53-58.) In fact, the two specifications rarely mention "training sequences," and when they do, it is limited to that same equivocation:

> Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays.

('837 patent at 3:34-40; '623 patent at 4:37-44);

> a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (*e.g.*, one or more training sequences).

('837 patent at 5:64-67; '623 patent at 7:4-7);

> a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (*e.g.*, one or more training sequences).

('837 patent at 6:4-7; '623 patent at 7:11-14);

> execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10

('837 patent at 7:19-21; '623 patent at 8:26-28); or a high-level system-wide discussion:

> For example, the MCH [(system memory controller)] according to such a scheme may give control to the local memory controller of a memory subsystem (*e.g.*, memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (*e.g.*, memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

('837 patent at 3:12-23; '623 patent at 4:17-26).

For the sake of completeness, the '623 patent has a different Abstract and Summary from the '837 patent specification, but again, no details on "training sequences" are disclosed that could possibly differentiate them from "initialization sequences:"

> generates a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode . . .

('623 patent at Abstract);

> generates a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode . . .

(*id.* at 1:55-57);

> generates a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences . . .

(*id.* at 2:31-34);

> enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences . . .

(*id.* at 3:6-9).

Thus, by all accounts, the specification uses "training sequences" and "initialization sequences" interchangeably. This may be why, for example, the claims of '837 patent

exclusively recite an "initialization sequence" and never a "training sequence;" while the claims of the '623 patent do the opposite, recite a "training sequence" and never an "initialization sequence." (*See* '837 patent at cls. 1-18; '623 patent at cls. 1-29.) In other words, the '623 patent claims swapped out "initialization sequence" for "training sequence." The idea that both patents generally encompass the same invention is further supported by Netlist's terminal disclaimers for every application within the continuation chain. (*Compare* '623 patent at 1:8-19 (priority claim) *with* Netlist1 at 57.)

Next, the 1023 ID coincidentally resolved the "status" infringement issue of the '837 patent in terms that resolve infringement of the '623 patent as well. Specifically, it was determined:

> [T]he '837 patent makes clear that the initialization mode of independent claim 1 can include a training sequence. Given the absence of any evidence that such scope was surrendered during prosecution, the undersigned can find no basis to so restrict the term "initialization mode" now so as to exclude a training sequence. Given (i) that the evidence shows and there being no dispute that the "ALERT_n" pin is an output and (ii) that the term "initialization mode" can include a training sequence, the undersigned finds that the accused products include this feature of independent claim 1.
>
> . . . .
>
> In doing so, to be sure, the memory controller utilizes information from the memory module by way of the "ALERT_n signal" (*i.e.*, "eye opening" communications). (RX-1587C at Q/A 238-242.) However, that information is not "status" information pertaining to, for example, whether the initialization sequence has been executed, is currently being execute or is completed. (*See* JX-0006 at 6:51-7:3.) Rather, the information provided by the "ALERT_n signal" signal is aggregated data points (*i.e.*, "LOW' or "HIGH") that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence. (RX-1587C at Q/A 238-242.) Put differently, these feedback signals passing

> through the memory module do not amount to a "status" until the memory controller utilizes them to make a status determination.

(1023 ID at 90-91 (citations omitted), 95-96.) These passages are a determination that an accused "notification signal" does not transmit the "status" of a training sequence—exactly what the claims of the '623 patent require. ('623 patent at cls. 1, 12, 21.) Logically, if I were to find in this investigation, that the "ALERT_n signal" indicated a "status" in satisfaction of the '623 patent claims, I would be directly contradicting the Commission's determination that "ALERT_n signals" "do not amount to a 'status' until the memory controller utilizes them to make a status determination." (1023 ID at 96.) Hence, I find this circumstance strongly, even compellingly, supports an identity of issues between the '837 patent and '623 patent claim terms.

I cannot conclude there is a meaningful difference between the "status" of an "initialization sequence" and the "status" of a "training sequence" which would affect an infringement analysis. *Ohio Willow Wood*, 735 F.3d at 1343 (holding "block copolymer" gel was not shown to be patentably significant in view of prior obviousness determination for "polymeric" gel); *Soverain Software*, 778 F.3d at 1319-20 ("The additional limitation here—transmitting a hypertext statement over the Internet, rather than over a generic network—does not materially alter the question of the validity of claim 39. . . . Here, too, the routine incorporation of Internet technology in claim 39 does not change the invalidity analysis. The invalidity of the asserted claims of the '314 and '492 patents is established by issue preclusion.").

In Netlist's view, however, a "status" of a "training sequence" is "materially different claim." (Netlist1 at 21.) Netlist's main evidence in support, however, is limited to emphasizing that the "initialization" and "training" are different words:

> As explained above, the '837 Patent requires a "status" of "initialization," whereas the '623 Patent requires a "status" of "training."

(Netlist1 at 55 (emphasis in original); *see also id.* at 21, 54), or repeating the well-explored excerpt where an "initialization sequence" can "compris[e] one or more training sequences:"

> Accordingly, "one or more training sequences" does not define "initialization sequence." Instead, the specification is clear that an "initialization sequence" may include "one or more training sequences;" not that an "initialization sequence" is "one or more training sequences." The terms have different scope.

(*Id.* at 56 (emphasis in original)). I do not find this limited reasoning persuasive in light of three points discussed above or those differing claim terms at issue in *Ohio Willow Wood* ("block copolymer" and "polymeric") and *Soverain Software* ("transmitting a hypertext statement over the Internet, rather than over a generic network").

Moreover, I also do not find Netlist's equivocation of "training sequence" with "eye-opening" so as to explain the purported difference in scope, to be persuasive or even helpful. I refer specifically to those times where Netlist writes:

> Visually, a single "eye opening" (*e.g.*, one or more training sequences) is depicted in the demonstrative below.

(Netlist1 at 21);

> "Eye-Opening" (Accused 'one or more training sequences' of the '623 Patent in 1089 Investigation).

(*id.* at 22 (within Figure));

> The ID highlighted the material difference in scope between these terms with reference to the accused products by analogizing the training sequences to "the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake," which are component parts of but not themselves the cake (*i.e.*, the initialization sequence).

(*id.* at 54);[5]

[5] This is a conspicuous mischaracterization of what CALJ Bullock determined in the 1023 ID. It is not the "training sequences" which were analogized to the ingredients of a cake; but rather the ALERT_n signals. (*See* 1023 ID at 96; see also Netlist1 at 59 ("Respondents expert

> To the contrary, a different question must be answered in the 1089 Investigation; namely, whether the "Alert_n" notification signal provides status information related to "one or more training sequences" (*e.g.*, "eye-opening").

(*id.* at 55);

> Whether Alert_n provides status of "one or more training sequences" (*e.g.*, "eye-opening")?

(*id.* at 56 (within Table));

> Respondents themselves distinguished a "status of one or more initialization sequences" (the Clock-to-CA training mode itself) form a "status of one or more training sequences" (the one or more "eye openings") to argue non-infringement in the 1023 Investigation.

(*id.* at 59);

> Accordingly, even though the 1023 Investigation adjudicated that the "ALERT_n" signal provides position information regarding the eye opening(s) themselves (*i.e.*, the one or more *training sequences*).

(*id.* at 60 (emphasis in original)). As explained, Netlist has attempted to subtly equate "training sequence" with an "eye-opening." However, neither the specifications nor the claims of either patent mention of eye openings or electrical waveforms, and especially not as any sort of definition for what a "training sequence" is. This is why there are no citations to evidence to support the connection.

Instead, Netlist uses a mischaracterization of the 1023 ID to portray that connection as somehow being already determined. Netlist states:

> The ID highlighted the material difference in scope between these terms with reference to the accused products by analogizing the training sequences to "the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal') of a cake," which are component parts of but not themselves the cake (*i.e.*, the initialization sequence). ASMF No. 78 (ID at 96).

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admitted that the 'ALERT_n' signal provides 'position information' regarding the 'eye opening' (*i.e.*, the ingredients).").)

(Netlist1 at 54.) This reflects a grave misreading of the 1023 ID.

In the 1023 Investigation the accused products were found not to infringe because the feature identified as a "notification signal" (ALERT_n) was not sophisticated enough to be a "status:"

> In doing so, to be sure, the memory controller utilizes information from the memory module by way of the "ALERT_n signal" (*i.e.*, "eye opening" communications). (RX-1587C at Q/A 238-242.) However, that information is not "status" information pertaining to, for example, whether the initialization sequence has been executed, is currently being execute or is completed. (*See* JX-0006 at 6:51-7:3.) Rather, the information provided by the "ALERT_n signal" signal is aggregated data points (*i.e.*, "LOW' or "HIGH") that are feedback signals that (i) initiate with the memory controller, (ii) merely pass through memory module and (iii) return to the memory controller which then utilizes that information to determine a status of the initialization sequence. (RX-1587C at Q/A 238-242.) Put differently, these feedback signals passing through the memory module do not amount to a "status" until the memory controller utilizes them to make a status determination.

(1023 ID at 95-96.) The baking analogy used by the 1023 ID treats the simple ALERT_n feedback signals as the ingredients, which do not amount to a status (*i.e.*, baked) until received and analyzed by the external system memory controller:

> By way of analogy, placing all of the ingredients (*i.e.*, 'eye opening' communications from the 'ALERT_n signal' of a cake in a shopping bag (*i.e.*, the memory module) at the grocery store does not transform them into a cake; that only occurs when they are blended and transferred into the oven and baked (*i.e.*, the memory controller).

(*Id.* at 96.) Thus, contrary to Netlist's claim, the 1023 ID did not in any way "analogiz[e] the training sequences to 'the ingredients . . . of a cake.'" (Netlist1 at 54.) The ALERT_n feedback signals were the "ingredients."

Similarly incorrect is Netlist's assertion that "Respondents prevailed in the 1023 Investigation precisely by convincing the CALJ that status of a training sequence alone was

different from and not enough to constitute the claimed initialization sequence." (Netlist1 at 58 (citing 1023 ID at 95-96.) If anything, the 1023 ID determined the opposite:

> Given the absence of any evidence that such scope was surrendered during prosecution, the undersigned can find no basis to so restrict the term "initialization mode" now so as to exclude a training sequence.

(1023 ID at 90-91; *see* Resp1 at 14 ("Rather, SK hynix (unsuccessfully) argued that the Clock-to-CA Bus training mode could not be the claimed 'initialization mode.'").)

Rather, Netlist's "eye-openings" are "training sequences" argument is an attempt to shoehorn its theory of infringement into claim interpretation —*i.e.*, take the accused product functionality which was found not to infringe "initialization sequence" in the '837 patent and declare that it is what is meant by "training sequence" in the '623 patent. This is improper. *SmithKline Beecham Corp. v. Apotex Corp.*, 403 F.3d 1331, 1340 (Fed. Cir. 2005) ("For this precise reason, this court has repeatedly stated that a court must construe claims without considering the implications of covering a particular product or process"). The argument, therefore, does nothing to move me away from finding, based on the patent's intrinsic evidence and actual findings contained in the 1023 ID, that "initialization sequence" and "training sequence" are not patentably distinct.

Additionally, as above, Netlist's concern that Respondents' motion is premature before a Markman process has taken place is not persuasive. Markman hearings are not mandatory to any section 337 investigation; and, when the claim terms are nearly identical verbiage, as is the case here, a distinct phase of claim construction briefing and argument is not necessary at all.

Thus, I find it is clear there is no material difference between "indicating at least one status of the at least one initialization sequence" data transmissions ('837 patent at cl. 1) and "indicating at least one status of one or more training sequences" ('623 patent at cl. 1; *see* '623

patent at cls. 12, 21). As the satisfaction of issue preclusion's other factors are met and not in dispute, I GRANT Respondents' motion of summary determination of non-infringement under the '623 patent under issue preclusion.

IV. CONCLUSION

For the reasons above, it is my Initial Determination to GRANT Respondents' Motion for Summary Determination of Non-Infringement. (Motion Docket No. 1089-006.)

This Initial Determination, along with any supporting documentation, is hereby certified to the Commission. Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission unless a party files a petition for review of the Initial Determination pursuant to 19 C.F.R. § 210.43(a), or the Commission, pursuant to 19 C.F.R. § 210.44, orders, on its own motion, a review of the Initial Determination or certain issues herein. The Investigation is hereby terminated in its entirety.

This Initial Determination is being issued as confidential, and a public version will be issued pursuant to Commission Rule 210.5(f). Within seven (7) days of the date of this Initial Determination, the parties shall jointly submit: (1) a proposed public version of this opinion with any proposed redactions bracketed in red; and (2) a written justification for any proposed redactions specifically explaining why the piece of information sought to be redacted is

confidential and why disclosure of the information would be likely to cause substantial harm or likely to have the effect of impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions.[6,7]

SO ORDERED.

Thomas B. Pender
Administrative Law Judge

[6] Under Commission Rules 210.5 and 201.6(a), confidential business information includes:

> information which concerns or relates to the trade secrets, processes, operations, style of works, or apparatus, or to the production, sales, shipments, purchases, transfers, identification of customers, inventories, or amount or source of any income, profits, losses, or expenditures of any person, firm, partnership, corporation, or other organization, or other information of commercial value, the disclosure of which is likely to have the effect of either impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions, or causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained, unless the Commission is required by law to disclose such information.

See 19 C.F.R. § 201.6(a). Thus, to constitute confidential business information the disclosure of the information sought to be designated confidential must ***likely have the effect of*** either: (1) impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions; or (2) ***causing substantial harm*** to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained.

[7] While the parties are required to jointly submit the proposed redactions, there is no requirement that the parties must agree on all the redactions. However, the parties' written justification for any proposed redactions should distinguish between those redactions that are agreed upon and those proposed by the individual parties.

CERTAIN MEMORY MODULES AND COMPONENTS THEREOF

INV. NO. 337-TA-1089

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **PUBLIC INITIAL DETERMINATION Order No. 13** has been served by hand upon the Commission Investigative Attorney, **Monisha Deka, Esq.**, and the following parties as indicated, on

MAY 0 1 2018

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U.S. International Trade Commission
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Washington, DC 20436

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