

In the Matter of

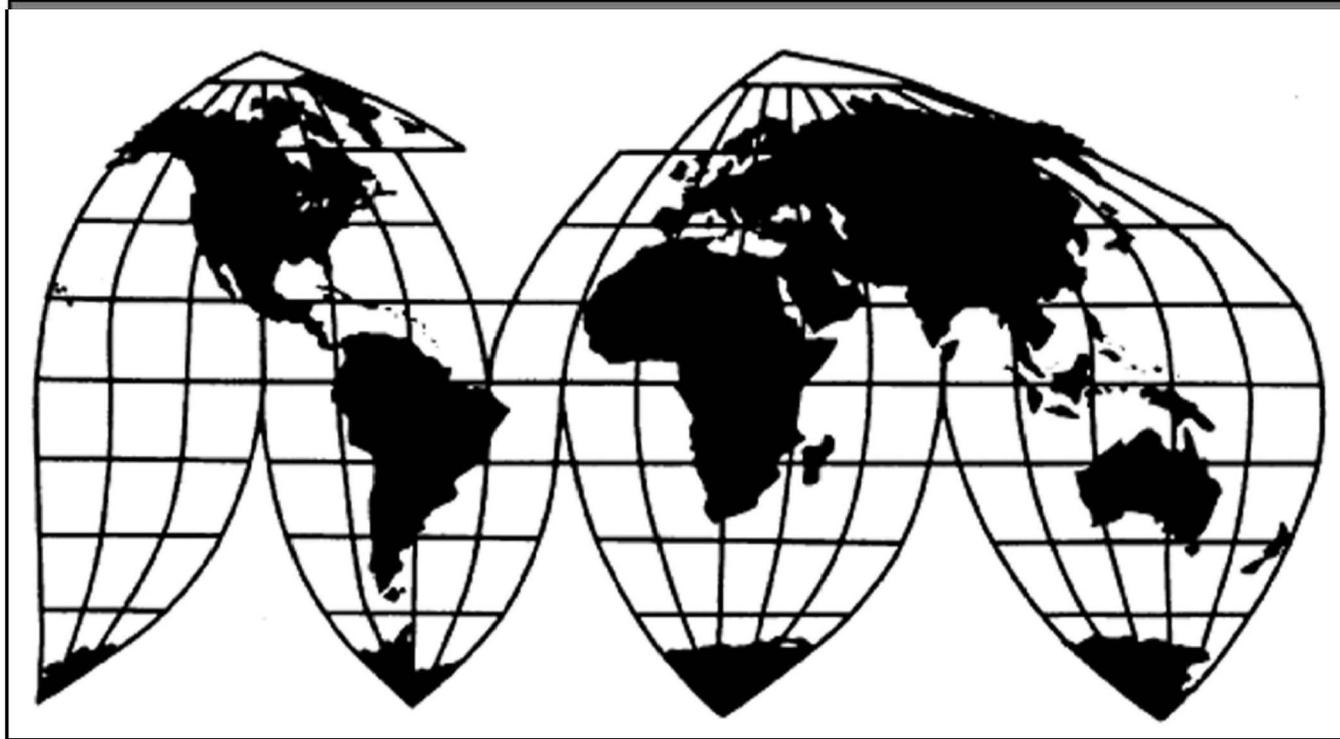
**CERTAIN INTEGRATED CIRCUITS AND
PRODUCTS CONTAINING THE SAME**

Investigation No. 337-TA-1148

Publication 5287

March 2022

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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Investigation No. 337-TA-1148



UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

**CERTAIN INTEGRATED CIRCUITS
AND PRODUCTS CONTAINING THE
SAME**

Investigation No. 337-TA-1148

**NOTICE OF A COMMISSION DETERMINATION TO REVIEW IN PART A
FINAL INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337
AND, ON REVIEW, TO AFFIRM THE FINDING OF NO VIOLATION;
TERMINATION OF THE INVESTIGATION**

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review in part the final initial determination (“ID”) issued by the presiding administrative law judge (“ALJ”) on May 22, 2020, finding no violation of section 337 in the above-referenced investigation and, on review, to affirm the finding of no violation. The investigation is terminated.

FOR FURTHER INFORMATION CONTACT: Michael Liberman, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW, Washington, D.C. 20436, telephone (202) 205-2392. Copies of non-confidential documents filed in connection with this investigation may be viewed on the Commission’s electronic docket (EDIS) at <https://edis.usitc.gov>. For help accessing EDIS, please email EDIS3Help@usitc.gov. General information concerning the Commission may also be obtained by accessing its Internet server at <https://www.usitc.gov>. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission’s TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: On March 15, 2019, the Commission instituted Inv. No. 337-TA-1148, *Certain Integrated Circuits and Products Containing the Same* under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337 (“section 337”), based on a complaint filed by Tela Innovations, Inc. of Los Gatos, California (“Tela”). 84 FR 9558-59 (Mar. 15, 2019). The complaint alleges a violation of section 337 by reason of infringement of certain claims of U.S. Patent Nos. 7,943,966 (“the ’966 patent”); 7,948,012 (“the ’012 patent”); 10,141,334 (“the ’334 patent”); 10,141,335 (“the ’335 patent”); and 10,186,523 (“the ’523 patent”). The complainant also alleges the existence of a domestic industry. The notice of investigation names as respondents Acer, Inc. of New Taipei City, Taiwan; Acer America

Corporation of San Jose, California; AsusTek Computer Inc. of Taipai, Taiwan; Asus Computer International of Fremont, California; Intel Corporation of Santa Clara, California; Lenovo Group Ltd. of Beijing, China; Lenovo (United States) Inc. of Morrisville, North Carolina; Micro-Star International Co., Ltd. of New Taipei City, Taiwan; and MSI Computer Corp. of City of Industry, California (collectively, “Respondents”). *Id.* at 9559. The Commission’s Office of Unfair Import Investigations (“OUII”) is also named as a party in this investigation. *Id.*

The Commission has previously terminated the investigation as to the ’966, ’012 and ’335 patents, and as to certain claims of the ’334 and ’523 patents. *See* Order No. 33 (Oct. 2, 2019), *unreviewed by* Notice (Oct. 22, 2019); Order No. 36 (Oct. 23, 2019), *unreviewed by* Notice (Nov. 15, 2019); and Order No. 44 (Jan. 6, 2020), *unreviewed by* Notice (Feb. 3, 2020).

On May 22, 2020, the ALJ issued his “Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond” (“ID/RD”) finding that there is no violation of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits and products containing the same, in connection with the asserted claims of the ’334 and ’523 patents, and that a domestic industry in the United States that practices or exploits the asserted patents does not exist.

The ID finds that Respondents directly infringe claims 1, 2, and 5 of the ’334 patent, and that claims 1, 2, 5, and 15 of the ’334 patent have been shown to be invalid. The ID also finds that Tela’s licensee has not been shown to practice any claims of the ’334 patent, and that the domestic industry requirement is not satisfied with respect to the ’334 patent. The ID finds that there is no violation of section 337 with respect to the ’334 patent.

The ID further finds that Respondents directly infringe claims 1-11, 14-20, 25, and 26 of the ’523 patent, and that no claims of the ’523 patent have been shown to be invalid. The ID also finds that Tela’s licensee has not been shown to practice any claims of the ’523 patent, and that the domestic industry requirement is not satisfied with respect to the ’523 patent. The ID finds that there is no violation of Section 337 with respect to the ’523 patent.

All the parties to the investigation filed petitions for review of various portions of the ID. On June 8, 2020, OUII filed a petition seeking review of the ID’s determination not to analyze whether the asserted domestic industry claims are invalid and, contingently, seeking review of the ID’s infringement findings. Also on June 8, 2020, Respondents filed a petition contingently seeking review of the ID’s infringement and validity findings.

On June 11, 2020, Tela filed a petition seeking review of the ID’s findings concerning the validity and the technical prong of the domestic industry requirement. Tela also seeks contingent review of the ID’s infringement findings and the ID’s finding that Intel’s 45 nm process is prior art under 35 U.S.C. 102(g)(2). In addition, Tela seeks review of Order No. 30 (Sept. 4, 2019), which granted-in-part Tela’s motion for leave to supplement its contention interrogatory responses.

On June 18, 2020, the parties filed responses to the various petitions.

Having examined the record in this investigation, including the final ID, the petitions for review, and the responses thereto, the Commission has determined to review the ID in part to correct a legal error in the ID's domestic industry findings. On review, the Commission has determined to strike the paragraph relating to the '334 patent on pages 101-102 of the ID and certain sentences relating to the '523 patent on page 168 of the ID. The Commission takes no position on the issue of whether the asserted domestic industry claims, *i.e.*, claims 29-30 of the '334 patent and claims 27-28 of the '523 patent, are invalid. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).

The Commission has also determined to review the ID in part on the issue of whether Tela satisfied the economic prong of the domestic industry requirement, *see* ID at 185-188, and to take no position on this issue. *See Beloit*, 742 F.2d at 1423.

The Commission has determined not to review the remainder of the ID, including the ID's finding of no violation of section 337 in this investigation. The Commission has also determined not to review Order No. 30.

The investigation is terminated.

The Commission vote for this determination took place on September 23, 2020.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337, and in Part 210 of the Commission's Rules of Practice and Procedure, 19 CFR part 210.

By order of the Commission.



Lisa R. Barton
Secretary to the Commission

Issued: September 23, 2020

CONFIDENTIAL CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served via EDIS upon the Commission Investigative Attorney, **John Shin, Esq.**, and the following parties as indicated, on 9/23/2020.



Lisa R. Barton, Secretary
U.S. International Trade Commission
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**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

In the Matter of

**CERTAIN INTEGRATED CIRCUITS
AND PRODUCTS CONTAINING THE
SAME**

Investigation No. 337-TA-1148

COMMISSION OPINION

The Commission has determined that there has been no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 (“section 337”) in this investigation with respect to U.S. Patent Nos. 7,943,966 (“the ’966 patent”); 7,948,012 (“the ’012 patent”); 10,141,335 (“the ’335 patent”); 10,186,523 (“the ’523 patent”); and 10,141,334 (“the ’334 patent”) (collectively, “the Asserted Patents”). This opinion sets forth the Commission’s reasoning in support of the Commission’s determination. In addition, the Commission adopts the findings in the ID that are not inconsistent with this opinion.

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation under section 337 on March 15, 2019, based on a complaint filed by Tela Innovations, Inc. of Los Gatos, California (“Tela”). 84 *Fed. Reg.* 9558-59 (Mar. 15, 2019). The complaint alleges a violation of section 337 by reason of infringement of certain claims of the ’966 patent, the ’012 patent, the ’335 patent, the ’523 patent, and the ’334 patent. The notice of investigation names as respondents Acer, Inc. of New Taipei City, Taiwan; Acer America Corporation of San Jose, California (together, “Acer”); AsusTek

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Computer Inc. of Taipai, Taiwan; Asus Computer International of Fremont, California (together, “Asus”); Intel Corporation of Santa Clara, California (“Intel”); Lenovo Group Ltd. of Beijing, China; Lenovo (United States) Inc. of Morrisville, North Carolina (together, “Lenovo”); Micro-Star International Co., Ltd. of New Taipei City, Taiwan; and MSI Computer Corp. of City of Industry, California (together, “MSI”), (all respondents collectively, “Respondents”). *Id.* at 9559. The Commission’s Office of Unfair Import Investigations is also named as a party in this investigation. *Id.*

The Commission subsequently terminated the investigation as to all asserted claims of the ’966, ’012, and ’335 patents, as well as to certain claims of the ’334 patent and the ’523 patent. *See* Order No. 33 (Oct. 2, 2019), *unreviewed by* Notice (Oct. 22, 2019); Order No. 36 (Oct. 23, 2019), *unreviewed by* Notice (Nov. 15, 2019); Order No. 45, *unreviewed by* Notice (Feb. 3, 2020). At the hearing, Tela asserted claims 1, 2, 5, and 15 of the ’334 patent and claims 1-11, 14-20, 25, and 26 of the ’523 patent against the accused products. For the technical prong of the domestic industry requirement, Tela argued that the domestic industry products practiced claims 29-30 of the ’334 patent and claims 27-28 of the ’523 patent. *ID* at 5.

On July 17, 2019, the ALJ held a *Markman* hearing and, on October 2, 2019, issued Order No. 34 (“the *Markman* Order”), construing certain claim terms of the patents at issue. Order No. 34 (July 17, 2019).

On August 19, 2019, complainant Tela moved for leave to supplement its contention interrogatory responses concerning infringement, domestic industry, and the public interest. On August 28, 2019, Respondents and the Commission’s investigative attorney (“the IA”) filed responses opposing the motion in part. On September 4, 2019, the ALJ issued Order No. 30,

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which partly granted and partly denied Tela’s motion. Order No. 30 (Sep. 4, 2019).¹

The evidentiary hearing took place on December 9-13, 2019. On May 22, 2020, the ALJ issued the final ID finding that there is no violation of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits and products containing the same, in connection with the remaining asserted claims of the ’334 and ’523 patents. ID at 204. In particular, the ID finds no domestic industry with respect to either patent. The ID’s findings are summarized in the following table:

Asserted Patent	ID’s Infringement Findings Per Claim	ID’s Domestic Industry Findings Per Claim	ID’s Validity Findings Per Claim
The ’334 patent	1, 2, 5 – directly infringed 15 – not infringed	29, 30 – not practiced	1, 2, 5, 15 – shown to be invalid 29, 30 – the validity is not addressed ²
The ’523 patent	1-11, 14-20, 25, 26 – directly infringed	27, 28 – not practiced	1-11, 14-20, 25, 26 – not shown to be invalid 27, 28 – the validity is not addressed ³

See ID at 5, 101, 168, 188.

Tela filed a petition for review of various portions of the ID and Order No. 30.⁴ The IA

¹ For a detailed procedural history, see ID at 1-3.

² See discussion *infra* at III.

³ See discussion *infra* at III.

⁴ See Complainant Tela Innovations, Inc’s Corrected Petition and Contingent Petition for Review (June 11, 2020) (“ComplPet”).

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likewise filed a petition for review of the ID in part.⁵ Respondents filed a contingent petition for review.⁶ The parties also filed responses to the various petitions.⁷

B. Semiconductor Chip Technology and the Asserted Patents

The technology at issue relates to the design and manufacture of semiconductor chips with lithographic and epitaxial processes. ID at 5, 68. A semiconductor is a material that has electrical conductivity properties falling between that of a conductor and an insulator. ID at 5-6 (citing Joint Technology Tutorial (“JTT”) at 2). The relevant transistor in the present investigation is a complementary metal oxide semiconductor, or CMOS. *Id.* (citing JTT at 11, 14). A CMOS transistor consists of four basic components: (1) a body; (2) a source region made of one type of semiconductor; (3) a drain region also made of that type of semiconductor; and (4) a gate made of metal and an oxide, where the gate oxide functions as an insulator by separating the gate metal from the other components. *Id.* (citing JTT at 10-14). The circuitry on a CMOS chip is formed through a multi-stage process, including layout, in which the size, shape, and spacing of the chip’s features are specified, followed by photolithography. *Id.* at 6-7 (citing JTT at 17, 19; Respondents’ Initial Claim Construction Brief, Ex. 6 at 6.). Further processing can then be used to build features on the wafer. The parties’ experts provided lengthy overviews of the technology.

⁵ See Petition of the Office of Unfair Import Investigations for Review-in-Part of the Initial Determination on Violation of Section 337 (June 8, 2020) (“IAPet”).

⁶ See Respondents’ Contingent Petition for Review of The Initial Determination (June 8, 2020) (“RespPet”).

⁷ See Complainant Tela Innovations, Inc.’s Response to Respondents’ and Staff’s Petitions for Review of The Initial Determination (June 18, 2020) (“ComplResp”); Response of The Office of Unfair Import Investigations to The Private Parties’ Petitions for Review of The Final Initial Determination On Violation Of Section 337 (June 18, 2020) (“IAResp”); Respondents’ Opposition to Complainant’s Petition for Review of The Initial Determination (June 18, 2020) (“RespResp”).

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See generally CX-1144C (Foty WS) at Q/A 46-135; RX-14C (Subramanian WS) at Q/A 15-69.

The '334 patent is entitled “Semiconductor Chip Including Region Having Rectangular-Shaped Gate Structures and First-Metal Structures.” '334 patent. The '334 patent issued on November 27, 2018. *Id.*

The '523 patent is entitled “Semiconductor Chip Having Region Including Gate Electrode Features Formed in Part From Rectangular Layout Shapes on Gate Horizontal Grid and First-Metal Structures Formed in Part From Rectangular Layout Shapes on at Least Eight First-Metal Gridlines of First-Metal Vertical Grid.” '523 patent. The application leading to the '523 patent was filed on August 31, 2018, and claims priority, through a series of intervening continuation applications, to a provisional application, 60/781,288, filed on March 9, 2006. *Id.* The '523 patent issued on January 22, 2019.

The remaining Asserted Patents both relate to the design and manufacture of integrated circuits forming semiconductor chips. The '334 patent focuses on the shape and fabrication of “structures” on the resulting chip, *see, e.g.*, '334 patent at claim 1, while the '523 patent focuses on the “layout shapes” used as an input to a lithography process during fabrication of the chip, *see, e.g.*, '523 patent at claim 1. These patents aim to address the manufacturing problems created by the “lithographic gap,” which is the “difference between the minimum feature size and the wavelength of light used in the photolithography process.” '523 patent at 4:11-13.

C. Accused Products

The accused products in this investigation are integrated circuits – central processing units (“CPUs”) and chipsets – fabricated with respondent Intel’s 14 nm and 10 nm manufacturing

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processes,⁸ and desktops, laptops, motherboards, and other computers manufactured and sold by respondents Acer, Asus, Lenovo, and MSI⁹ containing those integrated circuits. ID at 10 (citing CIB at 8-9). The ID notes that the individual part and model numbers are too numerous to be reproduced in the ID but are listed in demonstratives to Tela’s expert’s testimony and attached to the ID as Appendix A. *Id.* (citing CX-1144C at Q/A 7- 11; CDX-0003; CDX-0004; CDX-0005; CDX-0006; CDX-0007). All of the products listed in these demonstratives are referred to as the “Accused Products.” The 14 nm products listed in CDX-0003 from respondent Intel will be referred to as the “Intel 14 nm Products,” and the 10 nm products will be referred to as the “Intel 10 nm Products.” *See id.*

The ID further notes that Tela’s expert, Dr. Foty, and Respondents’ expert, Dr. Subramanian, have provided demonstratives associating subsets of the Intel 14 nm Products and Intel 10 nm Products with certain “cells”¹⁰ used in Tela’s infringement case. *Id.* These subsets, along with their associated cells, are listed below:

Intel 14 nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Broadwell;	[[]]
Sky Lake;	[[]]

⁸ The 14 nm and 10 nm manufacturing processes refer to the processes of making integrated circuits with certain characteristics, referred to as 14 nm and 10 nm products, respectively. *See* CX-1144C (Foty) at Q/A 7-11, 190, 606-614, 1881-1887, 1891-1892, 2358, 2401.

⁹ *See supra* at I.A.

¹⁰ “Typically the layout of an integrated circuit is constructed from smaller layout blocks called cells, which correspond to the layout of a particular function. An example of a cell is a flip-flop, which is a common element in an integrated circuit for storing data.” CX-1144 (Foty) at Q/A 107.

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Intel 14 nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Kaby Lake; Coffee Lake	[[]]
Cascade Lake	[[]]
Goldmont; Goldmont Plus	[[]] [[]] [[]]
Ice Lake Chipset; Cannon Lake Chipset	[[]]

Intel 10 nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Ice Lake; Cannon Lake	[[]] [[]] [[]]

ID at 10-11 (citing CDX-0012C at *25-26; RDX-0016C at *37-39).

D. Domestic Industry (“DI”) Products

The domestic industry products in this investigation are integrated circuits, more specifically, 14 nm Exynos computer processors, made for mobile devices. ID at 8 (citing CIB at 9). Tela’s licensee, Samsung Austin Semiconductor (“SAS”), performs front-end wafer fabrication in Austin, Texas. *Id.*; ComplPet at 30-32. Tela explains that these 14 nm Exynos processors are “fabricated using a version of Samsung’s¹¹ 14 nm process technology –

¹¹ Hereinafter, “Samsung” stands for Samsung Electronics Co., Ltd. ID at 177.

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LN14LPEM (14LPE), LN14LPPM (14LPP), or LN14LPCM (14LPC).” ID at 8 (citing CIB at 10 (citing CX-1144C at Q/A 1618-1622, 2692-1693; CX-0033C at 9; CX-1228C at 52:12-54:7)).

The particular processors made by each of these processes and relied on by Tela to satisfy the technical prong of the domestic industry requirement, are listed below:

Tela’s “DI Products”			
Code Name	Fab Part ID	Brand Name	Process Technology
[[]]	S5E7420	Exynos 7 Octa (7420) Mobile Processor	14LPE
[[]]	S5E8890	Exynos 8 Octa (8890) Mobile Processor	14LPP
[[]]	S5E8890	Exynos 8 Octa (8890) Mobile Processor	14LPP
[[]]	S5E7880	Exynos 7880 Mobile Processor	14LPP
[[]]	S5E7570	Exynos 7 Quad (7570) Mobile Processor	14LPC
[[]]	S5E7870	Exynos 7 Octa (7870) Mobile Processor	14LPC
[[]]	S5E7883	Exynos 7883 Mobile Processor	14LPC

Id. at 9 (citing CIB at 10) (internal citations omitted). These processors are referred together as the “DI Products.”¹²

¹² In Order No. 30, the ALJ denied Tela’s belated request to supplement its contention interrogatory responses; Tela had sought to add five Qualcomm processors to the DI Products. *See* Order No. 30 at 1-2. Tela now urges the Commission to reverse Order No. 30 and to consider the Qualcomm processors in its technical and economic prong analyses. *See generally* ComplPet at 46-60. The Commission declines Tela’s request because Order No. 30 reflects a reasonable exercise of judicial discretion. Further, Order No. 30 appropriately considers the moving party’s diligence and the prejudice to the non-moving party, which comports with similar orders. *See, e.g., Certain Semiconductor Devices, Semiconductor Device Packages, and Products Containing Same*, Inv. No. 337-TA-1010, Order No. 58 at 3 (Jan. 17, 2017) (assessing the complainant’s diligence and the prejudice to the respondent); *Certain Microelectromechanical Systems (“MEMS Devices”) and Products Containing the Same*, Inv. No. 337-TA-876, Order No. 49 at 2 (Dec. 13, 2013) (finding that the respondent’s lack of diligence undermined its ability to show good cause

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Tela’s evidentiary presentation regarding the economic prong of the domestic industry requirement and discussion of the relied upon investments is based on a separate, three-tiered classification of the DI Products, to accommodate situations in which less than all of them satisfy technical prong. *Id.* The tiers are as follows:

Tela’s Economic Prong Groups	
Group 1	[[]] (7420)
Group 2	Group 1 + [[]] (8890), [[]] (8890), [[]] (7880)
Group 3	Group 1 + Group 2 + [[]] (7570) + [[]] (7870) + [[]] (7883)

Id. (citing CIB at 160; RIB at 172-173).

II. STANDARD ON REVIEW

Under Commission Rule 210.43, the Commission will review an ID where it appears that –

- (1) a finding or conclusion of material fact is clearly erroneous;
- (2) a legal conclusion is erroneous, without governing precedent, rule or law, or constitutes an abuse of discretion; or
- (3) the determination is one affecting Commission policy.

19 C.F.R. § 210.43.

The Commission may review an ID on the basis of a petition for review or on its own initiative. 19 C.F.R. §§ 210.43, 210.44. The party seeking review is required to specify the issues for which review is sought. Any issue that is not raised in the petition is deemed to have been abandoned and may be disregarded by the Commission, unless the Commission determines to

for supplementing an interrogatory response). Accordingly, the Commission has not included the Qualcomm processors in the DI products.

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review the issue on its own initiative. Commission review will encompass those issues for which at least one participating Commissioner votes to review. *Id.*

Commission review of an initial determination is limited to the issues set forth in the notice of review and all subsidiary issues therein. *Certain Bar Clamps, Bar Clamp Pads, and Related Packaging Display and Other Materials*, Inv. No. 337-TA-429, Comm'n Op. at 3 (Jan. 4, 2001). Once the Commission determines to review an initial determination, its review is *de novo*. *Certain Polyethylene Terephthalate Yarn and Products Containing Same*, Inv. No. 337-TA-457, Comm'n Op. at 9 (Jun. 18, 2002). Upon review the "Commission has 'all the powers which it would have in making the initial determination,' except where the issues are limited on notice or by rule." *Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, Comm'n Op. on the Issues Under Review and on Remedy, the Public Interest, and Bonding at 9-10 (Jun. 2, 1997), USITC Pub. 3046 (July 1997) (quoting *Certain Acid-Washed Denim Garments and Accessories*, Inv. No. 337-TA-324, Comm'n Op. at 5 (Nov. 1992)).

On review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge. In addition, the Commission may take no position on specific issues or portions of the initial determination of the administrative law judge. The Commission may also make any findings or conclusions that in its judgment are proper based on the record in the proceeding." 19 C.F.R. § 210.45.

III. ANALYSIS

While analyzing invalidity and other defenses raised by Respondents, the ID declines to analyze respondents' arguments concerning the invalidity of the asserted domestic industry

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claims.¹³ See ID at 101, 168. The IA sought review of the ID in part, arguing that the ID’s decision not to analyze whether the asserted DI claims are invalid is a legal error. IAPet at 17. The Commission has determined to review the ID in part on this issue.

The ID states:

Before turning to the[] merits [of various invalidity and unenforceability theories for the 334 patent], however, a few preliminary points are warranted. Two of the disputed claims, 29 and 30, are pertinent only to the technical prong of domestic industry. See RIB at 74-75; SIB at 83-84. In general, however, it is “Commission practice not to couple an analysis of domestic industry to a validity analysis.” *Certain Soft-Edged Trampolines and Components Thereof*, Inv. No. 337-TA-908, Comm’n Op. at 53 (May 1, 2015). Indefiniteness is the only basis for invalidity that bears on whether the technical prong is met, because indefiniteness “ma[kes] it impossible for the complainant to demonstrate whether a patent claim [is] practiced.” *Certain Silicon Microphone Packages and Products Containing the Same*, Inv. No. 337-TA-695, Notice at 3 (Jan. 21, 2011). But indefiniteness is not one of the asserted grounds of invalidity of these two claims. See RIB at 74-75; SIB at 83-84. Therefore, whether claims 29 and 30 of the 334 patent are invalid is not relevant, and the parties’ dispute over these claims need not be resolved or otherwise addressed.

ID at 101-102. See also *id.* at 168 (“Claim 27 [of the ’523 patent] is pertinent only to the technical prong of domestic industry. See RIB at 148; SIB at 83-84. Thus, because indefiniteness is not an asserted ground of invalidity of claim 27, the parties’ dispute over that claim need not be resolved or otherwise addressed.”) (citing *Silicon Microphone Packages*, Inv. No. 337-TA-695, Notice at 3).

We find that the ID’s determination that the parties’ dispute over validity of the asserted DI claims “need not be resolved or otherwise addressed” is legally erroneous. See ID at 102. While the ID correctly notes that it is “Commission practice not to couple an analysis of domestic industry to a validity analysis,” ID at 101, this statement, correctly interpreted, indicates that a

¹³ As noted previously, the asserted DI claims are: claims 29-30 of the ‘334 patent and claims 27-28 of the ’523 patent.

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technical prong analysis and a validity analysis coexist and one does not affect, or preclude, the other.

Commission precedent supports this interpretation. Where the technical prong is *otherwise* met because the DI claims read on the DI products, but the DI claims are invalid, there can be no violation because the domestic industry articles are not protected by the patent. *See* 19 U.S.C. § 1337(a)(2) (the DI articles must be “protected by the patent”). Thus, as the IA correctly points out, “the *Trampolines* line of cases merely clarifies that even if a domestic industry claim is invalid, such an invalidity finding does not preclude a finding that the complainant’s domestic industry article has otherwise met the technical prong of the domestic industry requirement[.]” *i.e.*, by finding that the asserted DI products meet the limitations of the relevant claims. IAPet at 19.¹⁴ In short, the question of whether the DI claims are valid is a separate question argued by the parties that the ID should have addressed.

We therefore strike the paragraph quoted above, *see* ID at 101-102, and the following sentences relating to the ’523 patent:

Claim 27 is pertinent only to the technical prong of domestic industry. *See* RIB at 148; SIB at 83-84. Thus, because indefiniteness is not an asserted ground of invalidity of claim 27, the parties’ dispute over that claim need not be

¹⁴ The IA’s petition cites, *inter alia*, *Certain Silicon Microphone Packages and Products Containing the Same*, Inv. No. 337-TA-695, USITC Pub. No. 4293, Notice at 3 (Jan. 21, 2011) (“The Commission has determined to review and vacate the ID’s conclusion that the technical prong of the domestic industry requirement, 19 U.S.C. § 1337(a)(2) & (a)(3), is not met where all the asserted patent claims are found invalid. It is Commission practice not to couple an analysis of domestic industry to a validity analysis.”) (citation omitted); and *Certain Infotainment Systems, Components Thereof, and Automobiles Containing the Same*, Inv. No. 337-TA-1119, Comm. Op. at 27-44 (April 30, 2020)). *See* IAPet at 19-20. *See also* *Certain Microlithographic Machines and Components Thereof*, Inv. 337-TA-468, Initial Determination at 68, 447 (Jan. 29, 2003) (finding that the technical prong of the domestic industry requirement is satisfied with respect to the claims that were found to be invalid), *unreviewed by* Notice (March 17, 2003).

PUBLIC VERSION

resolved or otherwise addressed. *Silicon Microphone Packages*, Inv. No. 337-TA-695, Notice at 3.

ID at 168.¹⁵

We note Tela’s assertion that “[d]espite requesting that the Commission review the ID’s determinations regarding obviousness of the ’523 DI claims, the Staff did not assert obviousness as to any DI claim before the ALJ. (ID at 168; SIB at 113-14.) Staff thus waived any arguments that the DI claims of the ’523 Patent are obvious.” ComplResp at 46. Tela’s assertion, however, does not warrant a finding of waiver. The IA petitions for review of the ID’s alleged legal errors unrelated to the merits of the underlying invalidity contentions regarding the DI claims, and, therefore, the IA is permitted to petition for review of the question of whether the ID made a legal error in its analysis to conclude that the parties’ invalidity dispute need not be addressed. *See* IAPet at 21; *accord Myco Industries, Inc. v. BlephEx, LLC*, 955 F.3d 1, 11 n.4 (Fed. Cir. 2020) (“While a party can waive his or her ability to appeal a ruling for failure to object, there can be no waiver here of the Judge’s duty to apply the correct legal standard.”) (quotations omitted); *GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1372 (Fed. Cir. 2016) (“In general, ‘litigants waive their right to present new claim construction disputes if they are raised for the first time after trial.’ . . . [T]his is not what happened here.”) (internal citations omitted).

Accordingly, we find that the ID legally erred in concluding that a validity analysis does not need to be performed for claims that pertain only to the technical prong of the domestic

¹⁵ We note that, in addition, the above two sentences appear to contain a clerical error and were likely meant to read as follows: “Claims 27 and 28 are pertinent only to the technical prong of domestic industry. . . . Thus, because indefiniteness is not an asserted ground of invalidity of claims 27 and 28, the parties’ dispute over these claims need not be resolved or otherwise addressed.” *See* ID at 168; *see also* IAPet at 18 n. 4. The Commission’s decision to strike the above two sentences, however, renders this issue moot.

PUBLIC VERSION

industry requirement. However, the ID found no violation of section 337 because Tela does not practice the asserted DI claims with respect to either the '334 or '523 patents. *See* ID at 188-89. The Commission has determined not to review the finding concerning the technical prong of the domestic industry requirement. In light of this determination, there is no need for the Commission in this instance to resolve whether the asserted DI claims (*i.e.*, claims 29-30 of the '334 patent and claims 27-28 of the '523 patent) are valid because this issue will not affect the ultimate determination that there is no violation of section 337. Accordingly, the Commission takes no position on the issue of whether claims 29-30 of the '334 patent and claims 27-28 of the '523 patent are valid. *See Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).

The Commission has also determined to review the ID in part on the issue of whether Tela satisfied the economic prong of the domestic industry requirement, *see* ID at 185-188, and to take no position on this issue. *See Beloit*, 742 F.2d at 1423.

IV. CONCLUSION

For the reasons set forth herein, the Commission determines that complainant Tela has not established a violation of section 337 by Respondents with respect to the asserted claims of the '334 and '523 patents. Accordingly, the investigation is terminated with a finding of no violation of section 337.

By order of the Commission.



Lisa R. Barton
Secretary to the Commission

Issued: December 30, 2020

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **OPINION, COMMISSION** has been served via EDIS upon the Commission Investigative Attorney, **John Shin, Esq.**, and the following parties as indicated, on December 30, 2020.



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UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN INTEGRATED CIRCUITS
AND PRODUCTS CONTAINING THE
SAME**

Inv. No. 337-TA-1148

**INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND**

Administrative Law Judge Cameron Elliot

(May 22, 2020)

Pursuant to the Notice of Investigation and Rule 210.42(a) of the Rules of Practice and Procedure of the United States International Trade Commission, this is my Initial Determination in the matter of *Certain Integrated Circuits and Products Containing the Same*, Investigation No. 337-TA-1148.



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TABLE OF ABBREVIATIONS

CDX	Complainant's Demonstrative Exhibit
CIB	Complainant's Revised Initial Post-Hearing Brief
CPB	Complainant's Pre-Hearing Brief
CPX	Complainant's Physical Exhibit
CRB	Complainant's Reply Post-Hearing Brief
CX	Complainant's Exhibit
Dep. Tr.	Deposition Transcript
Hr'g Tr.	Hearing Transcript
JX	Joint Exhibit
RDX	Respondents' Demonstrative Exhibit
RIB	Respondents' Initial Post-Hearing Brief
RPB	Respondents' Pre-Hearing Brief
RPX	Respondents' Physical Exhibit
RRB	Respondents' Reply Post-Hearing Brief
RX	Respondents' Exhibit
SDX	Commission Investigative Staff's Demonstrative Exhibit
SIB	Commission Investigative Staff's Initial Post-Hearing Brief
SPB	Commission Investigative Staff's Pre-Hearing Brief
SPX	Commission Investigative Staff's Physical Exhibit
SRB	Commission Investigative Staff's Reply Post-Hearing Brief
SX	Commission Investigative Staff's Exhibit

I. INTRODUCTION

A. Procedural Background

Complainant Tela Innovations, Inc. (“Tela” or “Complainant”) filed the complaint underlying this Investigation on December 19, 2018, amended the complaint on February 7, 2019, and filed supplements to the amended complaint on February 13, 2019 and February 26, 2019. The amended complaint alleged respondents Acer, Inc., Acer America Corporation, AsusTek Computer Inc., Asus Computer International, Intel Corporation, Lenovo Group Ltd., Lenovo (United States) Inc., Micro-Star International Co., Ltd., and MSI Computer Corp. (altogether, “Respondents”) import or sell in connection with an importation certain products that infringe one or more claims of U.S. Patent Nos. 7,943,966 (“the 966 patent”), 7,948,012 (“the 012 patent”), 10,141,334 (“the 334 patent”), 10,141,335 (“the 335 patent”), and 10,186,523 (“the 523 patent”).

By publication of a notice in the *Federal Register* on March 15, 2019, the U.S. International Trade Commission ordered that:

Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of products identified in paragraph (2) by reason of infringement of one or more of claims 2, 32, and 33 of the '966 patent; claims 2, 27, and 28 of the '012 patent; claims 1, 2, 5, 6, 9, 11, 15, 20, and 24 of the '334 patent; claims 1, 2, 5, 6, 9, 11, 15, 20, and 24 of the '335 patent; and claims 1-12, 14-20, 22-24, and 26 of the '523 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337[.]

43 Fed. Reg. 9559 (Mar. 15, 2019). On April 3, 2019, I set a target date of August 14, 2020 for completion of this investigation via initial determination. Order No. 4. Also on April 3, 2019, I set a *Markman* hearing date of July 8 and July 10, 2019 and the evidentiary hearing for December 9-13, 2019. Order No. 5. On April 11, 2019, at the request of the parties, the *Markman* hearing was moved to July 15 and July 17, 2019. Order No. 6.



On July 17, 2019, I held a technology tutorial and *Markman* hearing, and on October 2, 2019, issued Order No. 34, construing certain claim terms of the patents at issue.

On July 29, 2019, Respondents moved for summary determination of invalidity due to lack of written description and enablement (Motion No. 1148-024) which was denied on August 20, 2019 with Order No. 27.

On September 19, 2019, Tela moved to terminate the investigation with respect to all asserted claims of the 966 and 012 patents (Motion No. 1148-033), which was granted via initial determination on October 2, 2019 with Order No. 33.

On October 8, 2019, Respondents moved for summary determination of invalidity due to indefiniteness (Motion No. 1148-035) based on certain findings made in Order No. 34, but Respondents withdrew the motion on October 22, 2019 in light of Tela's co-pending motion to terminate the pertinent claims and patent from the investigation (Motion No. 1148-037). I granted Tela's motion via initial determination on October 23, 2019 with Order No. 36, which terminated the investigation as to all asserted claims of the 335 patent, claims 6, 11, and 20 of the 334 patent, and claim 12 of the 523 patent.

Also on October 8, 2019, Tela moved for summary determination that it satisfies the economic prong of domestic industry (1148-036). I denied Tela's motion on November 4, 2019 with Order No. 38, but treated certain facts as established under Commission Rule 210.18(e) related to this issue and discussed further below.

The evidentiary hearing took place over December 9-13, 2019. Following the hearing, on January 3, 2020, Tela moved to terminate the investigation in part as to claims 9 and 24 of the 334 patent, and claims 22-24 of the 523 patent (Motion No. 1148-054). I granted Tela's motion via initial determination on January 6, 2020 with Order No. 45. As of the date of this initial

[REDACTED]

determination, no motions are pending, and only the 334 patent and 523 patent remain asserted (hereafter, “the Asserted Patents”).

Pursuant to the procedural schedule, the parties submitted initial and reply post-hearing briefs on January 6, 2020 and January 17, 2020, respectively. Finally, on February 19, 2020, I extended the target date by six weeks via initial determination with Order No. 47 due in part to the volume of contested issues in this investigation.

B. The Parties

Complainant Tela Innovations, Inc. is a United States corporation organized and existing under the laws of Delaware and having its principal place of business in Los Gatos, California. CPB at 7. Tela conducts engineering, research, and design related to integrated circuit design in areas such as performance, area, power consumption, and manufacturability characteristics. *See id.*

Respondent Intel Corporation (“Intel”) is a corporation organized and existing under the laws of Delaware and having its principal place of business in Santa Clara, California. RIB at 5. Intel is a historically significant entity in the semiconductor industry with offices worldwide, developing and selling, among other things, central processing units and other processors for personal and server-level computers. *See generally id.*

Respondent Acer, Inc. is a foreign corporation organized and existing under the laws of Taiwan and having a principal place of business in New Taipei City 221, Taiwan. RIB at 5. Acer, Inc. designs and sells, among other things, personal computers containing Intel processors. *See id.* at 7. Respondent Acer America Corporation is a corporation organized and existing under the laws of California and having a principal place of business in San Jose, California. *Id.* at 5. Acer America Corporation is a subsidiary of Acer, Inc. (together, “Acer”). *Id.*

[REDACTED]

Respondent ASUSTek Computer, Inc. is a foreign corporation organized and existing under the laws of Taiwan and having a principal place of business in Beitou District Taipei 112, Taiwan. RIB at 5. ASUSTek Computer, Inc. designs and sells, among other things, personal computers containing Intel processors. *See id.* at 7. Respondent ASUS Computer International is a corporation organized and existing under the laws of California and having a principal place of business in Fremont, California. *Id.* at 5. ASUS Computer International is a subsidiary of ASUSTek Computer, Inc. (together, “ASUS”). *Id.*

Respondent Lenovo Group Ltd. is a foreign corporation organized and existing under the laws of China and having a principal place of business in Beijing, China. RIB at 6. Lenovo Group Ltd. designs and sells, among other things, personal computers containing Intel processors. *See id.* at 7. Respondent Lenovo (United States) Inc. is a corporation organized and existing under the laws of Delaware and having a principal place of business in Morrisville, North Carolina. *Id.* at 6. Lenovo (United States) Inc. is an “indirect subsidiary” of Lenovo Group Ltd. (together, “Lenovo”). *Id.*

Respondent Micro-Star International Co., Ltd. is a foreign corporation organized and existing under the laws of Taiwan and having a principal place of business in New Taipei City 235, Taiwan. RIB at 6. Micro-Star International Co., Ltd. designs and sells, among other things, personal computers containing Intel processors. *See id.* at 7. Respondent MSI Computer Corp. is a corporation organized and existing under the laws of California and having a principal place of business in City of Industry, California. *Id.* at 6. MSI Computer Corp. is a subsidiary of Micro-Star International Co., Ltd. (together, “MSI”). *Id.*

C. The Asserted Patents and Claims

The Asserted Patents relate to semiconductor chips with gate structures and other feature layers arranged in a grid. The following claims are at issue in this investigation:

Asserted Patent	Infringement Claims	Domestic Industry Claims
10.141,334	1, 2, 5, 15	29, 30
10,186,523	1-11, 14-20, 25, 26	27, 28

See CIB at 11, 66, 101, 135.¹

The 334 patent is entitled, “Semiconductor Chip Including Region having Rectangular-Shaped Gate Structures and First-Metal Structures.” JX-0003 (also cited herein as “334 patent”). The application leading to the 334 patent was filed on August 28, 2017, and claims priority, through a series of intervening continuation applications, to a provisional application, 60/781,288, filed on March 9, 2006. *Id.* The 334 patent issued on November 27, 2018. *Id.*

The 523 patent is entitled, “Semiconductor Chip having Region including Gate Electrode Features Formed in part from Rectangular Layout Shapes on Gate Horizontal Grid and First-Metal Structures Formed in part from Rectangular Layout Shapes on at Least Eight First-Metal Gridlines of First-Metal Vertical Grid.” JX-0005 (also cited herein as “523 patent”). The application leading to the 523 patent was filed on August 31, 2018, and claims priority, through a series of intervening continuation applications, to a provisional application, 60/781,288, filed on March 9, 2006. *Id.* The 523 patent issued on January 22, 2019.

By way of background, a semiconductor is a material that has electrical conductivity properties falling between that of a conductor and an insulator. Joint Technology Tutorial, EDIS

¹ Tela does not identify claim 25 as infringed, but it is implicated by asserted dependent claim 26.

[REDACTED]

Doc. ID 680838 at 2 (“JTT”). These conductive properties may be changed with the addition of impurities. *Id.* at 6. The addition of different types of impurities results in two different types of semiconductor, known as p-type and n-type. *Id.*

P-type and n-type semiconductors can be used with other materials to construct transistors. JTT at 10-13. The relevant transistor here is a complementary metal oxide semiconductor, or CMOS. *Id.* at 11, 14. A CMOS transistor is made of four basic components: (1) a body; (2) a source region made of one type of semiconductor; (3) a drain region also made of that type of semiconductor; and (4) a gate made of metal and an oxide, where the gate oxide functions as an insulator by separating the gate metal from the other components. *Id.* at 10-14. The source region and the drain region together constitute the diffusion region. 523 patent at 9:35-42 (“diffusion regions 203 represent selected regions of the base substrate 201 within which impurities are introduced” and “diffusion contacts 205 are defined to enable connection between source and drain diffusion regions 203”).

When a voltage is applied to the gate an electric field is formed under it, causing a conductive channel connecting the source and drain to either appear or disappear, depending on the voltage and the type of semiconductor used to form the source and drain. JTT at 10-16. As a result, current can be made to either flow or not flow from source to drain, and the transistor in effect acts as an on/off switch. *Id.* at 10, 13. Logic circuits using this switching effect may be formed by connecting many transistors together. *See* JTT at 10. A set of such circuits disposed on a semiconductor substrate is called an integrated circuit, or chip. *Id.* at 2. A silicon wafer is the substrate material for a CMOS chip. *Id.* at 17.

The circuitry on a CMOS chip is formed through a multi-stage process, including layout, in which the size, shape, and spacing of the chip’s features are specified, followed by

[REDACTED]

photolithography. JTT at 17, 19; *see* Respondents’ Initial Claim Construction Brief, EDIS Doc. ID 678284, Ex. 6 at 6 (“A layout represents the size, shape, and spacing guidelines for a given layer in a transistor”). In photolithography, a material called photoresist is deposited on the wafer. JTT at 17. Photoresist undergoes chemical changes when exposed to light. *Id.* at 19. In one embodiment of the photolithography process, a pattern of opaque chrome material is placed on transparent quartz glass to form a photomask corresponding to at least a portion of the layout. *Id.* at 18. The photomask is placed over the wafer, ultraviolet light is shined through it, and the underlying photoresist chemically changes to match the photomask’s pattern. *Id.* Application of a solvent then removes some of the photoresist, leaving the remaining photoresist in either a positive or negative pattern (depending on the photoresist) matching that of the photomask. *Id.* at 18-19.

Further processing can then be used to build features on the wafer; for example, in areas where photoresist has been removed, material may be added by deposition or removed by etching. *See* JTT at 19. Repeated application of photolithography and additional processing results in a “stack of layers” on the wafer. 523 patent at 9:14-15; *see generally* 523 patent at Fig. 2. Within these layers, the various features forming the integrated circuit include gates, gate electrodes, source and drain contacts, and other elements, all of which “enable . . . the desired circuit connectivity.” *Id.* at 9:56-57; *see generally id.* at 9:30-49.

The density of circuitry can be increased by reducing feature size. JTT at 20. Historically, feature size has been shrinking, and in many cases features are smaller than the wavelength of the light used for photolithography. *Id.* Because of the small feature size, interference patterns are generated during fabrication as shapes on the photomask interact with the light. 523 patent at 4:16-

17. These interference patterns cause the fabricated feature shape to deviate from the designed feature shape, so much so that failure may result. *Id.* at 4:22-24.

In particular, when “two-dimensionally varying features are located in neighboring proximity to each other, the light used to expose the features will interact in a complex and generally unpredictable manner,” and may result in, for instance, “layout feature shape distortion.” 523 patent at 7:41-44, 8:25. Although “[c]orrection methodologies” exist to solve this problem, “semiconductor product yield is reduced as a result of . . . two-dimensionally varying features disposed in proximity to each other.” *Id.* at 4:24, 8:17-21. The Asserted Patents claim a new such methodology focused on “topology,” or feature shape. *Id.* at 7:36-37. Specifically, the Asserted Patents themselves assert that “layout feature shape enhancement can be realized if the layout feature shapes are rectangular, near the same size, and are oriented in the same direction.” *Id.* at 9:8-9. It stands undisputed that Tela is the owner of the Asserted Patents. CIB at 155 (citing JX-0008; JX-0010; CX-1148C at Q/A 6-9), 11 (citing JX-0003; JX-0005; JX-0013; JX-0015); *see generally* RIB; SIB.

D. Products at Issue

1. Domestic Industry Products

The domestic industry products in this investigation are integrated circuits; more specifically, 14nm Exynos computer processors, made for mobile devices. CIB at 9. These processors are made by Samsung Austin Semiconductor (“SAS”) in the United States. Tela explains how these 14nm Exynos processors are “fabricated using a version of Samsung’s 14nm process technology—LN14LPEM (14LPE), LN14LPPM (14LPP), or LN14LPCM (14LPC).” *Id.* at 10 (citing CX-1144C at Q/A 1618-1622, 2692-1693; CX-0033C at *9; CX-1228C at 52:12-54:7). The particular processors made by each of these processes, and relied on by Tela for satisfaction of domestic industry, are listed below:



Tela's "DI Products"			
Code Name	Fab Part ID	Brand Name	14nm Process Technology
[REDACTED]	S5E7420	Exynos 7 Octa (7420) Mobile Processor	14LPE
[REDACTED]	S5E8890	Exynos 8 Octa (8890) Mobile Processor	14LPP
[REDACTED]	S5E8890	Exynos 8 Octa (8890) Mobile Processor	14LPP
[REDACTED]	S5E7880	Exynos 7880 Mobile Processor	14LPP
[REDACTED]	S5E7570	Exynos 7 Quad (7570) Mobile Processor	14LPC
[REDACTED]	S5E7870	Exynos 7 Octa (7870) Mobile Processor	14LPC
[REDACTED]	S5E7883	Exynos 7883 Mobile Processor	14LPC

CIB at 10 (citing, *inter alia*, CX-0033C at *9; CX-1145C at Q/A 32-40; CX-1144C at Q/A 2619-2629, 2692-2693); *see* CX-0629; CX-0630; CX-0631; CX-0632; CX-0633; CX-1230. These processors will be referred together in this initial determination as the "DI Products." Further, Tela's presentation of economic prong domestic industry and discussion of significant investment is based on a separate, three-tiered classification of the DI Products, to accommodate situations in which less than all of them satisfy technical prong. The tiers are as follows:

Tela's Economic Prong Groups	
Group 1	[REDACTED] (7420)
Group 2	Group 1 + [REDACTED]
Group 3	Group 1 + Group 2 + [REDACTED]

CIB at 160; *see* RIB at 172-173.



2. Accused Products

The accused products in this investigation are integrated circuits—both CPUs and chipsets—fabricated on respondent Intel’s 14nm and 10nm manufacturing processes, and also desktops, laptops, motherboards, and other computers manufactured and sold by respondents Acer, Asus, Lenovo, and MSI containing those integrated circuits. CIB at 8-9. The individual part and model numbers are too numerous to reproduce here but are listed in demonstratives to Tela’s expert’s testimony and attached to this initial determination as Appendix A. CX-1144C at Q/A 7-11; CDX-0003; CDX-0004; CDX-0005; CDX-0006; CDX-0007. All of the products listed in these demonstratives will be referred to in this initial determination as the “Accused Products”; while the 14nm products listed in CDX-0003 from respondent Intel will be referred to as the “Intel 14nm Products” and the 10nm products will be referred to as the “Intel 10nm Products.”

Further, Tela’s expert, Dr. Foty, and Respondents’ expert, Dr. Subramanian, have provided demonstratives associating subsets of the Intel 14nm Products and Intel 10nm Products with certain “cells” used in Tela’s infringement case. These subsets, along with their associated cells, are listed below:

Intel 14nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Broadwell; Sky Lake; Kaby Lake; Coffee Lake	
Cascade Lake	
Goldmont; Goldmont Plus	



Ice Lake Chipset; Cannon Lake Chipset	
Intel 10nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Ice Lake; Cannon Lake	

See CDX-0012C at *25-26; RDX-0016C at *37-39.

II. STANDARDS OF LAW

A. Standing

Commission Rule 210.12 states in relevant part “[f]or every intellectual property based complaint (regardless of the type of intellectual property involved), [the complaint must] include a showing that at least one complainant is the owner or exclusive licensee of the subject intellectual property.” 19 C.F.R. § 210.12(a)(7). In determining whether this rule is met, the Commission looks to the standing requirement used by courts in patent infringement cases. *Certain Audio Processing Hardware, Software, and Products Containing the Same*, Inv. No. 337-TA-1026, Comm’n Op. at 9 (April 18, 2018) (citations omitted).

B. Claim Construction

“The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.” *Embrex, Inc. v. Serv. Eng’g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000). Although most of the disputed

[REDACTED]

claim terms were construed in an earlier order, some of the issues presented below are only resolvable with additional claim construction.

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *see also Markman v. Westview Instr., Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc). As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the “ordinary and customary meaning of a claim term” as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313. “Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.” *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). “Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms.” *Id.* at 1314; *see Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) (“In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to ‘particularly point [] out and distinctly claim [] the subject matter which the patentee regards as his invention.’”). The context in which a term is used in an asserted claim can be “highly instructive.” *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.* “Courts do not rewrite claims; instead, we give

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effect to the terms chosen by the patentee.” *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999). “[T]he specification ‘is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). “[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor’s lexicography governs.” *Id.* at 1316.

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Phillips*, 415 F.3d at 1317; see *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can “often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips*, 415 F.3d at 1317; see *Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (“The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.”).

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* “The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with

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the construction mandated by the intrinsic evidence.” *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) “the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;” or (2) “the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009); *see GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (“the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal.”); *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) (“[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.”); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) (“The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution.”). Nevertheless, there is a “heavy presumption that a claim term carries its ordinary and customary meaning.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is “exacting” and requires “a clear and unmistakable disclaimer.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012); *see Epistar Corp. v. Int’l Trade Comm’n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring “expressions of manifest exclusion or restriction,

representing a clear disavowal of claim scope” to deviate from the ordinary meaning) (citation omitted).

C. Infringement

“An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing.” *Markman*, 52 F.3d at 976.

A patentee may prove infringement either literally or under the doctrine of equivalents. Infringement of either sort must be proven by a preponderance of the evidence. *SmithKline Diagnostics, Inc. v. Helena Labs. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). A preponderance of the evidence standard “requires proving that infringement was more likely than not to have occurred.” *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n.15 (Fed. Cir. 2005).

Literal infringement, a form of direct infringement, is a question of fact. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). “To establish literal infringement, every limitation set forth in a claim must be found in an accused product, exactly.” *Microsoft Corp. v. GeoTag, Inc.*, 817 F.3d 1305, 1313 (Fed. Cir. 2016) (quoting *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed. Cir. 1995)). If any claim limitation is absent, there is no literal infringement of that claim as a matter of law. *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000).

Doctrine of equivalents is also a form of direct infringement. One rubric for evaluating if a claimed feature is not literally, but nonetheless equivalent to, a claimed feature is known as the function-way-result test. Under this test, the accused feature is equivalent to the claim limitation when “it performs substantially the same function in substantially the same way to obtain the same

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result.” *Duncan Parking Techs., Inc. v. IPS Grp., Inc.*, 914 F.3d 1347, 1362 (Fed. Cir. 2019) (quoting *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608 (1950)). Another test is known as the insubstantial differences test, where “[a]n element in the accused device is equivalent to a claim limitation if the only differences between the two are insubstantial.” *Voda v. Gordia Corp.*, 536 F.3d 1311, 1139 (Fed. Cir. 2008). The Supreme Court has further instructed, “the proper time for evaluating equivalency . . . is at the time of infringement, not at the time the patent was issued.” *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 37 (1997).

D. Domestic Industry

In an investigation based on a claim of patent infringement, Section 337 requires that an industry in the United States, relating to the articles protected by the patent, exist or be in the process of being established. 19 U.S.C. § 1337(a)(2). Under Commission precedent, the domestic industry requirement has been divided into (i) a “technical prong” (which requires articles covered by the asserted patent) and (ii) an “economic prong” (which requires certain levels of activity with respect to the protected articles or patent itself). *See Certain Video Game Systems and Controllers*, Inv. No. 337-TA-743, Comm’n Op. at 6-7 (April 14, 2011) (“*Video Game Systems*”).

1. Technical Prong

The technical prong of the domestic industry requirement is satisfied when the complainant in a patent-based section 337 investigation establishes that it is practicing or exploiting the patents at issue. *See* 19 U.S.C. §§ 1337 (a)(2), (3); *Certain Microsphere Adhesives, Process for Making Same and Prods. Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm’n Op. at 8 (U.S.I.T.C. Jan. 16, 1996). “In order to satisfy the technical prong of the domestic industry requirement, it is sufficient to show that the domestic industry practices any claim of that patent, not necessarily an asserted claim of that patent.” *Certain Ammonium*

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Octamolybdate Isomers, Inv. No. 337-TA-477, Comm’n Op. at 55 (U.S.I.T.C. Aug. 28, 2003). Historically, the Commission permits the complainant’s products, and those of its licensees, to be considered for technical prong purposes. *See Certain Magnetic Tape Cartridges and Components Thereof*, Inv. No. 337-TA-1058, Comm’n Op. at 28-29 (April 9, 2019).

The test for claim coverage for the purposes of the technical prong of the domestic industry requirement is the same as that for infringement. *See Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109 (U.S.I.T.C. May 21, 1990), *aff’d*, Views of the Commission at 22 (U.S.I.T.C. Oct. 31, 1990); *Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). “First, the claims of the patent are construed. Second, the complainant’s article or process is examined to determine whether it falls within the scope of the claims.” *Certain Doxorubicin and Preparations Containing Same*, Inv. No. 337-TA-300, Initial Determination at 109. As with infringement, the technical prong of the domestic industry can be satisfied either literally or under the doctrine of equivalents. *Certain Dynamic Sequential Gradient Devices and Component Parts Thereof*, Inv. No. 337-TA-335, ID at 44, Pub. No. 2575 (U.S.I.T.C. May 15, 1992). In short, the patentee must establish by a preponderance of the evidence that the domestic product practices one or more claims of the patent.

2. Economic Prong

The “economic prong” of the domestic industry requirement is satisfied when there exists in the United States, in connection with products practicing at least one claim of the patent at issue: (A) significant investment in plant and equipment; (B) significant employment of labor or capital; or (C) substantial investment in its exploitation, including engineering, research and development, and licensing. 19 U.S.C. § 1337(a)(3). Establishment of the “economic prong” is not dependent on any “minimum monetary expenditure” and there is no need for complainant “to define the industry itself in absolute mathematical terms.” *Certain Stringed Musical Instruments and*

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Components Thereof, Inv. No. 337-TA-586, Comm’n Op. at 25-26 (May 16, 2008) (“*Stringed Instruments*”). However, a complainant must substantiate the significance of its activities with respect to the articles protected by the patent. *Certain Printing and Imaging Devices and Components Thereof*, Inv. No. 337-TA-690, Comm’n Op. at 30 (Feb. 17, 2011) (“*Imaging Devices*”). Further, a complainant can show that its activities are significant by showing how those activities are important to the articles protected by the patent in the context of the company’s operations, the marketplace, or the industry in question. *Id.* at 27-28. That significance, however, must be shown in a quantitative context. *Lelo Inc. v. Int’l Trade Comm’n*, 786 F.3d 879, 886 (Fed. Cir. 2015). The Federal Circuit noted that when the ITC first addressed this requirement, it found the word “‘significant’ denoted ‘an assessment of the *relative* importance of the domestic activities.’” *Id.* at 883-4 (internal citation omitted) (emphasis added). In general, “[t]he purpose of the domestic industry requirement is to prevent the ITC from becoming a forum for resolving disputes brought by foreign complainants whose only connection with the United States is ownership of a U.S. patent.” *Certain Battery-Powered Ride-On Toy Vehicles*, Inv. No. 337-TA-314, USITC Pub. No. 2420, Initial Determination at 21 (Aug. 1991).

E. Invalidity

1. 35 U.S.C. § 102

Pursuant to 35 U.S.C. § 102, a patent claim is invalid as anticipated if:

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant;
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States;
- (c) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application

for patent by another filed in the United States before the invention by the applicant for patent;”

(g)(2) before such person’s invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.

35 U.S.C. § 102 (pre-AIA). “A patent is invalid for anticipation if a single prior art reference discloses each and every limitation of the claimed invention. Moreover, a prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference.” *Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003) (citations omitted); *see Santarus, Inc. v. Par Pharm., Inc.*, 694 F.3d 1344, 1354 (Fed. Cir. 2012). “A century-old axiom of patent law holds that a product ‘which would literally infringe if later in time anticipates if earlier.’” *Upsher-Smith Labs., Inc. v. Pamlab, L.L.C.*, 412 F.3d 1319, 1322 (Fed. Cir. 2005) (citing *Schering Corp.*, 339 F.3d at 1322).

2. 35 U.S.C. § 103

Section 103 of the Patent Act states:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

35 U.S.C. § 103(a) (pre-AIA). “Obviousness is a question of law based on underlying questions of fact.” *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1379 (Fed. Cir. 2008). The underlying factual determinations include: “(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness.” *Id.* (citing *Graham v. John Deere Co. of*

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Kansas City, 383 U.S. 1, 17-18 (1966)). These factual determinations are often referred to as the “Graham factors.”

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-21 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit’s rigid application of the teaching-suggestion-motivation test. While the Court stated that “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does,” it described a more flexible analysis:

Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 418. Since *KSR*, the Federal Circuit has announced that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, “the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device . . . and would have had a reasonable expectation of success in doing so.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007); *see KSR*, 550 U.S. at 399 (“The proper question was whether a pedal designer of ordinary skill in the art, facing the wide range of needs created by developments in the field, would have seen an obvious benefit to upgrading Asano with a sensor.”).

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In addition to demonstrating that a reason exists to combine prior art references, the challenger must demonstrate that the combination of prior art references discloses all of the limitations of the claims. *Hearing Components, Inc. v. Shure Inc.*, 600 F.3d 1357, 1373-4 (Fed. Cir. 2010) (abrogated on other grounds by *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S.Ct. 2120 (2014)) (upholding finding of non-obviousness based on the fact that there was substantial evidence that the asserted combination of references failed to disclose a claim limitation); *Velandier v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (explaining that a requirement for a finding of obviousness is that “all the elements of an invention are found in a combination of prior art references”).

An obviousness determination should also include a consideration of “secondary considerations” such as “commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.” *Graham*, 338 U.S. at 17-18. “For [such] objective evidence to be accorded substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention.” *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995); see *Merck & Cie v. Gnosis S.P.A.*, 808 F.3d 829, 837 (Fed. Cir. 2015). “Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention.” *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011).

3. 35 U.S.C. § 112

Pursuant to 35 U.S.C. § 112, a patent claim is invalid for lack of written description if the patent’s specification fails to “reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). “[T]he test requires an objective inquiry into

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the four corners of the specification from the perspective of a person of ordinary skilled in the art” (*id.*), and “the level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology” (*id.* (citing *Capon v. Eshar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005))).

Additionally, under 35 U.S.C. § 112, a patent claim is invalid for indefiniteness if “its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus*, 134 S. Ct. at 2124. Indefiniteness can result from a single claim covering both an apparatus and a method of use of that apparatus, as “a manufacturer or seller of the claimed apparatus would not know from the claim whether it might also be liable for contributory infringement because a buyer or user of the apparatus later performs the claimed method using the apparatus.” *IPXL Holdings v. Amazon.com*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); *see UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 826 (Fed. Cir. 2016) (holding these types of claims may make it “unclear whether infringement . . . occurs when one creates an infringing system, or whether infringement occurs when the user actually uses the system in an infringing manner”) (citation omitted). “[A]pparatus claims are not necessarily indefinite for using functional language,” however, as in, for example, means-plus-function formatted claims. *MasterMine Software, Inc. v. Microsoft Corp.*, 874 F.3d 1307, 1313 (Fed. Cir. 2017) (citing *Microprocessor Enhancement Corp. v. Tex. Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008)). Another example may be when the claim merely recites “that the system ‘possesses the recited structure which is capable of performing the recited functions.’” *Id.* at 1315-16 (quoting *Microprocessor Enhancement*, 520 F.3d at 1375). Overall, “the written description is *key* to determining whether a term of degree is indefinite.” *Guangdong Alison Hi-Tech Co. v. Int’l Trade Comm’n*, 936 F.3d

1353, 1361 (Fed. Cir. 2019) (citing *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1378 (Fed. Cir. 2017)) (emphasis in original).

Further, under 35 U.S.C. § 112, a patent specification must contain a description “of the manner and process of making and using” the invention. 35 U.S.C. § 112. This is referred to as the enablement requirement, and a patent claim is sufficiently enabled only when the specification teaches “those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation.” *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997). To determine whether the specification leaves a person of ordinary skill to perform undue experimentation, the Federal Circuit has identified the following factors to consider: (1) the quantity of experimentation necessary; (2) the amount of direction or guidance presented; (3) the presence or absence of working examples; (4) the nature of the invention; (5) the state of the prior art; (6) the relative skill of those in the art; (7) the predictability or unpredictability of the art; and (8) the breadth of the claims. *In re Wands*, 585 F.2d 731, 737 (Fed. Cir. 1988). “[I]t is not necessary that a court review all the *Wands* factors to find a disclosure enabling. They are illustrative, not mandatory.” *Amgen, Inc. v. Chugai Pharm. Co., Ltd.*, 927 F.2d 1200, 1213 (Fed. Cir. 1991).

III. IMPORTATION AND JURISDICTION

In its initial post-hearing brief, Tela asserts that “Respondents do not deny that they make the Accused Products over which the Commission has *in rem* jurisdiction.” CIB at 10. Tela notes that respondent Intel stipulated that it imports, sells for importation, and sells after importation into the United States various generations of its portion of the Accused Products (*see id.* at 11 (citing JX-0017C; CDX-0003C)) and argues the other respondents also import, sell for importation, or sell after importation, their respective Accused Products. Respondents do not dispute the Commission’s jurisdiction over this investigation or that the requisite importation or sales in

connection with importation of their respective Accused Products has taken place. *See* RIB at 13. Accordingly, the importation requirement under 19 U.S.C. § 1337(a)(1)(B) is satisfied, and the Commission has *in rem* jurisdiction over the Accused Products.

IV. U.S. PATENT NO. 10,141,334

A. Level of Ordinary Skill in the Art

In Order No. 34, I determined that a person having ordinary skill in the art of the 334 patent at the time of invention “would have: (1) a bachelor’s degree in electrical engineering or computer engineering with at least three years of experience in the field of semiconductor layout technology and integrated circuit design; (2) a master’s degree in electrical engineering or computer engineering with at least two years of experience in the same field; (3) a bachelor’s degree in physics or materials science with at least five years of experience in the same field; or (4) a comparable combination of education and experience.” Order No. 34 at 8. The parties do not challenge this determination (*see* RIB at 15; SIB at 24; *see generally* CIB; CRB; RRB; SRB), and it is applied throughout this initial determination.

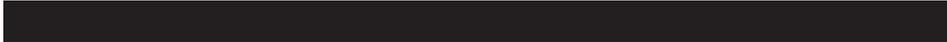
B. Claims-at-Issue

Claims 1, 2, 5, 15, 29, and 30 of the 334 patent are at issue in this investigation, either through allegations of infringement or of the domestic industry technical prong. *See* CIB at 11,

66. These claims are reproduced below along with additional claim limitation identifiers:

1. [1a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip,

[1b] the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,



[1c] wherein each gate gridline has at least one gate structure positioned thereon, wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[1d] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,

[1e] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[1f] a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material,

[1g] wherein the first-metal layer includes first-metal structures positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline,

[1h] each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers; and

[1i] at least six contact structures formed within the region of the semiconductor chip, wherein at least six gate structures within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six contact structures,

[1j] each of the at least six contact structures having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in the x-direction, each of

the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,

[1k] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein the logic circuit includes electrical connections that collectively include first-metal structures positioned on at least five of the at least eight first-metal gridlines.

2. [2a] The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures positioned in accordance with a second-metal horizontal grid, the second-metal horizontal grid including at least eight second-metal gridlines,

[2b] each second-metal structure in the region having at least one adjacent second-metal structure positioned next to each of its sides in accordance with an x-coordinate spacing of less than or equal to 193 nanometers, each second-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline,

[2c] wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure positioned thereon, wherein each pair of second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap,

[2d] wherein the second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the gate structures.

....

5. The semiconductor chip as recited in claim 2, wherein the at least six contact structures are positioned in accordance with a contact vertical grid, the contact vertical grid including contact gridlines extending in the x-direction, each of the at least six contact structures positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six contact structures positioned to also extend lengthwise in the x-direction in a substantially centered manner along a corresponding first-metal gridline.

....

15. The semiconductor chip as recited in claim 1, wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of at least one transistor within the region of the semiconductor chip has a substantially rectangular shape.

....

29. [29a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon,

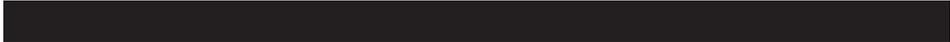
[29b] wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[29c] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,

[29d] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[29e] a number of contact structures formed within the region of the semiconductor chip, wherein each gate structure that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding contact structure having a substantially rectangular shape, wherein each contact structure that contacts a given gate structure that forms any transistor gate electrode does not contact another gate structure, wherein each contact structure having a corresponding length greater than or equal to a corresponding width is oriented to have its corresponding length extend in an x-direction, wherein each contact structure that contacts a corresponding gate structure is positioned to overlap at least one edge of the corresponding gate structure,

[29f] wherein each transistor within the region is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,



[29g] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

[29h] wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a first gate structure forms both a gate electrode of the first transistor of the first transistor type and a gate electrode of the first transistor of the second transistor type.

30. [30a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes a number of gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon,

[30b] wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[30c] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,

[30d] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[30e] a number of contact structures formed within the region of the semiconductor chip, wherein each of at least six gate structures within the region has a respective top surface in physical and electrical contact with a

corresponding contact structure having a substantially rectangular shape, wherein each contact structure is centered in an x-direction on the gate structure with which it physical contacts,

[30f] wherein each contact structure that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in an x-direction, wherein each corresponding contact structure is in physical contact with only one gate structure, wherein each corresponding contact structure is positioned to overlap at least one edge of the gate structure contacted by the corresponding contact structure,

[30g] wherein each transistor within the region is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

[30h] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

[30i] wherein both a gate electrode of a transistor of a first transistor type and a gate electrode of a transistor of a second transistor type are formed by a same gate structure within the region.

See 334 patent at cls. 1, 2, 5, 15, 29, 30 (annotated).

C. Claim Construction

As part of the *Markman* process, the following terms of the 334 patent were construed, either as agreed between the parties or as determined by Order No. 34:

Claim Term	Construction
“gate electrode”	“that portion of a gate electrode feature that forms a transistor gate”
“gate electrode feature(s)” / “gate structure(s)”	“a feature comprising a transistor gate”
“diffusion region(s)”	“selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor”



“[gate horizontal / first-metal vertical grid]; [second-metal horizontal] grid; [contact vertical] grid; [third-metal vertical] grid; [diffusion contact] grid”	“projected gridlines used at least during the fabrication stage of integrated circuit manufacturing”
“[gate / metal / contact] gridline(s)”	“one of the lines making up a grid”
“gate pitch”	“center-to-center separation distance between adjacent gate features”

See generally Order No. 34 at 52, 55, 56, 59, 60, 62. Notably, for the reasons expressed in Order No. 34, “contact structure(s)” and “gate contact structure(s)” were not construed. *Id.* at 61. The parties do not now explicitly identify these terms, or any others, as requiring construction. See RIB at 15-16; SIB at 23-24; see generally CIB; CRB; RRB; SRB. Thus, the scope of “contact structure(s)” and “gate contact structure(s)” are addressed below in the infringement and validity determinations to the extent required.

D. Infringement

According to Tela’s post-hearing briefing, the use, manufacture, or sale of the following Accused Products, and those computer products containing the same, are alleged to infringe the asserted claims of the 334 patent:

Claims	Accused Products Alleged to Infringe
1, 2, 5, 15	Intel 14nm Products
1, 2, 5, 15	Intel 10nm Products

See CIB at 11. Of these claims, claim 1 is independent and claims 2, 5, and 15 depend from it.

Respondents contest Tela’s claims of infringement under claims 1 and 15. See RIB at 16-49; RRB at 3-27. The Staff contests infringement under these claims, along with claims 2 and 5.

[REDACTED]

See SIB at 45. For the reasons discussed below, Tela has not shown infringement by any of the Intel 10nm Products under any of the Asserted Claims. Tela has shown infringement for the Broadwell, Skylake, Kaby Lake, Coffee Lake, and Cascade Lake models of Intel 14nm Products under claims 1, 2, and 5. No Accused Products have been shown to infringe claim 15.

1. Claim 1

For reference, claim 1 of the 334 patent requires:

1. [1a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip,

[1b] the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,

[1c] wherein each gate gridline has at least one gate structure positioned thereon, wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[1d] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,

[1e] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[1f] a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material,

[1g] wherein the first-metal layer includes first-metal structures positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline,

[1h] each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers; and

[1i] at least six contact structures formed within the region of the semiconductor chip, wherein at least six gate structures within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six contact structures,

[1j] each of the at least six contact structures having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in the x-direction, each of the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,

[1k] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein the logic circuit includes electrical connections that collectively include first-metal structures positioned on at least five of the at least eight first-metal gridlines.

334 patent at cl. 1 (annotated). Several disputes exist between the parties concerning whether Tela has sufficiently shown the Accused Products meet various limitations of the claim. These are addressed below. In view of the testimony of Dr. Foty that the Accused Products meet those remaining limitations which are not in dispute, the Accused Products have been shown to meet them as alleged. *See* CX-1144C at Q/A 1460-1648, 2395-2525²; CIB at 11-52.

² Starting at Q/A 1853, the question and answer numbering of Dr. Foty's witness statement (CX-1144C) becomes disjointed, and then again at Q/A 2549, and then again at Q/A 2606. Out of an abundance of caution, citations in this initial determination to a particular numbered question

[REDACTED]

a. Gate structures positioned in accordance with a gate horizontal grid

First, Respondents and Staff dispute that “gate structures positioned in accordance with a gate horizontal grid” is met in the Intel 14nm Products and the Intel 10nm Products. RIB at 16-19, 46; SIB at 27-32. Order No. 34 construed “grid” as it is used in this limitation as “projected gridlines used at least during the fabrication stage of integrated circuit manufacturing.” Order No. 34 at 59.

Tela contends, generally, that the limitation is met in the Accused Products because Intel utilizes a “1-D gridded approach” with “relevant layouts for the accused 14nm and 10nm Intel products [that] specify the size, shape, and spacing of gate structures so that those gate structures, when formed, have a substantially rectangular shape and are positioned in accordance with a gate horizontal grid as claimed” and “the claimed gate horizontal grid is, in fact, used (or ‘projected’) during manufacturing of the Intel 14nm and 10nm products pursuant to the ALJ’s construction.” See CIB at 12-13. Specifically, Tela argues “projected” in this construction “merely means that the grid is used to define the position of various features during the fabrication stage ‘with no limitation on how that is achieved.’” *Id.* (citing Order No. 34 at 58; 334 patent at 30:4-5; 523 patent at 11:18-19). For both the Intel 14nm Products and the Intel 10nm Products, Tela argues that one fabrication step involves “[REDACTED]

[REDACTED]

[REDACTED]” *Id.* at 15 (citing CX-1144C at Q/A 390-391; CPX-0410C; JX-0210C at *87), 19 (citing CX-1144C at Q/A 414-419, 427; CPX-0030C). In its reply brief, Tela explains:

and answer should be interpreted to apply to both the question bearing that number and the answer bearing that number.

[REDACTED]

Intel uses the gate grid in these further processing steps by [REDACTED]

[REDACTED] (CX-1144C (Foty) at Q/A 417-418; RX-0008C (Auth) at Q/A 103-105; Tr. (Auth) at 686:2-690:8 [REDACTED] 752:2-753:10 [REDACTED]

[REDACTED] The fact that one step of the fabrication stage allegedly does not use the grid does not preclude infringement, particularly where other parts of the fabrication stage do. *See Tate Access Floors v. Maxcess Techs.*, 222 F.3d 958, 970 (Fed. Cir. 2000) (“[O]ne cannot avoid infringement merely by adding elements if each element recited in the claims is found in in the accused device.”).)

CRB at 4.

Tela provides the following SEM image of an Intel 14nm Product as evidencing the “grid”:



JX-0210C at *87; *see* CIB at 16. Intel asserts “[a] simple, visual inspection of the layouts and resulting semiconductor shows that these features are formed along gridlines.” CRB at 2 (citing JX-210C at *87).

[REDACTED]

Tela views Respondents' expert, Dr. Subramanian, as "tacitly admit[ing]" the "structures positioned in accordance with a gate horizontal grid" aspect of the limitation is met (CIB at 13 (citing Hr'g Tr. at 876:3-877:8)), although he also contends that "use of the word 'projected' changes that ordinary meaning and the scope of the claims"—an opinion Tela urges should be rejected as contrary to basic principles of claim construction (*id.*). Tela contends "[n]othing in the ALJ's construction of 'grid' requires a lithographic projection of gridlines [during fabrication]." CRB at 2 (citing Order No. 34 at 57), 4.

Respondents contend the limitation is not met in the Intel 14nm Products because "Tela's expert, Dr. Foty, offered *no* opinion in his witness statement or at the hearing regarding how any alleged gate grid is used during fabrication." RIB at 16. Respondents specify that "the ALJ's construction of 'grid' is not directed to lines arbitrarily drawn after the fact on layout files or the final chip. For the '334 patent the grid must be used during *fabrication*." *Id.* at 16-17 (emphasis in original). This is not done in either the Intel 14nm Products or Intel 10nm Products, Respondents argue, because "[a]ll the evidence in the record of projection during fabrication comes in the context of lithography . . . [yet] [REDACTED] [REDACTED] in 14nm and 10nm process nodes. *See id.* at 17 (citing Hr'g Tr. at 424:19-425:9, 881:13-882:3; RX-0014C at Q/A 200-203, 299-303, 346-353; RX-0008C at Q/A 106, 110), 18 (citing RX-0008C at Q/A 119; RX-0012C at Q/A 18), 46 (citing RX-0014C at Q/A 408, 388-393); RRB at 4 (citing RX-0008C at Q/A 101-107; RX-0014C at Q/A 300, 356-357; Hr'g Tr. at 283:14-284:3). Respondents add, "Tela also does not dispute that during fabrication, the centerlines of the gates are determined *not* according to any pre-existing grid, but by [REDACTED]" RRB at 3 (citing Hr'g Tr. at 283:14-284:3).

[REDACTED]

Further, while lithography is used by Intel to form the [REDACTED] structures, Respondents explain these are “not the gates themselves [but] [REDACTED] [REDACTED] that actually form the gate shapes.” *Id.* at 17 (citing RX-0014C at Q/A 309-310; RDX-0016C at *149). Respondents claim it is undisputed these [REDACTED] do not fall along the alleged “gate gridlines.” *Id.* at 18 (citing RX-0014C at Q/A 405-410). Regardless, Respondents caution that in discussing these structures, Tela is attempting to contravene Order No. 42—an order denying Respondents’ motion *in limine* but issued with the understanding that Tela would not be presenting an infringement case which treated the [REDACTED] [REDACTED] structures as the “grid” in the 334 patent. RRB at 5-6 (citing, *inter alia*, Order No. 42 at 2).

The Staff agrees with Respondents’ positions on this limitation. *See* SIB at 29 (“Tela improperly vies the claimed ‘grid’ as only requiring similar end result structure/functionality for the ‘gate structures,’ thereby contradicting the ALJ’s claim construction of ‘grid,’ which requires a specific process limitation.”), 31 (“Intel uses a new technique known as [REDACTED] [REDACTED] but not the gates themselves. . . . it is undisputed that these [REDACTED] shapes do not fall along the alleged ‘gate gridlines’ or otherwise correspond to the supposed ‘gate grid.’”); *see generally* SIB at 27-32; SRB at 4-8.

This limitation is met in the Accused Products. In short, Respondents’ and Staff’s position is based in the “projected” portion of Order No. 34’s construction—“projected gridlines used at least during the fabrication stage of integrated circuit manufacturing”—and sees the absence of an actual, observable, emission of light (or other energy/substance) in the fabrication of the Accused Products as grounds for non-infringement. *See, e.g.*, Hr’g Tr. at 876:20-877:1 (“With respect to

[REDACTED]

the gate, I have not offered an opinion for non-infringement, with respect to the gridlines, for the purposes of the design rule analysis. However, I have offered the opinion that it is clear that there is no use of gate gridlines consistent with the claims with respect to the projection requirements associated therewith.”), 878:2-23 (“With respect to the second part of the answer, where I was referring to fabrication, it would be you actually have a gate gridline projected during the fabrication process. So for example, if you’re talking about lithography, I would expect gridlines to be lithographically projected. And that is not the case in the accused products.”). This is not the meaning of the ordered construction: “[i]n short, the claims (as opposed to the specification) do not require projection of a ‘grid’ and do not require such projection to be either virtual or actual.” Order No. 34 at 58. Further, as explained, the term “projected” was only put into the ordered construction because all parties incorporated it into their respective proposed constructions, and the term did appear at least once in the shared specification of the Asserted Patents. *See id.* at 56 (citing 523 patent at 11:18-19).

The clearest use of the term “projected” in the specification refers to “grid” in a virtual, or conceptual, sense:

FIG. 3A is an illustration showing an exemplary base grid to be projected onto the dynamic array to facilitate definition of the restricted topology, in accordance with one embodiment of the present invention. The base grid can be used to facilitate parallel placement of the linear-shaped features in each layer of the dynamic array at the appropriate optimized pitch. Although not physically defined as part of the dynamic array, the base grid can be considered as a projection on each layer of the dynamic array. Also, it should be understood that the base grid is projected in a substantially consistent manner with respect to position on each layer of the dynamic array, thus facilitating accurate feature stacking and alignment.

334 patent at 13:1-13. Notably, there is no mention in either patent of what kind of equipment, or when in the tightly controlled fabrication process, an actual, observable emission of a grid would occur, or that it would even facilitate the act of positioning gate structures. *See generally* 334

patent; 523 patent. Obviously, the Accused Products and the like are not handmade, where projections of light would be used as guides for a human operator and their work tool.

Additionally, the patent discusses “defin[ing]” the grid with consideration for light interaction effects (effects that can be mathematically characterized by a “sinc function”) such that “the spacing between gridpoints enables alignment of peaks in the sinc functions describing the light energy projected upon neighboring gridpoints.” 334 patent at 13:33-45. Yet there is no discussion of how the light from a “projected” grid—if any—is also taken into account. In sum, the specification does not support interpreting the “grid” as an actual, observable projection of light.

Despite this, Respondents suggest that in a plain and ordinary sense—and for those skilled in the art—actual, observable projections of grids are used in “various” ways in processor fabrication, but that Intel simply does not use those techniques. Respondents state:

Indeed, the unrebutted fact testimony of Intel witnesses is that Intel does not project any gridlines during fabrication. RX-0008C (Auth) at Q/A 119; RX-0012C (Kelleher) at Q/A 18. *Dr. Subramanian likewise testified that projected gridlines can be used during fabrication in various ways, but that Intel’s fabrication process does not use those techniques.* RX-0014C (Subramanian) at Q/A 192-197; Tr. (Subramanian) at 881:13-882:3 (“I am interpreting projected for use during fabrication to simply mean that there are gridlines that are available, and are actually used during fabrication. And that is not the case.”).

RIB at 18 (emphasis added). But the citation Respondents use to justify these “various” (*i.e.*, more than one) ways is the testimony of their expert, who was asked, “[h]ow might gridlines be projected?” RX-0014C at Q/193. And Dr. Subramanian, an expert in the field (*see* RX-0007C at Q/A 8-14), only observed that the 523 patent “claims at column 11, lines 19-23 that ‘the base grid is projected in a substantially consistent manner with respect to position on each layer of the

[REDACTED]

dynamic array, thus facilitating accurate feature stacking and alignment” (RX-0014C at Q/A 193).³

This is far from evidence that “projected gridlines can be used during fabrication in various ways,” and the quoted intrinsic evidence (523 patent at 11:19-23) is not even a statement on “ways” in which projected gridlines are used. Rather, it is a statement on the benefits of consistent “projection”—*i.e.*, the facilitation of accurate feature alignment within the integrated circuit’s many layers.

Dr. Subramanian’s invalidity opinions reinforce the conclusion that actual, observable emissions of grids to facilitate gate placement during fabrication are not real processes. For the Intel 45nm Product prior art reference, Dr. Subramanian admits that no such projection takes place and so the limitation can only be taught if Tela’s infringement theory succeeds:

Under the Court’s construction of “gate horizontal grid” and “gate gridlines,” there must be a projected grid used during the fabrication stage of integrated circuit manufacturing. There is no such grid projected during fabrication. However, under Tela’s infringement theory, any lines along which the structures corresponding to poly are defined are gridlines. Under this theory, Intel’s 45nm products’ gate structures are positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines.

RX-0014C at Q/A 385. For the Becker prior art reference, however, Dr. Subramanian asserts there is an explicit disclosure of a virtual grid which satisfies Order No. 34:

Becker describes at paragraphs [0050] to [0052] and [0066] that a base grid facilitates parallel placements of the features that would include the polysilicon features on 1403A to 1403G. Becker describes at paragraph [0050] that the base grid is not a physical part of the dynamic array, so a

³ Additionally, although not cited by Respondents, Dr. Subramanian’s other testimony was inconsistent regarding gridline projection. He testified “[i]f I was looking specifically at the lithographic process, for example, one way to get gridlines during a lithographic process would be to project it through the mask.” Hr’g Tr. at 881:21-24. But he also admitted this is not really something that is done: “[t]hat is not done in the accused products. *And in fact, there are no ways that I am aware of*, or that have been cited by Tela, that would establish that that is the case, that there are gridlines used during fabrication.” *Id.* at 881:24-882:3 (emphasis added).

POSITA would understand it is virtual. Further, Becker describes in that same paragraph that the base grid would be understood as a projection on each layer to facilitate accurate fabrication of features. For those reasons, the [] base grid satisfies the Court's construction of "gate grid" and "gridlines."

Id. at Q/A 848. But this latter position is in conflict with his opinions on the Intel 14nm Products, Intel 10nm Products, and Intel 45nm Product, to the effect that such virtual grids do not meet the ordered construction. *See* RX-0014C at Q/A 837-842. And Respondents take a similar inconsistent position in connection with invalidity. *See, e.g.*, RIB at 112-113 (stating "Tela does not dispute that Becker renders obvious each and every limitation of the '334 patent" and "it expressly discloses all elements, except for certain claimed ranges and spacings . . .").

In sum, the record does not support finding that "projected" gridlines need be anything more than virtual, conceptual lines which "gate structures are positioned in accordance with." 334 patent at cl. 1. No actual, observable projections are required. In fact, Dr. Subramanian's explanation of "projected" at the hearing is not necessarily inconsistent with this conclusion. *See* Hr'g Tr. at 881:13-20 ("Q. And so you're interpreting projection to require an actual projection by projecting and moving onto a screen. Is that true? A. No. You asked me to provide an example, and I gave an example. I am interpreting projected for use during fabrication to simply mean that there are gridlines that are available, and are actually used during fabrication.").

So "projected," a term not found in claim 1 but incorporated into that claim's construction, includes virtual or conceptual lines, and the parties have waded into a construction of the construction, which the Commission disfavors. *See Certain Automated Teller Machines, ATM Modules, Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-972, Comm'n Op. at 6 (Jan. 30, 2017) ("We find the claim constructions on review to be both more complicated, and less clear, than the claim terms themselves. Instead of focusing on interpreting the claim language, the parties invited the ALJ to construe the constructions, and then to construe

[REDACTED]

the constructions of the constructions. Doing so caused the constructions to lose sight of the claim language itself.”). In any event, Dr. Foty persuasively testified how the gate structures in the Accused Products are “positioned in accordance with a gate horizontal grid that includes at least seven gridlines,” where a grid is actual or virtual projected gridlines used at any point in the fabrication of an integrated circuit. In particular, the cited layout files for the Accused Products show the [REDACTED] (CDX-0009C at *8-13; CDX-0011C at *7-9) and teardown imagery shows the same (CDX-0009C at *20; CDX-0010C at *9). It does not matter that the *virtual* gridlines are only observable after gate creation and through controlling the [REDACTED] [REDACTED] to create the transistor gates. *See* RRB at 3. Intel documentation shows this arrangement, or positioning, was “in accordance” with a planned layout (*i.e.*, not happenstance). *See* CX-1144C at Q/A 686 (citing CX-0661C at -56472, 56460), 1912-1915 (citing CX-0135 at -13, -23; CPX-042 at -1512). Thus, the limitation is met in all Accused Products.

b. First-metal structures positioned in accordance with a first-metal vertical grid

Second, Respondents and Staff dispute whether “first-metal structures positioned in accordance with a first-metal vertical grid” is met in the Intel 14nm Products and Intel 10nm Products. RIB at 19-20, 46; SIB at 27-32.

For this limitation, Tela contends the “M0 layer” in the Intel 14nm Products and the “M0 layer” in the Intel 10nm Products both include structures positioned “using a 1-D gridded approach” in satisfaction of the claims; where “M0” “refers to the first metal interconnect layer above the gates.” CIB at 32, 34. Tela primarily relies on Intel’s design rules as evidence of the “1-D gridded approach” (*id.* at 32-37 (citing, *inter alia*, CX-1144C at Q/A 330-367, 438-440, 889-891, 1540-1570, 2034-2036, 2456-2470; RX-0008C at Q/A 145; CPX-0497C; CPX-0341C; CPX-

[REDACTED]

0097C)) in addition to “SEM images of the M0 interconnects” (*id.* at 34 (citing CX-1144C at Q.A 901-904, 1558; CDX-0008C at *68), 37 (citing CX-1144C at Q/A 2027-2030, 2462-2463; CDX-0010C at *36)). As one example, Tela argues the design rules specify [REDACTED]

[REDACTED] *Id.* at 33 (citing, *inter alia*, CX-1144C at Q/A 270, 330, 709; CPX-0497C at *780-781), 35 (citing, *inter alia*, CX-1144C at Q/A 270, 367, 709; CPX-0097C at *5851-5856).

Tela views Respondents’ non-infringement position as “premised upon a fixed pitch requirement” for any claimed “grid.” *See* CIB at 38. Tela contends this cannot be correct, in part under principles of claim differentiation and the language of dependent claim 19, which recites “each first metal structure positioned on any first-metal gridline within the region is positioned next to and spaced apart from at least one other first-metal structure in accordance with a fixed pitch.” *Id.* at 38-39 (citing 334 patent at cl. 19; Hr’g Tr. at 808:14-809:6, 812:16-20). Tela adds that Respondents’ presentation of M0 layouts next to each other with varying line widths juxtaposes images that are not meant to be viewed together and not otherwise in conflict with the claims. *See id.* at 39 (citing RPB at 22; Hr’g Tr. at 681:19-25); CRB at 11. To the extent Respondents argue there is no “projected” grid in connection with fabrication of the first-metal layer, Tela incorporates its discussion of this issue in the “gate structures” limitation. CRB at 9.

In their initial brief, Respondents rely on their discussion of the same limitation in the context of the 523 patent and summarize:

Intel’s [REDACTED] is not gridded, nor are any Metal-0 structures positioned in accordance with a grid. Moreover, as with the gate grid limitation discussed above, Tela’s expert offers no opinion at all regarding how any alleged first-metal grid is used during fabrication (as opposed to Tela’s expert drawing alleged gridlines after the fact on layout shapes or the final structures).

[REDACTED]

RIB at 20. In the 523 patent discussion, Respondents first discuss an emphasis on placing features at an “optimized pitch.” *Id.* at 132 (citing 523 patent at 11:14-17, 11:39-47, 15:21-35, Fig. 3A; RX-0014C at Q/A 211-218). Respondents then acknowledge [REDACTED] [REDACTED] but stress the “metal-0” layer (that which is accused of being the “first-metal” layer in the claim) is not and its layout is left to designers. RIB at 134-135 (citing, *inter alia*, RPX-1990C at *059, 076; RPX-1991C at *100, 120; RX-0008C at Q/A 139-143; Hr’g Tr. at 723:22-726:8), 143. Respondents contend “[i]n other words, in the Metal-0 layers, there is no defined ‘grid’ that shapes must be positioned in accordance with—whether uniform pitch or otherwise [because] [REDACTED] [REDACTED]” *Id.* at 135-136 (citing RX-0008C at Q/A 128-129; Hr’g Tr. at 722:4-21); *see id.* at 136 (“[REDACTED] [REDACTED] [REDACTED]”), 136-137 (“because Intel does not define any ‘grid’—regular or irregular—for the Metal-0 shapes to be positioned in accordance with, the Accused Products do not meet the claimed requirement that the ‘first-metal structure layout shapes are positioned in accordance with a ...grid.”), 138 (“Dr. Foty also attempts to rely on Intel layout files for Metal-0, such as the following, which [REDACTED] [REDACTED]”), 139 (“these lines—added after-the-fact by Tela’s expert—are not used by Intel.”). Respondents summarize:

As discussed above, the claim requires that there be a “first-metal vertical grid,” with layout shapes “positioned in accordance with” that grid and, more specifically, “positioned to extend ... in a substantially centered manner along” an associated gridline. However, instead of opining that there was a grid and that, during layout, Intel positioned shapes in accordance with it, Dr. Foty opined, in effect, that there were shapes and that an (irregular) grid could be drawn in accordance with those shapes after

[REDACTED]

layout. His ex-post analysis inverts the claim language, getting it backward. RX-0014C (Subramanian) at Q/A 216-20; Tr. (Subramanian) at 806:5-17.

RIB at 140.

Respondents also incorporate their argument regarding gridlines that are “projected” as discussed with the prior limitation, “gate structures positioned in accordance with gate horizontal grid,” noting “Intel does not project or otherwise use any such grid to position the Metal-0 layout shapes, [therefore] the Accused Products do not satisfy the ALJ’s construction.” RIB at 141 (citing RX-0014C at Q/A216-218; Hr’g Tr. at 723:9-15).

In their reply brief, Respondents contend Tela’s expert, Dr. Foty, inappropriately relies only on layout drawings for this limitation, which are only relevant to the 523 patent under the constructions contained in Order No. 34. *See* RRB at 10-11 (citing CX-1144C at Q/A 2457-2467)). In this way, Respondents argue any allusion to [REDACTED] used during fabrication to meet this limitation are untimely and should be ignored under Ground Rule 13.1. *See id.*

The Staff’s discussion of this limitation is incorporated into its discussions of “gate structures” and “grid” summarized above, and aligns with Respondents. *See* SIB at 27-34; SRB at 4-8.

The limitation is met. Much of the parties’ dispute has been resolved with the prior limitation “gate structures positioned in accordance with a gate horizontal grid.” Namely, no actual, observable projection of a grid is required, and the positioning of structures according to a documented plan indicates the positioning is “in accordance with” (*i.e.*, not happenstance).

Respondents’ additional point that “grid” is not met by the Metal-0 (M0) structures because there are no “gridding rules” which Intel designers must abide by (*see* RIB at 135-137) is not accurate. Respondents do not challenge that Intel’s design rules require [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] See CIB at 33, 35-36; *see, e.g.*, CX-1144C at Q/A 329-333, 358-367; CDX-0012C at *17 (citing CPX-0377C at -780); CPX-0497 at -780-781; Hr’g Tr. at 724:9-22; RPX-1991C at 120; RPX-0776C at 567. These are certainly rules, and their implementation results in the [REDACTED] and teardown imagery of the Accused Products, *i.e.*, a first-metal “grid.” This makes certain testimony from Intel witness [REDACTED]—not credible. RIB at 141 (citing Hr’g Tr. at 722:1-732:7).

The fact that the rules for the metal-0 structures allow [REDACTED] does not defeat infringement as Respondents contend. See RIB at 138-141, 143; RRB at 11. The intrinsic evidence does not support reading this characteristic into a construction of “grid” under principles of claim differentiation. Specifically, claim 19, dependent on claim 1, explicitly requires a single, fixed pitch for the first-metal structures. See 334 patent at cl. 19 (“The semiconductor chip as recited in claim 1, wherein each first-metal structure positioned on any first-metal gridline within the region is positioned next to and spaced apart from at least one other first-metal structure in accordance with a fixed pitch.”). Claims 13 and 18 are similar. See 334 patent at cls. 13 (“The semiconductor chip as recited in claim 2, wherein each first-metal structure in the region is positioned next to at least one other first-metal structure on a first side in accordance with a first-metal pitch and is positioned next to at least one other first-metal structure on a second side in accordance with the first-metal pitch”), 18 (“The semiconductor chip as recited in claim 1, wherein each of at least four of the first-metal gridlines has at least two first-metal structures positioned thereon within the region, wherein each

[REDACTED]

of the at least two first-metal structures positioned on the at least four of the first-metal gridlines is positioned next to and spaced apart from at least one other first-metal structure in accordance with a fixed pitch.”). *Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) (“[C]laim differentiation’ refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim.”). This differentiation between claim 1, which does not explicitly require a fixed pitch, and other claims, which do, is not automatically dispositive but does weaken Respondents’ reliance on the specification, which emphasizes structures placed at an “optimized pitch.” *Interactive Gift Express*, 256 F.3d at 1331 (“In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to ‘particularly point [] out and distinctly claim [] the subject matter which the patentee regards as his invention.”). Thus, irregular centerline-to-centerline distances between first-metal structures (*i.e.*, non-uniform pitch) cannot be a ground for non-infringement under claim 1. Indeed, Dr. Subramanian admitted at the hearing that fixed pitch was not a requirement. Hr’g Tr. at 808:18-809:5 (discussing similar limitation in 523 patent), 812:16-813:24 (discussing same).

Correspondingly, the fact that the rules, allowing for [REDACTED]
[REDACTED]
[REDACTED] (*see* RIB at 136; RRB at 72-73, 75) is not cause for concern, either. There is no restriction in the claims themselves, or that can be read in from the specification, that would limit where the grid is located. Indeed, the 334 patent discloses and illustrates that gridding systems may vary in different regions. 334 patent at Fig. 3B, 13:26-32. Regardless, the analysis here must be focused on the actual products at issue and not the full gamut of allowable designs under Intel’s rulebook.



Images of the Accused Products demonstrate that the pertinent structures are “positioned in accordance with a first-metal vertical grid”; the upper two images relate to the Intel 14nm Products and the lower to the Intel 10nm Products:



CRB at 8 (citing JX-210C at *84; CPX-0100C at -2152);



CDX-0010C at *40, 39. As shown, the “first-metal” structures are positioned in a linear and parallel fashion. Thus, they are positioned in the 334 patent’s “grid,” albeit  which distinguishes them from the gate structures discussed above. And the arrangement is intentional (*i.e.*, not happenstance) so the arrangement satisfies the “in accordance with” requirement. Accordingly, the Accused Products meet this limitation.

[REDACTED]

c. Each gate gridline has at least one gate structure positioned thereon

Third, Respondents and Staff dispute whether “each gate gridline has at least one gate structure positioned thereon” is met in the Intel 10nm Products, while only Respondents challenge the limitation in the Intel 14nm Products. RIB at 20-22, 46-48; SIB at 35-39.

For this limitation, Tela refers to its discussion of “gate structures positioned in accordance with a gate horizontal grid” and adds, for all Accused Products, that when more than one gate structure is positioned on a given gate gridline in the region, the end-to-end separation is always less than or equal to 193 nanometers, as required by claim 1. CIB at 24 (citing, *inter alia*, CX-1144C at Q/A 724, 1492-1506, 1930, 2419-2423; CDX-0009C at *14-20; CDX-0011C at *10-12). Further, Tela contends the Intel 14nm Products’ use of [REDACTED]

[REDACTED] on some gridlines does not defeat infringement, as Tela has:

[I]dentified regions that include seven gate gridlines, each with at least one transistor gate positioned on each gridline. For example, [REDACTED]

[REDACTED] each include a region that includes seven gate gridlines, with each gate gridline having at least one transistor gate positioned thereon.

CIB at 25; CRB at 14, 16. Regardless, Tela contends that embodiments within the 334 patent show regions with non-dummy gate structures on six of seven lines, demonstrating that dummy gates can constitute “gate structures” required for this limitation. *Id.* at 26 (citing 334 patent at Fig. 5); CRB at 16. Tela claims that [REDACTED]

[REDACTED] are properly considered as dummy gates and thus meet the construction for “gate structures” in the same way. CRB at 17 (citing, *inter alia*, CX-1144C at Q/A 583-584).

[REDACTED]

Tela also disputes that it has in any way been inconsistent with its identification of regions and gridlines across claim elements. *See id.* at 25-26. In its reply brief, Tela discusses the 14nm [REDACTED] in particular, and alleges Respondents “identify a portion that was not relied on by Tela or Dr. Foty,” noting that Tela instead “identified an infringing portion of the same cell with seven gate gridlines, each with at least one transistor gate positioned thereon (annotated in red)”:

[REDACTED]

CRB at 14. For the Intel 10nm Products, Tela again contends Respondents identify a different set of gridlines than what it relied on for proving up the limitation:

[REDACTED]

CRB at 15. In sum, Tela takes the position:

It is black letter law that “[t]he addition of features does not avoid infringement, if all the elements of the patent claims have been adopted.” *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 945 (Fed. Cir. 1990). The fact that Respondents identified seven gate gridlines that allegedly do not infringe under their interpretation of “gate structure” elsewhere in the cell does not avoid the seven gate gridlines within the Intel 14nm Products that infringe, even under Respondents’ interpretation requiring transistor gates on each gate gridline.

Id. at 14-15; *see id.* at 16 (“In other words, if the identified region includes seven gate gridlines where adjacent gate gridlines are separated by a gate pitch, then the claim is met. An eighth gridline that does not meet the claims is immaterial.”).

In opposition, Respondents contend “[t]he claim term ‘gate structure’ has been construed to mean ‘feature comprising a transistor gate.’ But the alleged grids include multiple gridlines with no transistor gate positioned thereon.” RIB at 20. For the Intel 14nm Products, Respondents argue “[f]or every 14nm cell Dr. Foty identifies, there is an alleged gridline that Dr. Foty numbers and relies on, but that [REDACTED] do not form transistor gates.” *Id.* at 21-22 (citing RX-0014C at Q/A 242-245; CDX-0008C at *16-21; CDX-0009C at *14-20); RRB at 8-9 (“None

[REDACTED]

of the regions identified by Dr. Foty has a transistor gate on each gridline”). For the Intel 10nm Products, Respondents argue they use [REDACTED] *Id.* at 20.

This technique results in [REDACTED]

[REDACTED]

[REDACTED]

Id. at 47-48 (citing RX-0014C at Q/A 233-234; CPX-0235C at *579; RPX-1704C; RPX-1708C). Respondents view Tela’s attempt to use [REDACTED] as “gate structures” as improperly rearguing claim construction and as otherwise not supported by the specification. RRB at 9-10.

Additionally, for these products, as opposed to the Intel 14nm Products, Respondents argue Tela has inconsistently identified what the claimed “region” is across different limitations and improperly excluded gridlines that are otherwise present in the “region” which do not contain gate structures, all in an attempt to avoid non-infringement. *See* RIB at 48 (citing, *inter alia*, CDX-0011C at *10, 11, 12, 17, 18; RX-0014C at Q/A 235-236, 243-245; RDX-0016C at *16; DCX-0010C at *41).

As noted, the Staff finds this limitation is met by the Intel 14nm Products, but not for the Intel 10nm Products. The Staff agrees with Tela that [REDACTED] in the Intel 14nm Products, which lie along a gridline, sufficiently qualify as “feature[s] comprising a transistor gate”:



The claim term “gate structure” has been construed to mean “feature comprising a transistor gate.” (Order No. 34). On its face, the formal construction does not explicitly allow for an inactive “dummy” transistor gate to replace an active, working transistor gate. But the ALJ’s claim construction considered the arguments by all parties that inactive, “dummy” gates were permissible on gridlines based on the intrinsic evidence and thus did not intend to exclude “dummy” gates, as no party argued for such a narrow construction.

SIB at 35-36. The trenches used in the Intel 10nm Products, on the other hand, cannot be “gate structures” according to the Staff, and the Staff relies on the same cell layout image as Respondents (reproduced above) to show non-infringement. *See id.* at 36-38 (citing, *inter alia*, RX-0014C at Q/A 233-234); SRB at 10-11. Further, Tela’s use of less than all gridlines in a “region” is improper, according to Staff, because “if more than seven gate gridlines exist in a selected region, then every gridline (not just seven) must be shown to have ‘at least one gate structure positioned thereon.’” SRB at 9. Last, the Staff agrees with Respondents that Tela has inconsistently and improperly identified the “region” across claim limitations, again citing the same evidence as Respondents. *See* SIB at 39 (citing, *inter alia*, RX-0014C at Q/A 235-236, 243-245; RDX-0016C at *16; CDX-0010C at *41).

Unlike some other disputes, resolution of this one depends upon the details of each of the cells. For background, these include:

Intel 14nm Products		Intel 10nm Products

See, e.g., CDX-0009C; CDX-0011C; CIB at App’x B.

[REDACTED]

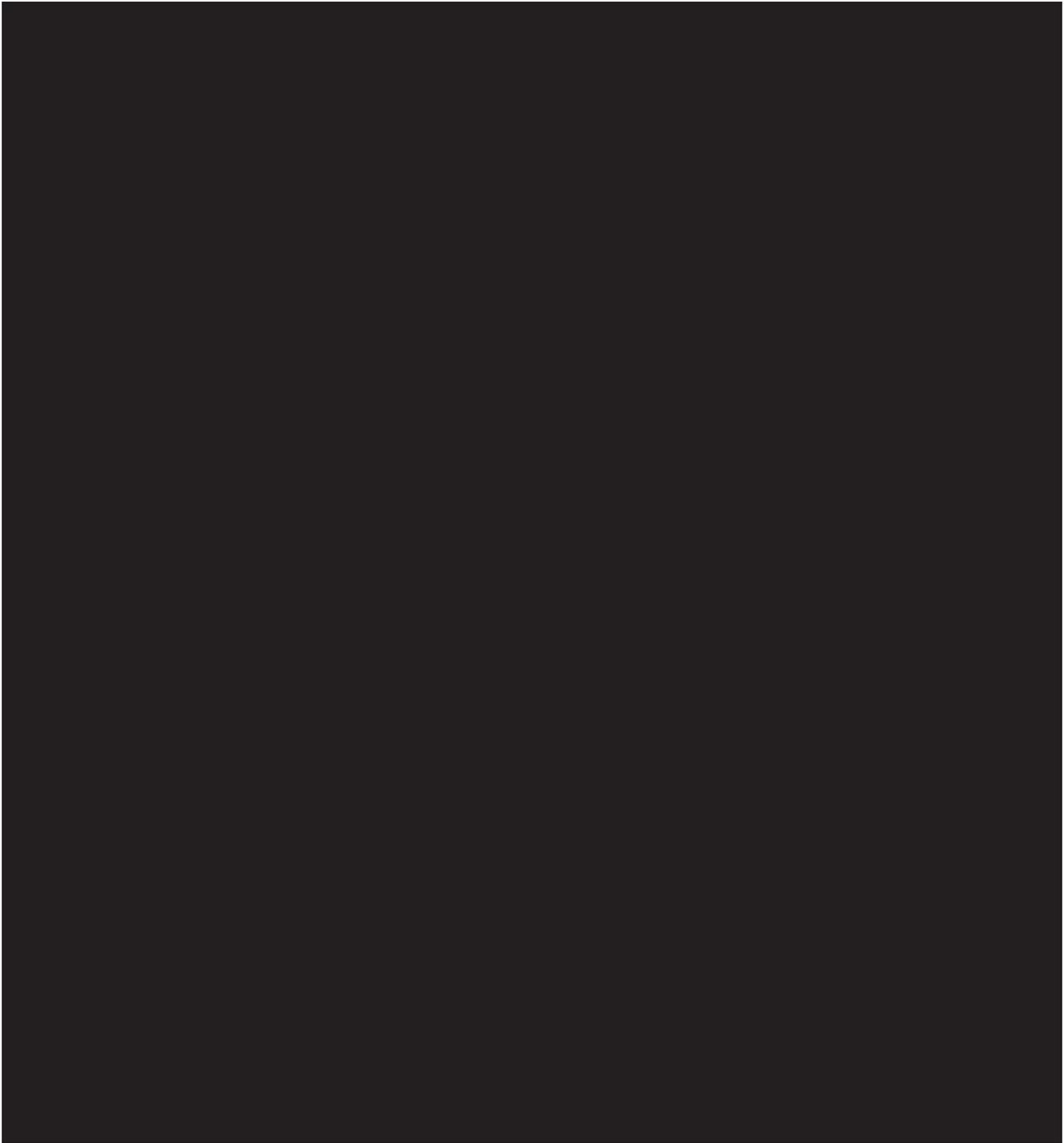
Resolution of this dispute also requires addressing two claim construction issues. First, Order No. 34 construed “gate structure” as a “feature comprising a transistor gate.” Order No. 34 at 55. Thus, a feature in an Accused Product that does not, somewhere along its length, function as a transistor gate is not a “gate structure.” *See* Order No. 34 at 54. Although Respondents’ claim construction briefs proposed use of the term “dummy gate” to describe such a feature, that proposed term was not construed because “the dispute over how to precisely define a ‘gate electrode feature’ that does not form a transistor gate at all” had been rendered moot by the withdrawal of previously-asserted patents. *Id.* Although that dispute remains moot, because the term “dummy gate” is not used in the 334 patent, a “gate structure” still must “form[] a gate structure over at least some of its length,” and a feature that otherwise appears to qualify as a gate structure, but does not because it does not form a transistor, will informally be referred to as a “dummy gate.” *Id.*

Second, Tela contends that not all gate gridlines in a region must possess gate structures, so long as at least seven gridlines with gate structures can be identified. *See* CRB at 16 (an eighth gridline without a gate structure is “immaterial”). This is a question of claim construction that was not addressed in Order No. 34. The briefing on this point is sparse; Tela’s only real argument is that its proposed construction must be proper because otherwise the embodiments shown in figures 5 and 14 of the 334 patent would be excluded. *See* CRB at 16. But these figures do not themselves match a host of other claim limitations, and patentees have the freedom to draft claims covering different embodiments. *See* RRB at 9-10 (citing *Intamin Ltd. v. Magnetar Techs. Corp.*, 483 F.3d 1328, 1337 (Fed. Cir. 2007)). Accordingly, the claim language “each gate gridline has at least one gate structure positioned thereon” is accorded its plain and ordinary meaning: each gate gridline within an identified region must have at least one gate structure positioned thereon.

[REDACTED]

Given these constructions, and with respect to the Intel 14nm Products, Respondents argue “[f]or every 14nm cell Dr. Foty identifies, there is an alleged gridline that Dr. Foty numbers and relies on, but that [REDACTED] do not form transistor gates.” RIB at 22 (citing RX-0014C at Q/A 242-245; CDX-0008C at *16-21; CDX-0009C at *14-20). Based on the numbered annotations Dr. Foty provides and relies on to show how the limitation is met in each cell (*see* CX-1144C at Q/A 1495-1500; CDX-0009C at *14-19), some of the gridlines do include [REDACTED]. This is shown in the cells below where there is no yellow or green substrate region on both sides of the orange structures (*see, e.g.*, CX-1144C at Q/A 267-269; RX-0014C at Q/A 230) on a numbered line:





[REDACTED]

[REDACTED]

Thus, these cells do not meet the limitation. The remaining cells for the Intel 14nm Products do not suffer from this problem and therefore do meet the limitation; this conclusion applies to [REDACTED] (CDX-0009C at *15) and [REDACTED] (CDX-0009C at *16).

Accordingly, the following cells from the Intel 14nm Products have not been shown to meet this limitation: [REDACTED] Dr. Foty's demonstratives indicate the latter three cells comprise the entirety of cells for the Goldmont, Goldmont Plus, Ice Lake Chipset, and Cannon Lake Chipset products. CDX-0012C at *25-26. Thus, the Accused Products including these models do not infringe. The remaining Intel 14nm Products use one or both of [REDACTED] so they meet the limitation.

With respect to the Intel 10nm Products, Respondents' and the Staff's argument that Intel's use of [REDACTED] "results in lines without any gate structures positioned thereon" (RIB at 47 (citing RX-0008C at Q/A 15; RX-0014C at Q/A 229-

[REDACTED]

331; RX-0157 at *10)) is not persuasive. Here, helpfully, Respondents and Dr. Subramanian are more specific and provide demonstratives for each of the three 10nm cells, showing the pertinent

[REDACTED] These demonstratives, however, do not match the gridlines Tela and Dr. Foty identify and rely on to show the limitation is met (CX-1144C at Q/A 2420-2422 (citing CDX-0011C at *10-12)) as shown below:



⁴ The demonstrative for this particular limitation for cell [REDACTED] omits the numerical annotations 1-9, but the identified gridlines are the same. *See* CDX-0011C at *10.

[REDACTED]



Tela's identification of gridlines in the [REDACTED] cell appears to include, and [REDACTED] See CDX-0011C at *7, 10; see also CDX-0012C at *38 (citing CPX-0237C at *3). Thus, this cell may not meet the limitation, if the layout files are taken at face value. But Dr. Auth and Dr. Subramanian testified unequivocally that the Intel 10nm Products [REDACTED] RX-0008C at Q/A 32, 135 (" [REDACTED] [REDACTED]"); RX-0014C at Q/A 229-242; RX-0157 at *10. Therefore, what appears to be a [REDACTED] must instead be a gate structure. And although the image of this cell includes structures (on the right hand side) that, if considered part of the claimed "region," do not meet the claim limitation at issue, they are clearly not part of the nine gridlines Dr. Foty identifies in his analysis; nothing in Dr. Foty's testimony suggests that the "region" he analyzes is the entirety of the cell. See CDX-0011C at *4, *7, *10; CX-1144C at Q/A 2397 (the cell "shows a region of a semiconductor ship that includes gate structures," which have been "highlighted"). In other words, the dummy gates are extraneous to the claimed "at least seven gate gridlines" and Dr. Foty was not inconsistent in his identification of the "region" across

[REDACTED]

RIB at 40 (citing RX-0014C at Q/A 176). Respondents explain more specifically, “it is undisputed that the [REDACTED]

[REDACTED]”
RRB at 11-12 (citing Hr’g Tr. at 312:8-21; RX-0008C at Q/A 160-163; RX-0014C at Q/A 170).

As noted, the Staff alludes to a similar dispute by identifying the specific claim language “contact structures” as limitation 1[i] (SIB at 39) and then asserting limitation 1[i] is not met (*id.* at 42), although its discussion focuses on a lack of “overlap.”

This claim element was not previously construed. *See* Order No. 34 at 61. The Federal Circuit has held that separate claim elements do not necessarily require separate structures within an accused device or the prior art when there is nothing in the claims or specification to suggest such a restriction. *See Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231-32 (Fed. Cir. 2011); *Linear Tech. Corp. v. Int’l Trade Comm’n*, 566 F.3d 1049, 1055 (Fed. Cir. 2009) (“We agree with the Commission’s construction of ‘second circuit’ and ‘third circuit,’ defining the terms broadly to not require entirely separate and distinct circuits. Indeed, there is nothing in the claim language or specification that supports narrowly construing the terms to require a specific structural requirement or entirely distinct ‘second’ and ‘third’ circuits. Rather, the ‘second’ and ‘third’ circuits must only perform their stated functions.”). Nothing in the 334 patent suggests “contact structures” cannot be integral to or formed at the same time as the “first-metal structures,” or that there would be an advantage to keeping them distinct. Respondents have certainly not explained, with reference to either the claims or the specification, why the restriction is appropriate. Therefore, this element is construed as including both structures integral to the first-metal structures and separate from the first-metal structures, so long as they contact the gate structures. And because the evidence shows that the [REDACTED] structures, which are formed [REDACTED]

[REDACTED]

[REDACTED] the higher-up, linear “first-metal structures,” do contact the gate structures, they qualify as contact structures. Accordingly, the limitation is met in the Intel 10nm Products.

- e. **Each of the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact**

Fifth, Respondents and Staff dispute whether “each of the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact” is met in the Intel 10nm Products. RIB at 40-46; SIB at 39-42. No party disputes the limitation is met in the Intel 14nm Products.

For this limitation, and the Intel 10nm Products in particular, Tela contends Intel’s design rules “[REDACTED]” CIB at 47 (citing CPX-0341C at 5827-28; CX-1144C at Q/A [REDACTED])” CIB at 47 (citing CPX-0341C at 5827-28; CX-1144C at Q/A 315-319, 1964, 1983, 2497-2498; CPX-0030C at 1493; CX-0662 at *7, 9). Tela adds:

An example of a [REDACTED] overlapping both edges of the top surface of the gate structure is illustrated in teardown images of an Intel 10nm Product (Intel i3-8121U), which show a cross-section and top view of a [REDACTED] further confirming that this claim element is met. (CX-1144C (Foty) at Q/A 1990-95, 2497-98; CDX-0010C.27-28.)

Id. More specifically, Tela argues “[n]othing in claim 1 requires the bottom surface of the contact structure to overlap the edges of the top surface of the gate structure. And the [REDACTED] [REDACTED] and as such is ‘sized to overlap both edges of the top surface of the gate structure’ as required by the claims.” CRB at 18. Tela shows this upper-edge overlap in the below images:

[REDACTED]

[REDACTED]

CRB at 49. Tela rejects a claim interpretation which would require “the bottom surface of the contact that physically contacts the top of the gate must overlap the edges of the gate.” *See id.* at 49-50.

In opposition, Respondents argue its [REDACTED]

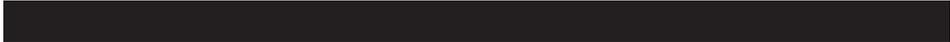
[REDACTED]

[REDACTED] RIB

at 41 (citing RX-0008C at Q/A 160, 161); RRB at 12. Thus, according to Respondents, there is no overlap as shown in teardown images:



RIB at 42-43 (citing RX-0014C at Q/A 168; JX-0220 at *1). Respondents argue Tela’s reliance on layout file shapes cannot overcome the actual structure of the fabricated device (*see* RIB at 43; RRB at 12), and Tela’s expert admitted that the green-box annotations in a demonstrative showing the required overlap between the first-metal layer and the gate structure were misleading (RIB at 44 (citing CDX-0010C at *28; Hr’g Tr. at 310:15-311:13, 305:9-313:1, 468:1-469:6)), as shown below:



(RIB at 45). Respondents contend the top of the yellow “T” shape in the above image cannot fulfill the requirement for “overlap” because “the claim language addresses overlap at the top surface of the gate—where the structures contact—not some flare-out of a broader Metal-0 structure far above the contact interface, as Dr. Foty argues.” *Id.* (citing Hr’g Tr. at 312:22-313:1; 334 patent at 21:26-37). Respondents suggest Dr. Foty admitted at cross-examination that the claimed concept addresses the interface between the top of the gate and the bottom of the contact structure” (*id.* at 45-46 (citing Hr’g Tr. at 470:2-471:4)) and that the position was never properly noticed by Tela (RRB at 13-14 (citing CX-1144C at Q/A 318, 2492-99)). The Staff concurs with Respondents on all these points. *See* SIB at 39-42; SRB at 11-14.

Resolution of this dispute requires construction of claim language not previously interpreted. Under a plain reading of the claim, and as supported by the specification, the “overlap” must actually be at the interface between the gate structure and the contact structure. The claim states “each of the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact.” 334 patent at cl. 1. Clearly the emphasis here is on contact (hence the name “contact structures”) with the “top

[REDACTED]

surface” of the gate structure, *i.e.*, the interface between two dissimilar materials. A person of ordinary skill would surely understand the “overlap” to occur at this location, namely, the point of contact. The specification reinforces this view, stating, “it should be appreciated that in the present invention, the gate electrode contact 601 is oversized in the direction perpendicular to the gate electrode feature 501 to ensure overlap between the gate electrode contact 601 and the gate electrode feature 501.” *Id.* at 17:50-55. At the hearing, Dr. Foty acknowledged misalignment between these two structures was a concern. *See Hr’g Tr.* at 470:2-471:1. Such misalignment can be seen in, for example, the red annotation to teardown imagery of one of the DI Products:



CX-1144C at Q/A 2652 (citing CX-0684 at -56335-51 (annotated)). It is clear that overlap at the point of interface would help ensure contact and alleviate misalignment between the structures. Tela’s proposed T-shape for “overlap” would not do the same.

With this construction in mind, the evidence indisputably shows the limitation is not met in the actual Intel 10nm Products. As Tela itself explains, after holes are patterned to expose the top surface of the gates, [REDACTED]

[REDACTED]

[REDACTED] CIB at 44 (citing CX-1144C at Q/A 315-320; RX-0014C at Q/A 167).

[REDACTED]

Teardown imagery shows this results in coextensive (*i.e.*, no overlap) contact at the interface between the contact structure and the gate structure, as presented above. *See, e.g.*, RX-0014C at Q/A 168; JX-0220 at *1. Thus, the limitation is not met in the Intel 10nm Products.

2. Claim 2

For reference, claim 2 of the 334 patent requires:

2. [2a] The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures positioned in accordance with a second-metal horizontal grid, the second-metal horizontal grid including at least eight second-metal gridlines,

[2b] each second-metal structure in the region having at least one adjacent second-metal structure positioned next to each of its sides in accordance with an x-coordinate spacing of less than or equal to 193 nanometers, each second-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline,

[2c] wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure positioned thereon, wherein each pair of second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap,

[2d] wherein the second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the gate structures.

334 patent at cl. 2. Claim 2 is not identified as in dispute by Respondents. *See generally* RIB.

The Staff, however, asserts that claim 2’s recitation of “grid(s)” and “gridlines” invokes the same grounds for non-infringement as discussed above in connection with claim 1. *See* SIB at 45.

Although it is unclear to which “grid” limitation of claim 1 the Staff refers—“gate horizontal grid” or “first-metal grid”—as determined above the linear and parallel positioning of both corresponding elements (gate and M0 layers) within the Accused Products satisfies “positioned in accordance with a . . . grid.” With no other elements of claim 2 in dispute, the Accused Products which infringe claim 1 have also been shown to meet the limitations of claim 2 by the testimony of Dr. Foty. CX-1144C at Q/A 1651-1709, 2527-2567.

3. Claim 5

For reference, claim 5 of the 334 patent requires:

5. The semiconductor chip as recited in claim 2, wherein the at least six contact structures are positioned in accordance with a contact vertical grid, the contact vertical grid including contact gridlines extending in the x-direction, each of the at least six contact structures positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six contact structures positioned to also extend lengthwise in the x-direction in a substantially centered manner along a corresponding first-metal gridline.

334 patent at cl. 5. Claim 5 is not identified as in dispute by Respondents. *See generally* RIB. Again, though, the Staff asserts that claim 5’s recitation of “grid(s)” and “gridlines” invokes the same grounds for non-infringement as discussed above in connection with claims 1 and 2. *See* SIB at 45. And as with claims 1 and 2, although it is unclear from which of the two “grid” limitations the Staff is incorporating its argument, the Accused Products which infringe claim 1 have also been shown to meet the limitations of claim 5 by the testimony of Dr. Foty. CX-1144C at Q/A 1710-1730, 2568-2578.

4. Claim 15

Claim 15 of the 334 patent requires:

15. The semiconductor chip as recited in claim 1, wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of at least one transistor within the region of the semiconductor chip has a substantially rectangular shape.

334 patent at cl. 15. Several disputes exist between the parties concerning whether Tela has sufficiently shown the Accused Products meet the limitations of the claim.

a. Diffusion Region

First, Respondents and Staff dispute that the Intel 14nm Products or the Intel 10nm Products have a “diffusion region.” RIB at 22-39, 49; SIB at 46-52.

[REDACTED]

Tela contends “[i]n the Intel 14nm Products, each transistor in the region is formed in part by a corresponding diffusion region, as evidenced by the diffusion region layout shapes that define the location of source and drain regions of the NMOS and PMOS transistors.” CIB at 56 (citing CX-1144C at Q/A 253-263, 284-288, 392-393, 951-988, 1731-1749; JX-0210C at *218, 225; CPX-0096C at 3554-3555). Tela explains “Intel uses a process [REDACTED] [REDACTED] to form the source or drain of a transistor.” *Id.* at 57 (citing CX-1144C at Q/A 255, 258-259, 953, 1731-1734; RPX-1997 at 307, 319; RPX-2021 at 1048, 1060; Hr’g Tr. at 450:25-452:19; Hr’g Tr. at 450:25-252:19, 649:2-652:12). Tela continues:

[REDACTED]

(CX-1144C (Foty) at Q/A74; *see also* Tr. (Foty) at 446:6-17.)

Id. Tela claims this meets Order No. 34’s construction for “diffusion region” as “selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor” because “the source and drain regions are heavily doped semiconductor regions occupy[ing] a portion of the area or region specified by a corresponding diffusion layout shape.” *Id.* (citing, *inter alia*, CX-1144C at Q/A 267, 972-974, 1354-1362). Tela argues “the construction is silent as to how impurities are introduced” and suggests [REDACTED] is one such technique. CRB at 20 (citing CX-1144C at Q/A 61; Hr’g Tr. at 489:8-490:11), 21 (Hr’g Tr. at 237:8-238:3, 649:2-650:3); RX-1664C at 138:15-25), 22 (citing CX-1144C at Q/A 61). Tela

[REDACTED]

asserts that “if the source and drain regions were separate from the substrate, charge carriers would not be able to flow from the source and drain regions, rendering the transistor inoperable.” CRB at 22 (citing CX-1144C at Q/A 69-74).

Tela observes that contemporaneous Intel documents “[REDACTED]” (CIB at 58 (citing Hr’g Tr. at 652:6-12, 654:3-12), 62 (citing CX-1144C at Q/A 127, 257, 267; CXP-0497C; CPX-0341C; Hr’g Tr. at 450:8-451:14); *see* CRB at 19) and “[a]s recently as 2017, [REDACTED]” (CRB at 212 (citing JX-0329 at *1, 3; Hr’g Tr. at 669:2-670:9)). Tela also argues that after the source and drain regions are [REDACTED] [REDACTED]” CIB at 58 (citing Hr’g Tr. at 454:8-24), 63; CRB at 23 (citing Hr’g Tr. at 452:20-454:7; RPX-1997C at 308; RPX-2021C at 1048, 1063).

Should these [REDACTED] sources and drains not be found to literally meet “diffusion region,” Tela contends they meet it under the doctrine of equivalents. *See* CIB at 60-61; CRB at 24-27. Tela claims the differences between Intel’s [REDACTED] regions and “diffusion regions” are both insubstantial and substantially the same in function, way, and result. *See* CIB at 60-61 (citing CX-1144C at Q/A 875-988), 63-66; CRB at 24-27. And Tela contends the Intel 10nm Products are created by the same process, and thus infringe for the same reasons as the Intel 14nm Products. *See* CIB at 58-59.

In its reply brief, Tela appears to challenge the notion that “diffusion region” is limited to the exact structures which make up the source and drain of a transistor:

Respondents suggest that Dr. Foty’s reliance on the n-diffusion and p-diffusion layout shapes is irrelevant to the ALJ’s construction of “diffusion

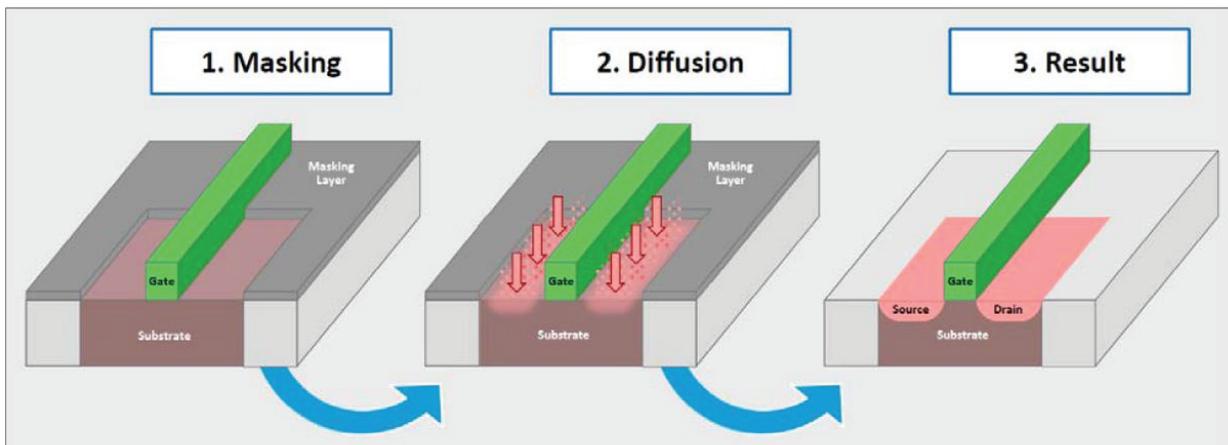
region” because it “refers to the source or drain of the transistor, not to a layout shape.” (RIB at 29.) Respondents appear to suggest that the ALJ’s construction requires an exact correspondence between the area where the impurities are introduced and the area where the source and drain are formed. (See *id.* at 29-30.) There is no such requirement. The ALJ defined “diffusion region” as the portion (*i.e.* region or area) of the substrate where impurities are introduced and source or drain regions are formed as a result. (Order No. 34 at 56.) Respondents acknowledged that [REDACTED]

[REDACTED] and sources and drains are formed within those areas. (RIB at 30; JX-0329.0001, 3; see also Tr. (Auth) at 669:2-670:9.) This establishes that the ALJ’s construction of “diffusion region” is met.

CRB at 20-21.

In opposition, Respondents argue that [REDACTED] cannot meet the construction for “diffusion region” given in Order No. 34: “selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor.” Put simply, Respondents contend the substrate in the Accused Products [REDACTED]

[REDACTED] RIB at 22, 26 (citing, *inter alia*, RX-0014C at Q/A 90-93, 100; RPX-1997C at *316-319; RX-0008C at Q/A 83), 31 (citing Hr’g Tr. 249:7-18, 661:16-17), 49. Respondents provide the following two diagrams showing this difference:



(RIB at 24 (citing RDX-0016C at *44; RX-0014C at Q/A 83-85; RX-0008C at Q/A 59-60));

[REDACTED]



(*id.* at 25 (citing RX-0008C at Q/A 62-70; RPX-1997C at *316; Hr’g Tr. at 235:19-236:2, 241:10-242:18)). Respondents also provide the following teardown image showing the bulbous shape of the epitaxially grown material:



RIB at 32 (citing RX-0008C at Q/A 75; PRX-2021C; Hr’g Tr. at 743:3-10).

Respondents claim “[f]orming sources/drains by [REDACTED]

[REDACTED]—was a critical innovation.” RIB at 26.

Respondents explain the innovation was needed to enable Intel’s three-dimensional FinFET source

[REDACTED]

and drain structures because: 1) [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] See generally RIB at 26-29 (citing, *inter alia*, RX-0008C at Q/A 62, 73-79; Hr’g Tr. at 254:2-5). For these technical reasons, Respondents argue, the [REDACTED] sources and drains cannot be deemed equivalent to or interchangeable with “diffusion regions,” either. See RIB at 33-39 (citing, *inter alia*, Hr’g Tr. at 236:12-238:19, 253:6-255:21, 737:16-742:3, 1114:15-19; RX-0008C at Q/A 75-83; RX-0014C at Q/A 117-118; *Freedman Seating Co. v. Am. Seating Co.*, 420 F.3d 1350, 1361 (Fed. Cir. 2005); *Minebea Co. v. Think Outside, Inc.*, 159 F. App’x 197, 204 (Fed. Cir. 2006)). Respondents claim “diffusion region” is a “meaningful structural and functional limitation of the claim,” and the doctrine of equivalents cannot be used to erase it” (RIB at 35 (citing *Conopco, Inc. v. May Dep’t Stores Co.*, 46 F.3d 1556, 1562 (Fed. Cir. 1994))) and point out the [REDACTED] regions are subject to their own issued patent (*id.* at 38 (citing RX-0167; RX-0014C at Q/A 122-123; *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 493 F.3d 1368, 1379-80 (Fed. Cir. 2007))). Respondents also contend the “doctrine of ensnarement” precludes application of the doctrine of equivalents for this limitation, claiming that since they raised it as a defense, the burden lies with Tela to “propose a hypothetical claim and prove that this claim did not ensnare the prior art”—a burden they have not and cannot meet with no expert testimony on the subject. *Id.* (citing *G. David Jang, M.D. v. Bos. Sci. Corp.*, 872 F.3d 1275, 1287 (Fed. Cir. 2017)).

As to Tela’s evidence, Respondents argue n-diffusion and p-diffusion layout shapes cannot meet the limitation, as the ordered construction refers to the source and drain of a transistor, which

[REDACTED]

the shapes are not—as acknowledged by Dr. Foty. RIB at 29-30 (citing Hr’g Tr. at 227:20-228:21). Additionally, Respondents explain [REDACTED] and “does not indicate the actual use of diffusion in the layout shape area, and certainly not that diffusion is used to form the sources/drains.” *Id.* at 30 (citing RX-0008C at Q/A 89-91). Respondents also dispute Dr. Foty’s opinion that any material electrically connected to the substrate can be considered “substrate” (*see id.* at 30-31) and argue his opinion is largely conclusory (*see* RRB at 38-39 (citing CX-1144C at Q/A 976)).

Finally, Respondents address Tela’s theory of [REDACTED]

[REDACTED] with the following:

Tela raises a new argument for the first time in its Post-Hearing Brief that Intel somehow infringes because it uses [REDACTED]

[REDACTED] Tela’s attempt to argue infringement based on this hypothetical unintentional by-product is neither timely nor credible, and it underscores the weakness of Tela’s original theories. As a preliminary matter, because Tela did not raise this infringement theory until its Post- Hearing Brief, the theory has been waived. G.R. 13.1

RRB at 22. If the argument is not deemed waived, Respondents argue the un rebutted testimony in the record is that no diffusion takes place. *See id.* at 23-24 (citing RX-0008C at Q/A 98; Hr’g Tr. at 970:13-971:2).

The Staff agrees with Respondents’ non-infringement positions, in both the literal and equivalence contexts. *See* SIB at 46-52, 56-58; SRB at 15-17, 18-20. The Staff summarizes, “[s]imply put, [REDACTED] process does not introduce impurities into the substrate to form sources or drains” (SIB at 50), and views a lack of interchangeability as precluding a finding of equivalence (SRB at 19).

[REDACTED]

The limitation is not literally met. The ordered construction for “diffusion region” is “selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor.” Order No. 34 at 56. The parties’ proposals for this term all included the phrase “portions of the substrate” or “defined in the base substrate.” *See id.* at 55. Within all Accused Products, Tela has identified the [REDACTED] source and drain structures, located along the fins created by FinFET processes, as the “diffusion region[s].” *See* CIB at 57 (“The diffusion regions in the Intel 14nm Products meet the ALJ’s construction of ‘diffusion region.’ The [REDACTED] source and drain regions in the Intel 14nm Products are ‘selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor’”); *see* CRB at 19.

The record is clear, however, that the [REDACTED] structures cannot fairly be considered “substrate.” The parties’ experts both describe how these structures are first created by [REDACTED]

[REDACTED] Dr. Foty testified:

The source and drain regions in the Intel 14nm and 10nm processors are formed [REDACTED]

[REDACTED]

CX-1144C at Q/A 255; *see* CX-1144C at Q/A 259, 392-393; CPX-0197C at -974-1043. Dr. Subramanian testified:

Starting back at Intel’s [REDACTED]

[REDACTED]

[REDACTED]

RX-0014C at Q/A 79; *see* RX-0014C at Q/A 87-97; RPX-2062C; RPX-2064C; RPX-1997C at -298-319; RPX-2021C at -11-60. The [REDACTED] is not a modification of existing material through the introduction of impurities, as required by the claim. Dr. Auth credibly explained that the “substrate” is simply that wafer material which is received from the wafer manufacturer:

Q. Are Intel’s [REDACTED] sources and drains a portion of the substrate?

A. No. Our [REDACTED] as opposed to modifying the substrate.

Q. Why don’t you consider [REDACTED] to be a portion of the substrate?

A. The substrate is the wafer we receive from the wafer manufacturer. Our [REDACTED]

RX-0008C at Q/A 81-82. This is a point on which Tela witness Mr. Gandhi agreed. RX-1662C at 103:17-22. Dr. Foty also described the growth as “a different way of creating a source/drain that’s *electrically connected* to the substrate” (Hr’g Tr. at 254:14-21 (emphasis added)) as opposed to the previously discussed means of modifying the substrate itself (*see generally id.* at 235:19-254:13).

Tela offers a number of arguments as to why the [REDACTED] should still be considered “substrate” [REDACTED] but none are persuasive. For

[REDACTED]

example, Tela characterizes the [REDACTED]” (CIB at 57 (emphasis added)), but the cited expert testimony from Dr. Foty (*id.* (citing CX-1144C at Q/A 67-72, 393, 423)) never describes it as such. Tela also claims that the [REDACTED] [REDACTED] (CIB at 57; CRB at 23), but this is not supported beyond the say-so of its expert (*see id.* (citing CX-1144C at Q/A 393, 423; Hr’g Tr. at 446:6-17); *see* CX-1144C at Q/A 425) and it is apparently disputed by Dr. Auth (RX-0008C at Q/A 80 (discussing [REDACTED]”). Moreover, [REDACTED] [REDACTED] As stated by Dr. Subramanian, “the claim construction requires introducing impurities into the substrate, not into a material that ‘matches’ the substrate.” RX-0014C at Q/A 107.

Relatedly, Tela’s claim that [REDACTED] must be present “because without it, charge carriers could [not] flow between the source and drain regions of the transistor, rendering it inoperable” (CIB at 57; *see* CRB at 22 (citing CX-1144C at Q/A 74) is beside the point. Even assuming this assertion is true, at most it implies that [REDACTED] source and drain regions have [REDACTED] not that they are part of that substrate.

Moreover, that “Intel’s technical witness and contemporaneous documents describe the portion of the substrate where impurities have been introduced using [REDACTED] [REDACTED] (CIB at 58; *see* CRB at 21-22) is immaterial. The source and drain regions, in actuality, are [REDACTED], regardless of Intel’s own terminology.

Lastly, Tela’s additional argument concerning a “[REDACTED] [REDACTED]

[REDACTED]

(*see, e.g.*, CIB at 58), is particularly revealing. The theory, if true, would avoid the substrate problem discussed above, because the “pre-existing portions of the fin” are indisputably substrate. But this contention was not disclosed in Tela’s pre-hearing brief and has been waived under Ground Rule 13.1. *Compare* CPB at 14, 36 (all mentions of [REDACTED]) *with* Hr’g Tr. at 452:20–454:24. Moreover, there is no evidence that any [REDACTED] causes the relevant region of the substrate to “form the source or drain of a transistor,” as required by claim 15. Order No. 34 at 56.

Accordingly, the Accused Products have not been shown to literally infringe because they literally lack the required “diffusion region(s).”

The limitation has been shown under the doctrine of equivalents, however. Admittedly, Dr. Foty’s testimony on equivalence under an “insignificant differences” test is insufficient. It largely consists of generalities about processes that would allegedly be understood as insignificantly different, only to conclude with “[t]he source and drain regions in the Intel 14nm processor are highly doped n-type or p-type regions, which is the same as the source and drain regions in a transistor fabricated using a standard CMOS process in 2005.” CX-1144C at Q/A 976. The opinion does not address on any technical level why those differences which might, and did, preclude literal infringement are insignificant. Accordingly, equivalence is not proven under this approach.

With respect to function-way-result analysis, Dr. Foty’s discussion is more substantial and, ultimately, persuasive. As determined above, the Accused Products do not literally infringe because their sources and drains are formed through the introduction of impurities via [REDACTED] [REDACTED]—and not into substrate as the limitation requires. *See* RX-0014C at Q/A 107, 119; RX-0008C at Q/A 65-71, 98. Thus, the issue is whether these latter sources and

[REDACTED]

drains, once created, are substantially the same in function, way, and result, as the former sources and drains.

Dr. Foty has persuasively explained how the functions of each type of source and drain are the same—to provide charge carriers in a transistor circuit. CX-1144C at Q/A 976. Respondents’ expert, Dr. Subramanian, seems to acknowledge this shared function but then focuses on differences which are not material to the analysis, particularly the use of the [REDACTED] sources and drains in three sided-fin applications as opposed to planar layouts. RX-0014C at Q/A 118. Respondents’ briefing similarly focuses too narrowly on attributes of Intel’s epitaxially grown structures that enable certain levels of performance, and then describes them as the “function.” See RIB at 36 (“[t]he function of Intel’s [REDACTED] sources/drains is to act as sources/drains specifically for FinFET transistors and to achieve strained silicon”).

Dr. Foty has also persuasively explained how the ways the functions are achieved are the same: “by including a [REDACTED] other than and in addition to those of the semiconductor material,” which are referred to as dopants or impurities. CX-1144C at Q/A 976. Respondents’ witnesses agree such impurities are introduced during [REDACTED] (albeit not introduced into the substrate). See RX-0014C at Q/A 107, 119; RX-0008C at Q/A 65-71. The record further shows these impurities are responsible for charge carrier creation by leaving electron “holes” in P-type semiconductors and providing extra electrons in N-type semiconductors. See CX-1144C at Q/A 69; RX-0014C at Q/A 119. Thus, the way involves different structures but is substantially the same.

Lastly, Dr. Foty has sufficiently explained substantially the same results from the functions, and ways of accomplishing those functions, between sources and drains formed from introducing impurities into an epitaxial growth and sources and drains formed from introducing impurities into

[REDACTED]

a substrate—namely, a functioning transistor. CX-1144C at Q/A 976. Respondents’ emphasis on the [REDACTED] [REDACTED] (see RIB at 37; RRB at 17-18) are all well taken; they lead to enhanced performance of the sources and drains, are no doubt necessary for smaller process nodes, and perhaps are entitled to separate protection under the patent laws.⁵ Respondents call these “critical differences” (RIB at 39), yet none actually differentiate the function of the [REDACTED] as it pertains to the claimed invention (*i.e.*, to serve as source or drain), the way in which that function is accomplished (*i.e.*, electron vacancies due to first type of impurity, electron surplus due to second), or the result (functioning transistor) from the ordered construction of “diffusion region.” Accordingly, the function-way-result test is satisfied.

Nor is doctrine of equivalents infringement precluded under ensnarement. True, “the burden of persuasion is on the patentee to establish . . . that the asserted scope of equivalency would not ensnare the prior art.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1323-24 (Fed. Cir. 2009); see *Intendis GMBH v. Glenmark Pharms. Inc., USA*, 822 F.3d 1355, 1363 (Fed. Cir. 2016). But Respondents have a burden of production to identify the prior art they contend is ensnared, and with sufficient specificity to identify what is in dispute. See *Intendis*, 822 F.3d at 1363 (“prior art introduced by the accused infringer [must be] assessed”). Respondents’ only effort to meet this burden is a single sentence in their opening brief, where they assert that the doctrine of equivalents “would improperly ensnare the prior art, including Intel’s prior art 45 nm process node.” RIB at 38. This is too vague to trigger Tela’s burden. It is also

⁵ It appears the patent granted to Intel that Respondents’ reference (RIB at 38 (citing RX-0167)) focuses on features other than the mere fact of epitaxial deposition (see RX-0014C at Q/A 122 (citing RDX-0016C at *58; RX-0167 at cl. 4)).

[REDACTED]

not clear that the Intel 45nm Products would even be ensnared because they lack other elements of the claim such as gate structures orthogonal to first-metal structures. *See, e.g.*, RX-0007C at Q/A 426, 610. Moreover, generation of a hypothetical claim, which Respondents contend Tela must do, is not the only method of demonstrating non-ensnarement. *See* RIB at 38; *see G. David Jang*, 872 F.3d at 1285 n.4 (“hypothetical claim analysis is not the only method” to evaluate ensnarement).

Accordingly, the “diffusion region” limitation is met in the Accused Products under the doctrine of equivalents.

b. Substantially rectangular shape

Second, Respondents and Staff allege that, should the Intel 14nm Products or the Intel 10nm Products have “diffusion region[s],” those regions have not been shown to have “a substantially rectangular shape.” RIB at 39-40, 49; SIB at 52-56. This claim element was not previously construed. *See* Order No. 34 at 48-50.

Tela’s position is that “[t]he identified regions have a substantially rectangular shape from a layout or top down view. This is evidenced by a top view illustration presented in Dr. Foty’s demonstratives at CDX-0009C pages 127-131.” CIB at 58 (citing Hr’g Tr. at 454:8-24; CX-1144C at Q/A 758-765, 1734), 59 (citing CX-1144C at Q/A 2578-2589; CDX-0011C at *72-74). Tela disputes that the “rectangular” shape can be evaluated from a side-perspective or vertical cross-section, as Respondents contend. CRB at 27-28 (citing Order No. 34 at 50). Tela also criticizes the Staff for alleging that, from a top-perspective, the source and drain regions are not rectangular. *See id.* at 28 (citing SIB at 54).

The limitation is not met. As defined in Order No. 34 and explained above, the “diffusion regions” of the claim must be a location within a substance (*i.e.*, the substrate) where the introduction of impurities causes the creation of a source or drain of a transistor. Even assuming

[REDACTED]

the [REDACTED] constitute the diffusion region, there is no evidence they are substantially rectangular from a top-perspective. *See, e.g.*, CDX-0012C at *8; CDX-0009C at *126-131. And Dr. Foty conceded he did not provide any opinions on this issue. Hr’g Tr. at 357:12-359:12, 389:13-391:22. Accordingly, this element is not satisfied by the Accused Products, and claim 15 overall has not been shown to be infringed by the Accused Products.

E. Domestic Industry – Technical Prong

According to Tela’s post-hearing briefing, the construction or use of the DI Products practices claims 29 and 30 of the 334 patent. *See* CIB at 66. For the reasons discussed below, I find Tela has not shown by a preponderance of the evidence that the DI Products practice the claims.

1. Product Representativeness

As noted above, the DI Products consist of multiple processors from non-party SAS, made with varying processes designated LPE, LPP, and LPC. Tela explains Samsung’s 14LPP and 14LPC processes are more recent variants of Samsung’s 14nm FinFET process based on Samsung’s 14LPE process (CIB at 69 (citing CX-1144C at q/A 2619-2622, 2684-2690; JX-0209; CX-0686C at *17)) and yet “[t]he differences between 14LPE, 14LPP, and 14LPC are not material to the technical prong analysis; the relevant features such as [REDACTED] [REDACTED] are consistent between the three” (*id.* at 66 (citing CX-1144C at Q/A 2627)). In support, Tela references, *inter alia*, a 14LPP [REDACTED] (*id.* (citing CX-0728C at *9)), 14LPC design manuals (*id.* at 67-68 (citing CX-1144C at Q/A 2663-2674, 2685)), and 14LPP advertisements which mention a “lower cost option, ‘without design rule changes or performance sacrifice’” (*id.* at 68 (citing CX-1614 at *1)).

Thus, according to Tela, “Samsung’s 14nm FinFET process variants are representative of one another and individually and collectively show that the Exynos Products practice the ’334

[REDACTED]

Patent claims 29 and 30.” CIB at 69. Tela also claims, more specifically, that the particular logic circuit it located within the Exynos 7420 model, and relies on for technical prong domestic industry, is a 2:1 multiplexer and so common that it “is almost certainly found in the other Exynos Products. *Id.* at 69-70 (citing, *inter alia*, CX-1144C at Q/A 2691, 2953-2965, 3272-3278; Hr’g Tr. at 668:9-669:1). Tela observes that a similar [REDACTED] [REDACTED] and argues Respondents and Staff ignore this industry practice of repeating transistor arrangements. *See id.* at 70 (citing CPX-0094C at -3546; CPX-0091C at -3533); *see also* CRB at 29-30 (citing CX-1144C at Q/A 2614-2694). Importantly, Tela takes the position that “Dr. Foty confirmed that the relevant features to his analysis of the Exynos 7420 (*e.g.*, rectangular gate shape, rectangular contacts, gate pitch) are found in the design rules for the subsequent Samsung 14LPP and 14LPC processes.” CRB at 29-30 (citing CX-1144C at Q/A 2653-2694).

In its reply brief, Tela views Respondents’ and Staff’s arguments on this issue as strawmen—*i.e.*, immaterial to the claims—akin to discussions of fin height and voltage types. CRB at 30 (citing RX-1144C at 2626-2629); JX-0209 at *3), 33 (“Respondents identify design rules allowing [REDACTED] But this too has no effect on the technical prong claim analysis.”). Tela argues, “[t]ellingly, Respondents and Staff never directly refute Dr. Foty’s analysis as to representativeness. Instead, they merely observe that that the design rules allow [REDACTED] without explaining how those rules are material to the technical prong analysis.” *Id.* at 32. In one example, Tela refers to a [REDACTED] [REDACTED] for Samsung’s “14nm processes” and argues that larger pitches, as Respondents suggest is possible, “would result in a larger, slower, more expensive chip that no longer qualified as ‘14nm.’” *Id.*

[REDACTED]

Respondents and the Staff challenge this representativeness. RIB at 49-59; SIB at 59-65. Respondents specifically note that besides the Exynos 7420, “Tela did not perform reverse engineering or obtain any technical discovery from Samsung on the Other DI Products,⁶ and therefore Tela has no evidence that they actually practice the claims.” RIB at 49; *see id.* at 56 (discussing Samsung manuals come from [REDACTED])

As to the particular logic circuit in the Exynos 7420 Tela has selected and claims is likely present in all other DI Products, Respondents view it as just “one specific configuration of 22 transistors in a chip with over a billion transistors” (*id.* at 50) and allege “Dr. Foty makes no attempt to show that this transistor configuration is present in any of the Other DI Products” (*id.* (citing RX-0014C at Q/A 439-4509)). Respondents contend Dr. Foty was misleading when he claimed to rely on SEM images for products other than the Exynos 7420 to determine physical layouts as “[t]here is no such reverse engineering of the Other DI Products in the record.” *See id.* at 57 (citing CX-1144C at Q/A 2629; RX-0014C at Q/A 497). Respondents emphasize that showing the particular 22-transistor configuration from the Exynos 7420 is present in the other DI Products is critical to certain claim elements, as opposed to claim elements which may be shown through design manuals; claim elements such as “29(g), 29(h), 30(h), and 30(i) of the ’334 patent and elements 27(m) and 28(m) of the ’523 patent.” RRB at 27-28.

As to the manufacturing processes 14LPE, 14LPP, and 14LPC, Respondents claim there is actually a fourth process, 14LPU, and within each, several different [REDACTED] [REDACTED] with “significant impact” on arrangement of transistors and structure dimensions. *See* RIB at 50 (citing RX-0014C at Q/A 428; JX-0209 at 3), 55. At a more basic

⁶ Respondents designate the S5E8890, S5E7880, S5E7570, S5E7870, and S5E7883 as the “Other DI Products.” RIB at 49.

[REDACTED]

level, Respondents argue the 14LPP and 14LPC design manuals Tela relies on “are ‘a set of parameters that specify certain geometric and connectivity restrictions’—they do *not* specify the actual design of the chip or configuration of the structures, which is what Tela must prove to show that the claims are practiced.” *Id.* at 51 (citing RX-0014C at Q/A 438). Respondents allege “Samsung has explicitly stated that its 14LPE process used to manufacture the Exynos 7420 has a different “transistor structure” than the 14LPP process used for two of the other chips, and Samsung has distinguished the 14LPP and 14LPC processes used for the Other DI Products as an improvement over the LPE process.” *Id.* at 52 (citing RX-0014C at Q/A 452-454; RX-0146 at *2; RX-0148 at *2). Respondents also point to different [REDACTED] [REDACTED] in the 14LPP and 14LPC processes than are found in the Exynos 7420. *Id.* at 53 (citing RX-0014C at Q/A 461-466, 470-478; CX-0727C at 135, 146; CX-0726C at 165).

In their reply brief, Respondents criticize Tela’s use of news articles to supplement the details found in the design manuals themselves (*see* RRB at 28-29) and observe that one article which Tela quotes is actually a comparison between LPP and LPC, and not between either with LPE (*see id.* at 29 (citing CX-1614 at *1)). Respondents also argue that the evidence regarding commonality of 2:1 multiplexers was based on “Mr. Becker’s non-objective testimony, with no foundation, especially as to Samsung chips.” *Id.* at 30 (citing Hr’g Tr. at 121:18-122:4). Respondents state flatly “[t]here is no evidence that the specific multiplexer identified in the Exynos 7420 was used in any of the Other DI Products” and add “[a] logic function by itself does not practice the claims—the logic circuit must be implemented into a semiconductor chip in a particular way.” *Id.* at 30 (citing RX-0014C at Q/A 501-507).

The Staff echoes many of Respondents’ points including the facts that “Tela did not obtain any technical discovery—no documents and no testimony—from Samsung or SAS. For example,

[REDACTED]

Samsung and SAS (and relevant third party Qualcomm) did not produce design layout files, mask layout files, or source code for any of the alleged DI Products” (SIB at 59; *see id.* at 61 (citations omitted)), and “Dr. Foty did not obtain or reverse-engineer any of the Other DI Products—consistent with his failure to obtain or personally reverse-engineer any of Intel’s Accused Products—to provide any direct evidence for those newer semiconductor chips” (*id.* at 61). The Staff, relying on testimony from Dr. Subramanian, claims “[t]he evidence shows that these three processes are materially different and were released at different times” and the designs are “quite different” as between the Exynos 7420 and other DI Products. SIB at 63 (citing RX-0014C at Q/A 435); SRB at 21 (citing RX-0014C at Q/A 435, 448-509). Thus, the Staff takes the position that Tela and its expert, Dr. Foty, were not able to conduct a proper “representativeness” analysis and cannot meet their burden here. SIB at 61.

Tela has not met its burden of showing representativeness. *Certain LED Lighting Devices, LED Power Supplies, and Components Thereof*, Inv. No. 337-TA-1081, Comm’n Op., at 10 (July 23, 2019) (holding the complainant “must show by a preponderance of the evidence that the products its expert analyzed are indeed representative of unanalyzed products.”) (citing *Certain Semiconductor Devices, Semiconductor Device Packages, and Products Containing Same*, Inv. No. 337-TA-1010, Order No. 77 (March 15, 2017)). Its collected evidence is of mixed nature and circumstantial at best. Tela obtained and analyzed an actual Exynos 7420 chip, but no corresponding LPE design rule document; and obtained LPP and LPC design rule documents for the remaining DI Products, but no chips. CX-1144C at Q/A 2683⁷; RX-0014C at Q/A 437; RDX-0016C at *176. Thus, Tela claims both: that the LPP and LPC design rule documents apply to the

⁷ Dr. Foty refers to an Exynos 7240 throughout his testimony, which I understand should be 7420.

[REDACTED]

Exynos 7420, and that the identified transistor cell within the Exynos 7420 applies to products made under LPP and LPC processes. *See* CIB at 67 (“In particular, the analysis is based on a teardown of the Exynos 7420, teardown reports for the Exynos 7420, and design rules for Samsung’s 14LPP and 14LPC processes. The two sets of design rules are substantially similar and the teardown analysis establishes that the relevant features of the Exynos 7420 conforms to both sets of design rules.”).

Tela has not sufficiently shown the latter of the two claims, *i.e.*, that the particular cell it identifies and relies on within the Exynos 7420 (CX-1144C at Q/A 2701, 3122) exists within the other five models of DI Products. This is critical because there are claim limitations which require an arrangement of transistors that would come from the chip designer’s chosen layout and not guaranteed to be present under the design rules. RRB at 27-28; *see* CRB at 30 (“The purpose of design rules is to tell layout designers what they can and cannot do – if the layouts fail to comply with these rules, they cannot be manufactured.”). Respondents refer to limitations 29(g), 29(h), 30(h), and 30(i) of the 334 patent, reproduced below:

[29g] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

[29h] wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a first gate structure forms both a gate electrode of the first transistor of the first transistor type and a gate electrode of the first transistor of the second transistor type.

(334 patent at cl. 29);

[30g] wherein each transistor within the region is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

[30h] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch[.]

(*id.* at cl. 30). Considering it is the patentee’s choice where to define the claimed “region” within an accused product, many other limitations could be added to this list including, for example, “wherein each gate gridline has at least one gate structure positioned thereon” and “a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region.” 334 patent at cl. 29. It is entirely unclear how these limitations, as just two examples and in addition to those identified by Respondents, could be shown merely by design rules as opposed to an actual fabricated design. Indeed, Dr. Foty does not rely on design documents to show them. *See* CX-1144C at Q/A 3133, 3215-3218.

Moreover, in a discussion of gate contact structures, Tela actually emphasizes, and thereby acknowledges, that the content of the LPP and LPC design manuals is not the basis for practicing the claim. Rather, the basis is the actual circuit arrangement found in the Exynos 7420 and imputed to the other chips:

Similarly, Respondents identify design rules allowing [REDACTED] [REDACTED] But this too has no effect on the technical prong claim analysis. The multiplexer identified by Dr. Foty does not include [REDACTED] (See, e.g., CDX-0013.14) Respondents’ identification of a potential non-practicing structure does not undermine Dr. Foty’s identification and analysis of a representative logic circuit in Exynos 7420.

CRB at 33.

[REDACTED]

Dr. Foty’s opinion that the particular transistor arrangement is present in the other DI Products is therefore little more than speculation. He starts with a general observation that the semiconductor industry relies on cell libraries and jumps to the conclusion that the particular Exynos 7420 region is “almost certain[ly]” in *any* other 14nm Exynos processor:

Q. How, if at all, do the SEM image that you reviewed relate to other Exynos processors?

A. Based on my review of the SEM images, it is my understanding that the Samsung Exynos 7240 was laid out using cells from a cell library. In the industry, it is typical to reuse verified cell libraries at a given process node – once it has been shown that the cell (as specified in the layout) can be successfully manufactured with the desired performance characteristics. As such, the circuits in the SEM images that I analyzed for the Exynos 7240 are almost certain to also be found in other Exynos processors manufactured using Samsung’s 14nm process.

CX-1144C at Q/A 2692. Tela implies additional testimony explains the connection beyond assertions of industry practice (*see* CRB at 29 (citing CX-1144C at Q/A 221-222, 2614-2694), 20 (“Respondents characterize the multiplexer cell as a ‘22-transistor arrangement’ and allege that there is no evidence it is found in the other Exynos Products. . . . These allegations, however, are controverted by the evidence of standard industry practice.”), 32-33 (citing CX-1144C at Q/A 2627, 2679-94)). But the testimony does not provide such additional support.

This is not enough on its own to satisfy Tela’s burden, and even if it was, the record contains contradicting evidence. For example, Tela’s identification of cells in the Accused Products shows that even with industry use of cell libraries (and the thousands of repetitions of cells within a certain model (*see* CIB at 70)), not all cells within a single process node are necessarily covered by the 334 patent’s claims. For instance: the [REDACTED] [REDACTED] cells for certain Intel 14nm Products (Broadwell, Sky Lake, Kaby Lake, Coffee Lake); the [REDACTED] cell for just one of the Intel 14nm Products (Cascade Lake); the [REDACTED] cells for another group of Intel 14nm



Products (Goldmont, Goldmont Plus); and, finally, the [REDACTED] cell for a last group (Ice Lake Chipset; Cannon Lake Chipset), as in the table below:

Intel 14nm Products	
<i>Product Family/Architecture</i>	<i>Associated Cells</i>
Broadwell; Sky Lake; Kaby Lake; Coffee Lake	[REDACTED] [REDACTED] [REDACTED]
Cascade Lake	[REDACTED]
Goldmont; Goldmont Plus	[REDACTED] [REDACTED] [REDACTED]
Ice Lake Chipset; Cannon Lake Chipset	[REDACTED]

See CDX-0012C at *25-26; RDX-0016C at *37-39. Under Dr. Foty’s reasoning on the DI Products, just one cell from this set of six could be representative of all the Intel 14nm Products. Clearly, however, this would not have sufficed as evidence of infringement.

Furthermore, Dr. Foty’s opinion is generally not as well supported for this topic. At one point in his testimony, he states he “completely disagree[s]” with Dr. Subramanian’s opinions on the materiality of Samsung’s 14nm process variants because, in part, he “was able to observe the physical layout of the devices through the SEM images, and confirm my understanding as to how those features are placed in view of the design rules.” CX-1144C at Q/A 2629. Yet in another portion he only mentions the Exynos 7420 as a physical product received and looked into:

[REDACTED]

Q. Did you analyze any particular Samsung Exynos products as part of your consideration of the technical prong of domestic industry requirement?

A. Yes, in forming my opinions regarding the technical prong of the domestic industry requirement, I analyzed the Samsung Exynos [7420] processor.

Q. What is the Samsung Exynos [7420] processor?

A. The Samsung Exynos [7420] processor is a processor fabricated using Samsung's LPE Process.

Q. How did you perform your analysis of the Samsung [7420] processor?

A. I analyzed teardown images of a Samsung Exynos processor, such as SEM images, which is fabricated using Samsung's LPE process. I also considered documents regarding the Samsung Exynos products such as the design rules we discussed earlier.

CX-1144C at Q/A 2680-2682. On this point, Respondents argue, and Tela does not dispute, that "Tela identifies—and its expert relies on—such images only for the Exynos 7420. . . . There is no such reverse engineering of the Other DI Products in the record." RIB at 57 (citing RX-0014C at Q/A 497).

As to other evidence, Tela's briefing refers to testimony on the extreme commonality of 2:1 multiplexers (CIB at 69; CRB at 30), but Respondents are persuasive when they note "a logic function by itself does not practice the claims—the logic circuit must be implemented into a semiconductor chip in a particular way. Indeed, there are a number of well-known 'circuits' that implement a 2:1 multiplexer, as well as a number of known implementations of a 2:1 multiplexer into a semiconductor chip that do not practice the DI claims" (RRB at 30-31 (citing, *inter alia*, RX-0014C at Q/A 500-507); *see* Hr'g Tr. at 1018:14-1019:21). Dr. Foty has not even attempted to refute this point.

In sum, the actual transistor arrangement within a chip is critical to satisfaction of the claims. Tela has no direct evidence showing the identified transistor arrangement of the Exynos

7420 is present in the other DI Products, however, and the circumstantial evidence regarding industry practices is particularly weak.

Accordingly, Tela has not shown the Exynos 7420 is representative of the other DI Products (S5E7570, S5E7870, S5E7880, S5E7883, and S5E8890) such that practice of the claims of the Asserted Patents by the Exynos 7420 suffices for all. Nevertheless, the following discussion of particular claim limitations assumes all products are represented by the Exynos 7420.

2. Disputed Claims

Respondents contest Tela's alleged practice of claims 29 and 30. *See* RIB at 59-62. The Staff takes the same position. SIB at 65-67. Tela has not shown practice of either claim.

a. Claim 29

For reference, claim 29 of the 334 patent requires:

29. [29a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon,

[29b] wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[29c] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type,

[29d] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[29e] a number of contact structures formed within the region of the semiconductor chip, wherein each gate structure that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding contact structure having a substantially rectangular shape, wherein each contact structure that contacts a given gate structure that forms any transistor gate electrode does not contact another gate structure, wherein each contact structure having a corresponding length greater than or equal to a corresponding width is oriented to have its corresponding length extend in an x-direction, wherein each contact structure that contacts a corresponding gate structure is positioned to overlap at least one edge of the corresponding gate structure,

[29f] wherein each transistor within the region is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

[29g] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

[29h] wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a first gate structure forms both a gate electrode of the first transistor of the first transistor type and a gate electrode of the first transistor of the second transistor type.

334 patent at cl. 29 (annotated). Several disputes exist between the parties concerning whether Tela has sufficiently shown the DI Products meet various limitations of the claim. These are addressed below. In view of the testimony of Dr. Foty that the DI Products practice those remaining limitations which are not in dispute, the DI Products have been shown to practice them as alleged. *See* CX-1144C at Q/A 3127-3290; CIB at 70-73.

i. Gate structures positioned in accordance with a gate horizontal grid

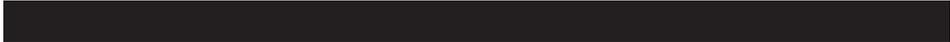
First, Respondents and Staff dispute that “gate structures positioned in accordance with a gate horizontal grid” is met in the DI Products. RIB at 62; SIB at 65-67.

For this limitation, Tela alleges:

[T]he Samsung 14LPP and 14LPC design manuals specify [REDACTED] [REDACTED] (CX-1144C (Foty) at Q/A 2786-96, 2823-25; CX-0727C.117, 120, 128, 132-33; CX-0726C.137, 156, 161-62.) Teardown analysis of the Exynos 7420 further show that the Exynos Products meet this claim limitation. (CX-1144C (Foty) at Q/A 3128-35; CDX-0013C.47-50; *see also* JX-0215.9-14.)

CIB at 70-71. In particular, Tela alleges Samsung’s use of [REDACTED] results in the positioning of gate structures in accordance with a grid, and provides the following teardown image in support:





CRB at 35 (citing JX-0215 at *9). Tela claims “[t]his positioning and orientation is also consistent with the requirements of the 14LPP and 14[LPC] design rules.” *Id.* (citing CX-1144C at Q/A 2642, 2671-2672, 2786-2793; CX-0726C at *156, 159, 177; CX-0727C at *128, 130, 146).

In opposition, Respondents argue “Tela . . . offers no documents, testimony, or any other evidence describing Samsung’s fabrication stage at all, let alone establish that any such gridlines were used during fabrication.” RIB at 62 (citing RX-0014C at Q/A 625-636); RRB at 33. The Staff argues similar points, claiming “Tela offers no evidence of any grid or gridlines, projected or otherwise, used during Samsung’s fabrication process, and has failed to prove that this limitation is met for that reason alone.” *See* SIB at 66; SRB at 23. The Staff asserts no equivalence has been shown, let alone alleged, for this element either. *See* SIB at 66-67; SRB at 23.

The limitation is met, under the same reasoning as applied to the Accused Products. Teardown images of the Exynos 7420 provided by Dr. Foty, reproduced above and below, show an unmistakable linear and parallel arrangement of gate structures:

[REDACTED]

[REDACTED]

CDX-0013 at *47 (citing CX-0723C). The most reasonable inference to draw is that these structures were positioned in accordance with a pre-planned grid (*i.e.*, not happenstance) during fabrication—despite Respondents’ and the Staff’s complaints over a lack of documentary or testimonial evidence. The proof is in the final product. Further, as discussed above in connection with the Accused Products, no actual, observable, projection of a grid is required. Accordingly, the DI Products practice this limitation.

ii. Diffusion regions

Second, Respondents and the Staff dispute that the DI Products have any “diffusion region[s].” RIB at 60; SIB at 67-71.

For this limitation, Tela notes that the Exynos Products use FinFET technology, and “design manuals, for example, show that the Exynos Products include an [REDACTED] [REDACTED] diffusion regions.” CIB at 72 (citing CX-1144C at

[REDACTED]

Q/A 2931-2936; CX-0727C at *38, 138, 141; CX-0726C at *46, 168, 171). In its reply brief, Tela highlights 14LPC and 14LPP design rules which, again, refer to the [REDACTED] as a diffused or diffusion region:

[REDACTED]

(CRB at 33 (citing CX-0726C at *46; CX-0727C at *38));

[REDACTED]

(*id.* (citing CX-0726C at *104; CX-0727C at *85)). Tela reasons, “[a]s such, a POSITA would understand that [REDACTED] source/drain regions in Exynos Products are diffusion regions.” *Id.*

As with the Accused Products, [REDACTED] and therefore not “substrate” as literally required by the construction of “diffusion region.” It does appear, however, that Tela asserts [REDACTED] source/drain regions are diffusion regions” for the DI Products under the doctrine of equivalents. *See* CRB at 33 (citing CRB at 19-28). And also as with the Accused Products, the evidence supports this assertion, so the DI products practice this limitation.

iii. Substantially rectangular shape

Third, Respondents and Staff argue that, should the DI Products have “diffusion region[s],” they have not been shown to possess “a substantially rectangular shape.” RIB at 60-62; SIB at 67-71.

[REDACTED]

For this limitation, Tela alleges the [REDACTED] as shown and referred to in Exynos Product design manuals, [REDACTED] CIB at 72 (citing CX-1144C at Q/A 2931-2936; CX-0727C at *38, 138, 141; CX-0726C at *46, 168, 171; CX-1144C at Q/A 3255-3258; CDX-0013C at *61; JX-0215 at *11, 13, 15, 19, 21). Tela presents the following image from the 14LPP design rules to “show substantially rectangular diffusion regions”:



CRB at 34 (citing CX-0726C at *170; CX-0727C at *38; CDX-0013 at *61). Tela continues:

[REDACTED] (See Tr.

(Subramanian) 1012:3-1013:8; Tr. (Auth) at 660:18-25.)

Id. Dr. Foty’s testimony relies similarly on layout shapes showing that “the [REDACTED] [REDACTED] are rectangular”:

[REDACTED]

[REDACTED]

CX-1144C at Q/A 2934 (citing CX-0272 at -00141).

The limitation is not met. There is a clear discrepancy between the [REDACTED] [REDACTED] Dr. Foty analyzes for the “substantially rectangular” requirement (CX-1144C at Q/A 2934), and the more specific [REDACTED] sources and drains Tela asserts meet the “diffusion region” limitation (CRB at 33). This is problematic because only the [REDACTED] source and drain structures can meet Order No. 34’s construction of “diffusion region,” as discussed above with respect to the Accused Products, and so it is those structures which must be “substantially rectangular” from a top-perspective.

As Respondents suggest (RIB at 61), the likely reason for this discrepancy is that undisputed teardown imagery of the Exynos 7420 shows the epitaxially grown source and drain structures do not have a substantially rectangular shape from a top-perspective, as shown in the bottom image below:

[REDACTED]

[REDACTED]

(RIB at 60 (citing RX-0014C at Q/A 579); *see* JX-0215 at *15);

[REDACTED]

(CX-0684 at *26 (excerpted); CIB at 61 (citing RX-0014C at Q/A 580)). Accordingly, this limitation is not practiced by the DI Products.

b. Claim 30

For reference, claim 30 of the 334 patent requires:

30. [30a] A semiconductor chip, comprising: gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a gate horizontal grid that includes a number of gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon,

[30b] wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers,

[30c] wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second

transistor type and does not form a gate electrode of a transistor of the first transistor type,

[30d] wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

[30e] a number of contact structures formed within the region of the semiconductor chip, wherein each of at least six gate structures within the region has a respective top surface in physical and electrical contact with a corresponding contact structure having a substantially rectangular shape, wherein each contact structure is centered in an x-direction on the gate structure with which it physical contacts,

[30f] wherein each contact structure that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in an x-direction, wherein each corresponding contact structure is in physical contact with only one gate structure, wherein each corresponding contact structure is positioned to overlap at least one edge of the gate structure contacted by the corresponding contact structure,

[30g] wherein each transistor within the region is formed in part by a corresponding diffusion region, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

[30h] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

[30i] wherein both a gate electrode of a transistor of a first transistor type and a gate electrode of a transistor of a second transistor type are formed by a same gate structure within the region.

334 patent at cl. 30 (annotated). The parties largely treat claim 30 the same as claim 29, as both claims require “diffusion regions” with “a substantially rectangular shape,” along with “gate structures positioned in accordance with a gate horizontal grid.” *See* CIB at 73-74; RIB at 60-62; SIB at 65-71. For all of the same reasons discussed with respect to claim 29, Respondents and the

Staff dispute that claim 30 is practiced by the DI Products. As determined above the DI Products do not practice claim 29. Accordingly, the DI Products have not been shown to practice claim 30.

F. Validity and Other Defenses

Respondents and the Staff identify and discuss the following invalidity and unenforceability theories for the 334 patent:

Claims	Theory
1, 2, 5, 15, 29, 30	Lack of written description 35 U.S.C. § 112, ¶ 1
1, 2, 5, 15, 29, 30	Lack of enablement under 35 U.S.C. § 112, ¶ 1
1, 2, 5, 15, 29, 30	Anticipated under 35 U.S.C. § 102(a), (b) by Intel’s 14nm Products
1, 2, 5, 15, 29, 30	Rendered obvious under 35 U.S.C. § 103 by Kitabayashi (JX-0267) and/or Intel 45nm Products
1, 2, 5, 15, 29, 30	Rendered obvious under 35 U.S.C. § 103 by Becker (RX-0027)
1, 2, 5, 15, 29, 30	Rendered obvious under 35 U.S.C. § 103 by Becker (RX-0027) and Greenway (JX-0286)
1, 2, 5, 15, 29, 30	Unenforceable due to covenant not to sue

See generally RIB at 62-121; SIB at 71-95. These theories are addressed in order below.

Before turning to their merits, however, a few preliminary points are warranted. Two of the disputed claims, 29 and 30, are pertinent only to the technical prong of domestic industry. *See* RIB at 74-75; SIB at 83-84. In general, however, it is “Commission practice not to couple an analysis of domestic industry to a validity analysis.” *Certain Soft-Edged Trampolines and Components Thereof*, Inv. No. 337-TA-908, Comm’n Op. at 53 (May 1, 2015). Indefiniteness is the only basis for invalidity that bears on whether the technical prong is met, because indefiniteness

[REDACTED]

“ma[kes] it impossible for the complainant to demonstrate whether a patent claim [is] practiced.” *Certain Silicon Microphone Packages and Products Containing the Same*, Inv. No. 337-TA-695, Notice at 3 (Jan. 21, 2011). But indefiniteness is not one of the asserted grounds of invalidity of these two claims. *See* RIB at 74-75; SIB at 83-84. Therefore, whether claims 29 and 30 of the 334 patent are invalid is not relevant, and the parties’ dispute over these claims need not be resolved or otherwise addressed.

An additional threshold matter is the priority date of the 334 patent. In their motion for summary determination, Respondents argued that new matter had been added to the application resulting in the 334 patent, and that the 334 patent is consequently not entitled to the priority date Tela asserts. *See* Order No. 27 at 2. This argument was rejected because of the existence of genuine issues of material fact. *Id.* at 3. Respondents and the Staff now seemingly renew this argument. *See* RIB at 65; SIB at 73-74; JX-0003 at *3. Tela does not dispute that the 334 patent’s grandparent application, U.S. Patent Application No. 14/711,731 (the “731 Application”), filed on May 13, 2015, contained a paragraph not found in any earlier filing in the chain of applications, but it characterizes that paragraph as “not new matter, but a recitation of the as-filed claims.” CRB at 37; *see* CIB at 79; *see also* RX-0019 at *24-26; 334 patent at 5:49-7:24.

In general, “claims to subject matter in a later-filed application not supported by an ancestor application . . . do not receive the benefit of the earlier application’s filing date.” *Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1346 (Fed. Cir. 2000). “Support” in this context means compliance with the first paragraph of 35 U.S.C. § 112. *Id.* (citing 35 U.S.C. § 120). One requirement of Section 112 is an adequate written description, meaning that the patent’s disclosure “conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010)

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(en banc) (citing 35 U.S.C. § 112). And one way that claimed subject matter may be conveyed, particularly for purposes of evaluating whether a disclosure contains “new matter,” is if the subject matter is “inherently contained in the original application,” that is, if it is “necessarily [] present in the original application’s specification such that one skilled in the art would recognize the disclosure.” *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1352 (Fed. Cir. 2001) (citation and internal quotation omitted); *TurboCare Div. of Demag Delavai Turbomachinery Corp. v. General Electric Co.*, 264 F.3d 1111, 1119 (Fed. Cir. 2001) (citing 35 U.S.C. § 120).

The subject matter at issue comprises two claim limitations recited in claim 1, from which claims 2, 5, and 15 depend: “a gate pitch of less than or equal to about 193 nanometers” and “gate structure[s] . . . with a width of less than or equal to about 45 nanometers.” 334 patent at 30:7-11. The 334 patent specification (disregarding the new paragraph) addresses pitch and width dimensions in several places: “minimum feature sizes are approaching 45nm” (*id.* at 4:7-8); “current feature sizes are as small as 65 nm and are expected to soon approach sizes as small as 45nm” (*id.* at 9:4-6); “in a 90 nm process technology, *i.e.*, minimum feature size equal to 90 nm, the gridpoint pitch . . . is about [240 nm]” (*id.* at 14:67-15:2; *see also id.* at 17:35, 21:54); “grid spacing is [360 nm]” (*id.* at 17:16; *see also id.* at 17:32) “gate electrode track pitch is [360 nm]” and “metal 2 track pitch” is either 240 nm or 270 nm (*id.* at 23:3-10); “metal 2 pitch of 280 nm” and “[w]ith the via lithography issues removed . . . about 220 nm” (*id.* at 26:45-49); and “at 90 nm the metal 4 pitch is 280 nm” (*id.* at 29:11-12). That is, the smallest pitch mentioned in the 334 patent specification is 220 nm, and although a feature size of 45nm is referenced, it is entirely aspirational. And the 2006 Provisional Application contains even fewer references to width and pitch (*see generally* RX-1365), with 240 nm being the smallest pitch mentioned (*id.* at 12).

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This is inadequate, even applying a broad understanding of “inherency.” No person of ordinary skill would understand that the inventors of the 334 patent possessed the claimed subject matter—a width of 45 nanometers and a pitch of 193 nanometers, much less smaller dimensions—as of March 9, 2006, or at any time prior to May 13, 2015. The 45 nanometer width limitation is supported only by a “mere wish or hope,” and the 193 nanometer pitch limitation is supported by literally nothing at all. *Nuvo Pharm. (Ireland) Designated Activity Co. v. Dr. Reddy’s Labs. Inc.*, 923 F.3d 1368, 1381 (Fed. Cir. 2019).

Tela’s arguments against this conclusion are unavailing. Tela principally contends that the “disclosure of scalability combined with the established knowledge of a POSITA is more than sufficient to meet the written description requirement.” CRB at 36 (citing *Streck, Inc. v. Research & Diagnostics Sys.*, 665 F.3d 1269, 1285 (Fed. Cir. 2012)). Certainly the written description requirement may be satisfied, in appropriate cases, by the combination of a patent’s disclosure and the knowledge of a skilled artisan, as *Streck* holds. 665 F.3d at 1285 (“in some instances, a patentee can rely on information that is ‘well-known in the art’ to satisfy written description”) (citation omitted). But Dr. Hook, one of Tela’s experts, did not examine the 334 patent’s prosecution history for the purpose of evaluating the priority date. Hr’g Tr. at 1135:8-1136:23, 1215:6-1216:20. And the patent flatly states that “current feature sizes are as small as 65 nm and are expected to soon approach sizes as small as 45nm.” 334 patent at 9:4-6. This is essentially an acknowledgment that the inventors did not consider feature sizes of 45 nanometers to be a part of their invention as of March 9, 2006, regardless of the disclosure and the knowledge of a skilled artisan.

Nor does the disclosure of “scalability,” combined with a skilled artisan’s capacity to create feature sizes of 65 nanometers, contribute anything meaningful to the analysis. The 334

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patent states that “circuit chip area” is reduced by “approximately 50% every two years,” and that this is achieved by “reducing the feature sizes between 25% and 30%.” 334 patent at 3:60-64. But the patent is directed to “managing lithographic gap issues as technology continues to progress toward smaller semiconductor device feature[] sizes,” not to actually achieving such smaller feature sizes. *Id.* at 4:31-33; *see* CIB at 76 (the patent is “directed to a layout methodology for use as semiconductor sizes continue to scale down”). The specification describes a layout methodology which would seemingly apply where gate widths are 45 nanometers and gate pitches are 193 nanometers, but it does not “teach[] how to scale gate layouts” to achieve those smaller widths and pitches, or otherwise provide any indication that the inventors even believed that such sizes were part of their invention. CIB at 77. That the “scaling has proven true in the industry,” resulting in 2019 widths and pitches even smaller than 45 and 193 nanometers, respectively, does not mean that the inventors had possession of such small widths and pitches in 2006, or believed that those widths and pitches were a part of the invention. CRB at 36. In fact, although some of the listed prior art references use the term “scalable” or the like, the 334 patent itself does not even use the term “scalability.” *E.g.*, JX-0003 at *12 (listing, *inter alia*, Baldi, et al., “A Scalable Single Poly EPROM Cell for Embedded Memory Applications”).

Although not explicitly raised by Tela, there is evidence of the inventors’ conception and reduction to practice pertaining specifically to the 2006 Provisional Application, and it is similarly unhelpful. CIB at 100-101. Specifically, for purposes of establishing the date of conception, Tela argues that the 2006 Provisional Application “discloses . . . features smaller than 45nm or 193 nm, as claimed.” *Id.* at 101. But the evidence Tela relies on for this argument does not, in fact, support it. Dr. Hook’s opinion that gate widths and pitches of less than 45 and 193 nanometers are so “disclose[d]” is based on Figure 1 of the 2006 Provisional Application, which shows an expected

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“feature size” of less than 45 nanometers beginning only some time after about 2012, and does not even reference gate pitch. *Compare CX-1231C at Q/A 405 with RX-1365 at *15* (Figure 1 of the 2006 Provisional Application). And Mr. Becker’s rebuttal testimony about feature sizes seems to be based entirely on hindsight: although he testified that at the time the 2006 Provisional Application was filed, “minimum feature sizes” were “less than or equal to about 45nm process technology,” the application itself states only that minimum feature sizes were “approaching 45nm.” *CX-1233C at Q/A 39; RX-1365 at *4.*

Tela also cites witness testimony to the effect that as of March 2006, “others in the industry had fabricated” devices with gate widths of 10 nanometers. *CRB at 36-37; see also CIB at 76-77.* Admittedly, Dr. Hook testified that “10 nm FinFET structures” had been described “in the early 2000’s,” and this does not appear to be genuinely disputed by Respondents. *CX-1231C at Q/A 1761.* But one exhibit cited as evidence for 10 nanometer FinFET structures, U.S. Patent No. 6,413,802, does not disclose any particular dimension size, and although Dr. Subramanian, one of its co-inventors, testified that it had “gate features in the tens of nanometer range,” it also had a gate pitch of 75,000 nanometers, not 80-100 nanometers, as Tela claims (*see CIB at 76* (citing *JX-0271*); *Hr’g Tr. at 1007:5-17*; *CRB at 39* (citing *JX-0302 at *47*, which describes gates fabricated in 2011 with widths of 22 nm and pitches of 80-100 nm)). Also, Dr. Hook’s testimony is based in part on *CX-1315*, a document not admitted in evidence. *CX-1231C at Q/A 1761.* That is, it may have been possible in 2006 to fabricate an individual transistor with a 10 nanometer gate width, but Tela cites no evidence that an entire chip could be fabricated with 10 nanometer widths and pitches of 193 nanometers or smaller, or, more to the point, that the inventors of the 334 patent viewed such dimensions as a part of their invention. *See Hr’g Tr. at 1007:5-17* (Dr. Subramanian

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opined that a person of ordinary skill in 2006 would not have been able to make “a semiconductor chip with FinFET transistors”).

Tela further cites testimony that the dimensions recited in the 334 patent refer to feature sizes “available in commercial products at that time.” CRB at 36-37 (citing CX-1233C at Q/A 40 (Becker)); *see also* CIB at 76-77. The specification does not distinguish between what was known at the cutting edge of chip technology and what was commercially available, however; the disclosure merely states that feature sizes “are approaching 45nm”—demonstrating that a gate width of 10nm was simply not contemplated by the inventors except as an objective that might be reached years in the future, without regard to commercial viability. 334 patent at 4:8; *see also* 334 patent at 9:5-6. And Mr. Becker’s testimony about feature sizes in 2006 being “less than or equal to about 45nm process technology” is inconsistent with the 334 patent itself, which (like the 2006 Provisional Application) only states that minimum feature sizes were “approaching 45nm.” CX-1233C at Q/A 39; 334 patent at 4:8. In fact, even as of 2010 the International Technology Roadmap for Semiconductors (“ITRS”) implied that 24 nanometer structures were expected to have known “[m]anufacturable solutions” by 2012, but that 10 nanometer structures were not. JX-0302 at *47; Hr’g Tr. at 1117:2-1119:24; *see* Hr’g Tr. at 1266:1-23 (products described in the ITRS with no known manufacturable solutions are “in research or early development phase”).

Lastly, the Examiner’s views on priority date, although not binding in this investigation, warrant mention. Notices of Allowability and of Allowance issued on April 12, 2018, and what is now the 334 patent received an issue date of June 5, 2018 as U.S. Patent No. 9,991,283. *See* RX-0019 at *7548-7552, 7579. On May 25, 2018, however, the applicants filed an Information Disclosure Statement containing a complaint, filed 10 days earlier in the United States District Court for the Northern District of California, in which Respondent Intel Corp. sued Complainant

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Tela for a declaratory judgment of invalidity and noninfringement of claims of other patents assigned to Tela, including patents previously asserted in this investigation. *See id.* at *7583-7610. In response, an Examiner Interview took place on May 31, 2018, in which the Examiner “suggest[ed] removing [the 45 nanometer width and 193 nanometer pitch] limitations from the specification” because they were “new matter.” *Id.* at *7630. “No agreement was reached,” however, and on August 8, 2018, the Examiner issued a “Corrected Notice of Allowability” that found every claim “not entitled to the benefit of the prior application,” on the basis that the claimed width and pitch ranges had “no antecedent basis” in the prior-filed application. *Id.* at *7630-7636. The applicants then traversed the notice of allowability and filed a declaration from Dr. Sunil P. Khatri, who opined that the ancestors of the 731 Application, including the 2006 Provisional Application, contained “written description support” for the width and pitch ranges at issue, essentially on the same basis Tela advances here. *Id.* at *7645-7659. The 334 patent eventually issued on November 27, 2018; although Tela argues from this that the Examiner “apparently agreed with Dr. Khatri,” there is no documentary evidence of such agreement beyond the mere fact of issuance. *Id.* at *7660; CIB at 79.

In sum, the evidence demonstrates clearly and convincingly that the 334 patent’s disclosure does not convey to those skilled in the art, either explicitly or inherently, that the inventors had possession of the entire subject matter of claim 1 as of March 9, 2006. So the claims at issue, claims 1, 2, 5, and 15, are only entitled to a priority date of May 13, 2015, the date the new matter was added to the 731 Application,

1. 35 U.S.C. § 112, ¶ 1 (Written Description)

Neither Respondents nor the Staff advance any substantive argument that the written description requirement is not satisfied by the 334 patent, in view of the 2015 priority date. They argue only that: (1) the “2015 amendment adding the Claimed Ranges *in ipsius verbis*” is

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inadequate; and (2) the 2015 priority date is unavailable because the 731 Application was a continuation, not a continuation-in-part. RIB at 65-66, 65 n.8; *see* SIB at 74-75. Neither argument is persuasive.

As to the first argument, the case law is clear that simply reciting the claim language in the specification is not enough to meet the written description requirement; the specification must “described the claimed invention” and not merely state the claimed limitations. *Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 968 (Fed. Cir. 2002). But that is not the situation here. The new matter is a long, detailed paragraph describing the ranges in dispute, as well as the rest of the invention of claim 1 and its dependent claims. *See* 334 patent at 5:49-7:24. This is sufficient to satisfy the written description requirement.

As to the second argument, Respondents and the Staff rely on *TurboCare* to argue that “new [matter] introduced during prosecution without a CIP application must find written support in the originally-filed application or else it is invalid.” RIB at 65 (citing 264 F.3d at 1119) (emphasis omitted); *see* SIB at 75. In *TurboCare*, the applicant amended his specification during prosecution in response to an indefiniteness rejection, and further added new claim 2. *See* 264 F.3d at 1117. The United States Court of Appeals for the Federal Circuit affirmed a summary judgment of invalidity, holding that one new element of claim 2 was new matter because the “original disclosure was [not] sufficiently detailed” to enable a skilled artisan to recognize that the applicant had invented that claim. *Id.* at 1118-19. But it also noted, citing in part 35 U.S.C. § 120, that “[b]ecause [the applicant] did not file a continuation-in-part application, he cannot rely on any alternative filing date for his newly added claim . . . [so] claim 2 is invalid for an inadequate written description.”

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Respondents and the Staff place too much reliance on this statement. The applicant in *TurboCare* filed an application, and then amended it by adding new matter, in contravention of 35 U.S.C. § 120. Had the applicant instead added the new matter by filing a continuation-in-part application, or presumably an entirely new original application, Section 120 would not have been violated, and the filing date of new claim 2 would have been the priority date. In other words, the obverse of the Federal Circuit’s dicta in *TurboCare* amounts to “had the applicant added new matter by filing a later application, he would have received a later priority date, and new claim 2 would have satisfied the written description requirement.” That is essentially what happened here: the applicants filed a new application containing new matter, and because all the claims in suit possess the gate width and pitch ranges at issue, the priority date for all claims is the filing date of the new application, May 13, 2015. Admittedly, the applicants here filed a continuation application rather than a continuation-in-part, but the consequence of that is simply a later priority date rather than invalidation. *See Reiffin*, 214 F.3d at 1346 (“claims to subject matter in a later-filed application not supported by an ancestor application” receive a later priority date). Inasmuch as the other cases on which Respondents rely interpret *TurboCare* differently, those cases are not binding on me, and their interpretations are not persuasive. *See* RIB at 65 n.8.

Therefore, claims 1, 2, 5, and 15 of the 334 patent satisfy the written description requirement of Section 112.

2. 35 U.S.C. § 112, ¶ 1 (Enablement)

As with the written description requirement, Respondents renew the enablement argument that was previously rejected in the context of summary determination. *See* CIB at 68; Order No. 27 at 2. The crux of Respondents’ argument is that, “at the effective filing date of the patent, one of ordinary skill in the art could not practice the[] full scope” of the ranges of gate width and pitch recited in claim 1 of the 334 patent “without undue experimentation.” RIB at 68 (citing *Wyeth*

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and *Cordis Corp. v. Abbott Labs.*, 720 F.3d 1380, 1384 (Fed. Cir. 2013)). The Staff agrees. SIB at 76.

There is “significant overlap” between the written description and enablement requirements of 35 U.S.C. § 112. *Univ. of Rochester v. G.D. Searle & Co., Inc.*, 358 F.3d 916, (Fed. Cir. 2004). In one respect pertinent here, however, they are significantly different: the written description requirement is satisfied no matter how far the gate width and pitch ranges extend below 45 and 193 nanometers, respectively, but enablement cannot be properly analyzed without ascertaining the “full scope” of the claimed ranges. *AK Steel Corp. v. Sollac and Ugine*, 344 F.3d 1234, 1241 (Fed. Cir. 2003) (“an enablement inquiry typically begins with a construction of the claims”). This is because the written description supports width and pitch ranges with no lower bounds, but the written description may not enable them. *See* RIB at 68 and n.11; *see also* SIB at 82.

So claim 1 must be construed to establish those lower bounds. As noted with respect to infringement, there is no genuine dispute that the two lines of Accused Products possess gate widths and pitches of 28 nanometers and 70 nanometers (for the Intel 14nm Products) and 22 nanometers and 54 nanometers (for the Intel 10nm Products). *See* CX-1144C at Q/A 275-280. Nor is there a genuine dispute that the Samsung Exynos products possess a gate width of no more than about 36 nanometers, and a gate pitch of about 78 nanometers. *See id.* at Q/A 3133-35. The parties’ only contentions on constructions of the claimed ranges are therefore in connection with invalidity.

Unfortunately, those contentions are not entirely clear. Respondents state that “there is a (yet unknown) physical limit to how small gate widths and pitches can ultimately be.” RRB at 37 n.5. And they appear to contend, in reliance on the testimony of Tela’s expert, Dr. Hook, that

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“single-digit nanometer gate widths” and 40 nanometer gate pitches are within the scope of the claims, although they do not explicitly assert that anything smaller qualifies. RRB at 34, 37. The Staff takes a similar position. SIB at 77. Tela, also citing the testimony of Dr. Hook, contends that the lower bound is “the limit of standard CMOS processing,” which it further specifies as gate widths of 10 nanometers and gate pitches of 40 nanometers. CRB at 39 (internal quotation omitted).

The parties therefore appear to agree that the lower bound for gate pitch is 40 nanometers; there does not appear to be any relevant intrinsic evidence, and this dimension is supported by the knowledge of a skilled artisan, as established by Dr. Hook. The parties do not agree on the lower bound for gate width, although they are not far apart, and Tela and Respondents seemingly agree that Dr. Hook’s testimony is authoritative regarding the knowledge of a POSITA. Dr. Hook testified that a “7 nanometer node” is within the scope of the claimed range of gate width, although he admitted it is “beyond today’s manufacturing” abilities. Hr’g Tr. at 1120:20-1122:9. So the claimed ranges are construed as a gate width from about 45 nanometers to 7 nanometers and a gate pitch from about 193 nanometers to 40 nanometers.

Much of the briefing on enablement presupposes a priority date of 2006 rather than 2015. Nonetheless, Respondents argue in the alternative that the full scope of the claims cannot be practiced “even today without undue experimentation.” RIB at 68. That argument is meritorious, as consideration of the factors enumerated in *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988), shows:

The quantity of experimentation necessary and the relative skill of those in the art. These factors are related. Dr. Hook does not dispute that it takes the full-time effort of at least 1,000 engineers, 95% of whom have doctorates, and “billions” of dollars in research and development

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expenses, to reduce the scale of integrated circuit chips by a single process node. Hr’g Tr. at 1105:12-1106:13. This would indeed seem to be “the very definition of ‘undue experimentation.’” RRB at 39. Although such labors are “commonplace” and “business as usual” for the semiconductor industry, as Dr. Hook testified, they are surely far from “routine” within the meaning of *Wands*. See CIB at 78. And although the level of ordinary skill in the art is neither especially high nor especially low, the level of skill needed to achieve a reduction in scale, as opposed to simply practicing the invention, is clearly well beyond the capabilities of a POSITA.

The amount of direction or guidance presented. Even considering the new matter added in 2015, Dr. Hook is correct that the 334 patent is “silent on the process” of resolving the various technical hurdles to scaling down chip size. Hr’g Tr. at 1111:20-25. Tela’s position, that the disclosure of a standard CMOS process is adequate, is unpersuasive. CRB at 40-41. Describing CMOS as a “standard” and “well-known” process provides no guidance whatsoever to a skilled artisan about how to shrink chip size. The specification essentially just presupposes that any technical hurdles in reducing gate width and pitch will eventually be overcome; that is, it leaves entirely to someone else the task of solving the problems preventing a skilled artisan from practicing the full scope of the invention.

The presence or absence of working examples and the state of the prior art. As noted in analyzing the written description requirement, all the working examples in the specification pertain to sizes larger than or equal to the claimed range. E.g., 334 patent at 9:4-16. Even the new matter added in 2015 provides only a single working example possessing the upper bounds of the claimed ranges. See *id.* at 6:38-46. And the state of the prior art was such that no working examples of the smallest width and pitch would have existed as of 2015; again, Dr. Hook admitted at the hearing that the lower bound of the claimed gate width is “beyond today’s manufacturing”

abilities. Hr’g Tr. at 1121:18-1122:9. So Dr. Subramanian’s testimony that in 2016, after the priority date, the lowest width and pitch combination commercially available was 22 and 70 nanometers, more than one process node greater than the lower bound of the claimed ranges, stands un rebutted. *See* RX-0007C at Q/A 157.

The nature of the invention. As noted, during prosecution the Examiner specifically suggested removing the 45 and 193 nanometer limitations from the claims, but the applicants declined to do so, and instead traversed their own notice of allowability. *See* RX-0019 at *7630-7659. This indicates that the applicants considered the feature ranges to be sufficiently important to the invention that they needed to remain in that application, and in the descendant applications, including the one that issued as the 334 patent. On the other hand, it is not clear why the applicants believed this; Respondents suggest that it was because the applicants wished to avoid prior art, but point to no evidence explicitly supporting such an inference. *See* RIB at 64. Moreover, the “heart of the invention” appears to be the combination of various chip layers possessing rectilinear features, and not the actual sizes of those features. *E.g.*, 334 patent at 4:30-33 (“a solution is needed for managing lithographic gap issues as technology continues to progress toward smaller semiconductor device feature sizes”), 10:6-7 (the problem “stem[s] from variability introduced by design-dependent unconstrained feature topologies”); *Certain Multi-Stage Fuel Vapor Canisters and Activated Carbon Components Thereof*, Inv. No. 337-TA-1140, Final Initial Determination at 168 (Jan. 28, 2020) (not reviewed in relevant part). So on balance, this factor weighs slightly against a finding of undue experimentation.

The predictability or unpredictability of the art. This factor also weighs against a finding of undue experimentation. Dr. Hook explained it succinctly: “you can do a pretty good job of predicting that a bunch of engineers will arrive at a solution if you give them enough time and

enough money.” Hr’g Tr. at 1125:18-1126:11. In fact, semiconductor design and fabrication is so predictable an art that it has historically followed “Moore’s Law”—integrated circuits have halved in area on average once every two years. *See* 334 patent at 3:59-61; CX-1231C at Q/A 1699.

The breadth of the claims. As of 2015 integrated circuits with gate widths and pitches well below 45 and 193 nanometers, respectively, had been fabricated. *E.g.*, JX-0302 at *47 (describing a chip made in 2011 with 22 nm gate width and 80-100 nm gate pitch). But the claims are not limited to what could be made and used in 2015; they include ranges with lower bounds beyond what can be made and used even today. Hr’g Tr. at 1121:18-1122:9. Had the claimed ranges been drafted with the knowledge of a skilled artisan in mind, the breadth of the ranges would likely have been uncontroversial. But that is not the situation presented here, and the breadth of the claims weighs against finding enablement.

In sum, the *Wands* factors are mixed. That the relevant art is predictable weighs against a finding of undue experimentation, but, importantly, that predictability is achieved by tremendous research and development efforts. And the nature of the invention also weighs against undue experimentation, albeit only slightly. Otherwise, the *Wands* factors weigh in favor of finding that undue experimentation would be needed to practice the full scope of the claims, down to the lower bounds of the claimed ranges of gate width and pitch. Particularly significant is Dr. Hook’s admission at the hearing that the lower bounds are both within the scope of the claims and not manufacturable. *See* Hr’g Tr. at 1121:18-1122:9. So the “breadth of enablement in the patent specification[] is not commensurate in scope with the claims.” *Enzo-Biochem, Inc. v. Calgene, Inc.*, 188 F.3d 1362, 1377 (Fed. Cir. 1999).

Therefore, claims 1, 2, 5, and 15 of the 334 patent are invalid for lack of enablement.

3. Intel 14nm Products

Respondents contend that the asserted claims of the 334 patent are anticipated, but only by the Intel 14nm Products. RIB at 75-76. As a threshold issue and more specifically, Respondents contend that the “Broadwell” 14nm product is prior art to the 334 patent under 35 U.S.C. § 102(a) and (b), assuming that patent’s priority date is May 13, 2015. *Id.* Tela presents no argument on this point beyond its assertion that the 334 patent’s priority date is instead 2006. CRB at 42.

Intel publicly demonstrated the operation of the Broadwell chip, an Intel 14nm Product, on September 10, 2013, at an Intel Developer Forum. *See* RX-0174 at *5-6. Based on the transcript (RX-0174) and video (RX-0176) of that forum, Dr. Subramanian opines that the Intel 14nm Products were publicly disclosed no later than the date of the forum, in 2013. *See* RX-0007C at Q/A 941. This qualifies as public use more than one year before the application date under the pre-AIA version of 35 U.S.C. § 102(b). *See Honeywell Int’l, Inc. v. Universal Avionics Systems Corp.*, 488 F.3d 982, 998 (Fed. Cir. 2007) (“A barring public use requires a public use more than one year before the patent filing date that employs a completed invention in public, without confidentiality restrictions, and without permitted experimentation.”) (citing 35 U.S.C. § 102(b) (2002)); *see also* 35 U.S.C. § 102(a)(1) (2015) (post-AIA version of Section 102: “the claimed invention was . . . in public use” more than one year “before the effective filing date”).

Therefore, the Broadwell 14nm Product is prior art to the 334 patent. As determined above, the Broadwell 14nm Product infringes claims 1, 2, and 5, but not claim 15, of the 334 patent. Thus, under the principle that an infringing product, if earlier, anticipates (*see Upsher-Smith Labs.*, 412 , F.3d at 1322), claims 1, 2, and 5 of the 334 patent are invalid as anticipated, and claim 15 is not.

4. Kitabayashi in combination with Intel 45nm Products

Respondents contend it would have been obvious to a POSITA to combine the teachings of a U.S. patent prior art reference, Kitabayashi, with certain 45nm processor products from

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respondent Intel, in such a way that meets all limitations of the asserted claims. *See* RIB at 77-112.

Kitabayashi, U.S. Patent No. 7,200,831, issued on April 3, 2007, and is unquestionably prior art. *See* 35 U.S.C. § 102(a) (2015) (“the claimed invention was patented” more than one year “before the effective filing date of the claimed invention”). It is also prior art under the pre-AIA version of 35 U.S.C. § 102(e), as Respondents allege; the 334 patent’s invention date is the filing date, May 13, 2015, because of the new matter added at that time, and Kitabayashi was therefore “granted on an application for patent by another filed in the United States before the invention by the applicant for patent.” 35 U.S.C. § 102(e) (2002). Tela does not dispute that Kitabayashi is prior art. *See* CIB at 80.

Whether the Intel 45nm Products qualify as prior art is disputed, however. Respondents contend, presumably on the assumption that the 334 patent is entitled to a 2006 priority date, only that the Intel 45nm Products are prior art under the pre-AIA version of 35 U.S.C. § 102(g). RIB at 77-78. Under that provision, a patent is invalid if “before [the patentee]’s invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it.” 35 U.S.C. § 102(g)(2) (2002). The Intel 45nm Products were on sale in the U.S. no later than November 12, 2007, under the commercial name “Penryn,” so Respondents have made out a prima facie case that they were “made” and “not abandoned, suppressed, or concealed” before the 334 patent’s 2015 priority date. *See* RX-0007C at Q/A 224-25 (citing JX-0274 and JX-0276). Tela does not dispute that the Penryn chip was on sale in the U.S. by November 2007. CIB at 81.

Tela instead contends—also presumably on the assumption that the 334 patent has a 2006 priority date—that the Penryn chips were based on a “45nm test chip” that was not commercialized

[REDACTED]

and remains confidential to this day, and which therefore was abandoned, suppressed, or concealed. CIB at 81-82. So most of Tela’s Section 102(g) arguments are irrelevant because they are directed exclusively to the test chip rather than to the Penryn chip. *See generally id.* at 81-88.

But Tela does advance three arguments that seemingly apply separately to the Penryn chip: (1) because the technical details of the Penryn chip have never been adequately publicized, that chip was abandoned, suppressed, or concealed (*see* CIB at 82-83); (2) Intel was not diligent in reducing the Penryn chip to practice (*see* CRB at 45-47); and (3) the Penryn chip was not “made in this country by another inventor” (*see* CIB at 86-87). The first two arguments are foreclosed by *Fox Group, Inc. v. Cree, Inc.*, 700 F.3d 1300 (Fed. Cir. 2012). In that case, the United States Court of Appeals for the Federal Circuit held that “commercialization” of a good embodying a product claim is a “way to prove public disclosure,” even when that commercialization by itself is non-enabling, thus negating any claim of abandonment, suppression, or concealment. 700 F.3d at 1306-07. That is precisely what Intel did here, and Tela’s arguments that *Fox Group* is inapposite, or that its dissenting opinion should be followed, are unpersuasive. *See* CRB at 51-52; CIB at 144 n.12. The Federal Circuit also held that an accused infringer may demonstrate invalidity under Section 102(g) by proving it “reduced its invention to practice first,” without regard to diligence. *Id.* at 1304. That, too, is precisely what Intel did here, so proof of diligence is not required. *See id.*; RX-0007C at Q/A 247 (Dr. Subramanian opining that Intel performed a reduction to practice).

The third argument is foreclosed by *Solvay S.A. v. Honeywell Int’l Inc.*, 742 F.3d 998 (Fed. Cir. 2014). In that case, involving method claims, Russian engineers “first conceived the invention and reduced it to practice in Russia.” 742 F.3d at 1002. Honeywell, the accused infringer, then “replicated the Russian process by following the information provided by [the

[REDACTED]

Russian engineers], thereby practicing the invention in the United States.” *Id.* at 1007. The Federal Circuit held that such a later reduction to practice in the United States qualifies as “mak[ing]” the invention “in this country by another inventor,” even though the Russian engineers were not the ones who performed the domestic reduction to practice. *Id.* And, again, Intel performed a reduction to practice, and did so domestically. *See* JX-0275 at 5 (the 45nm chip “is being developed by [Intel’s] Logic Technology Development group located in Hillsboro, Oregon”); JX-0278 at *2; RX-0007C at Q/A 247. That Intel has never identified the Penryn chip’s inventors by name is irrelevant, because there is no evidence, or even argument, that the inventors of the 334 patent made the Penryn chip. *See* CRB at 44 (asserting that the persons who conceived of the test chip are unidentified); CIB at 82.

Therefore, the Intel 45nm Products, and more precisely the Penryn chip, are prior art to the 334 patent.

As to the merits of the obviousness theory, Kitabayashi discloses “semiconductor integrated circuit wiring” having a “multilayer structure.” JX-0267 at 1:15-16, 2:37. Each successive wiring layer consists of straight-line wiring that is “orthogonal” or “inclined” relative to the previous layer, so that “the wiring traces constitute a grid,” and each successive wiring layer is “connected through vias.” *Id.* at 5:2, 5:56-58, Figs. 1-9. The lowest wiring layer is “connected to . . . the transistors (circuit elements).” *Id.* at 5:2-3.

The Intel 45nm Products, including the Penryn chip, are described in various documents summarized by Dr. Subramanian. *See generally* RX-0007C at Q/A 213-336. Dr. Subramanian also provides an element-by-element claim comparison. *See generally id.* at Q/A 370-462. The Intel 45nm Products comprise gate structures on a semiconductor chip, positioned relative to

diffusion regions to form transistor gates. *See id.* at Q/A 379; RDX-0009C at *108. Above that are metal layers that do not use a “gridded layout.” *Id.* at Q/A 327; *see* RDX-0009C at *96.

Respondents’ basic contention is that “it would have been obvious to combine Kitabayashi’s gridded metal structure with Intel’s unidirectional gate structures . . . [and] to set the lowest-lying metal layer of Kitabayashi to run orthogonal to the gate direction.” RRB at 57. But Claim 1 also requires “at least five” substantially rectangular first-metal structures positioned on “at least eight first-metal gridlines,” with “adjacent” first-metal structures spaced “less than or equal to 193 nanometers” apart. 334 patent at 30:42-50, 31:3-5. Kitabayashi teaches no particular spacing, and the Intel 45nm Products have neither first-metal gridlines nor consistent spacing, because they are not substantially rectangular. *See* RX-0007C at Q/A 420-23, 433-34. Dr. Subramanian’s testimony that the Intel 45nm Products have “metal interconnect layers” with a fixed pitch, that a skilled artisan would know to set at 160 nanometers, makes no sense; the conducting structures in those layers are two-dimensional, and therefore either have no pitch at all or two pitches which appear to be different. *Id.* at Q/A 434; RDX-0009C at *129. And although a 1992 textbook by Maziasz and Hayes, also referenced by Dr. Subramanian, discloses six rectangular first-metal structures, it does not disclose eight gridlines. *See* RX-0028 at 15, Fig. 1.10; RX-0007C at Q/A 324-325. Therefore, even though a combination of the gate arrangement of the Intel 45nm Products and the gridded metal layers of Kitabayashi comes close to an embodiment of claim 1 of the 334 patent, Tela is correct that there is an element missing from that combination, and from the various additional references on which Respondents rely. *See* CRB at 59-60.

Additionally, Tela argues that the combination of seven gate gridlines and eight first-metal gridlines, perpendicular to each other, is not found in the prior art. *See* CIB at 90; CRB at 57.

[REDACTED]

This requirement is found in the references to “y-direction” and “x-direction” in the claim limitations “each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline” and “each first-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline.” 334 patent at cl. 1.

Kitabayashi may provide an express motivation to combine the “semiconductor integrated circuit wiring” structures it discloses with “transistors,” *i.e.*, the combination of structures forming the transistors in the Intel 45nm Products. JX-0267 at 5:2-3; CIB at 90 (citing RX-0007C at Q/A 335, 338); RIB at 86-87. But Kitabayashi is silent as to what the transistors look like, how they are oriented, and how many there must be. *See generally* JX-0267. Dr. Subramanian does not persuasively provide these elements, either. He identifies a region in the Intel 45nm Products, not asserted for purposes of invalidity, which happens to have metal structures more closely resembling rectangles and extending perpendicular to the gate structures. RX-0007C at Q/A 322; RDX-0009C at *96. But in the region of the Intel 45nm Products which is asserted for purposes of invalidity, the first-metal structures largely extend perpendicular to the gate structures and do not resemble rectangles at all. *See* RDX-0009C at *125, 129, 131, 132, 135, 139; RX-0007C at Q/A 415-446. This is shown below with gate structures in dark green, running vertically, and first-metal structures in light blue, also running largely vertically:



RDX-0009C at *125;



id. at *135.

Dr. Subramanian’s testimony that it was known in 2006 that “metal 1” structures “could” run perpendicular to gate structures is not evidence of motivation either. RX-0007C at Q/A 323-

[REDACTED]

would have been obvious) with unidirectional first-metal structures, Intel went in a different direction.

So Respondents have not clearly and convincingly shown why, even once Kitabayashi and the Intel 45nm Products are combined, a person of ordinary skill would place the lowest, first-metal, layer of Kitabayashi perpendicular or orthogonal to the gate structures in the Intel 45nm Products. In other words, Respondents have not shown “all the elements of [claim 1] are found in a combination of prior art references.” *Velandier v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003). And, necessarily, they also have not shown “an apparent reason to combine” existing elements with a nonexistent element. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). That is, the combination of Kitabayashi and the Intel 45nm Products, in view of “(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, [and] (3) the differences between the claimed invention and the prior art,” does not make out a prima facie case of obviousness of claim 1. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1379 (Fed. Cir. 2008).

5. Becker, and Becker in combination with Greenway

Respondents allege that Becker, U.S. Pub. No. US 2007/0210391, which was published on September 13, 2007, renders the claims of the 334 patent obvious under a single-reference theory. *See* RIB at 112-113. Respondents are correct that Becker is prior art under the pre-AIA version of 35 U.S.C. § 102(b), because it is a printed publication predating the 334 patent’s priority date of May 13, 2015. *See id.* As with the Intel 14nm Products, Tela advances no argument that Becker is not prior art, beyond its erroneous contention that the 334 patent is entitled to a 2006 priority date. *See* CIB at 92-93; CRB at 62-63.

Respondents also offer an obviousness theory based in a combination of Becker and a printed publication referred to as Greenway, entitled “32nm 1-D Regular Pitch SRAM Bitcell

[REDACTED]

Design for Interference-Assisted Lithography.” RX-0007C at Q/A 94. Greenway predates the 334 patent’s priority date of May 13, 2015, and therefore qualifies as prior art under the pre-AIA version of 35 U.S.C. § 102(b). JX-0286. Tela does not expressly dispute this, although Greenway was published after 2006. *See* CIB at 93; CRB at 62-63.

As to the merits of the obviousness theory, Becker contains a disclosure similar to that of the 731 application and the 334 patent, but, notably, without the additional paragraph constituting new matter. *Compare* RX-0027 at *22 with 334 patent at 5:49-7:24. Respondents concede that “Becker does not expressly disclose gate widths . . . and gate pitches and other spacing” having the ranges recited in claim 1. RIB at 112-13. Therefore, Becker by itself does not make out a prima facie case of obviousness. Nor does the fact that by 2015 “feature sizes and spacings that fall within” the claimed ranges would have been known to a skilled artisan change this conclusion, because the full extent of the claimed ranges were not known to a skilled artisan at that time, and are still not manufacturable today. *Id.*

As for the combination of Becker and Greenway, Tela’s (erroneous) response is that Becker is not prior art. *See* CIB at 93; CRB at 62-63. Greenway does disclose certain elements of claim 1 that are not disclosed in Becker, as Dr. Subramanian explains. *See* RX-0007C at Q/A 939. However, as with the combination of Kitabayashi and the Intel 45nm Products, there is an element missing from the combination of Becker and Greenway.

Claim 1 requires a layer of “at least seven gate gridlines,” each containing at least one “substantially rectangular” gate structure, that is, a gate layer of at least seven substantially rectangular structures, each of which “compris[e] a transistor gate.” 334 patent 30:5-14; Order No. 34 at 55. This element is not found in either Becker or Greenway; Becker discloses at most six gate structures, and Greenway apparently discloses only four. *See* JX-0267 at 5:2-3; RX-0027

[REDACTED]

at Fig. 5. By contrast, the new matter added to the 731 Application describes “at least ten conductive structures,” where “[s]ome of the at least ten conductive structures form at least one transistor gate electrode.” 334 patent at 5:53-56. Dr. Subramanian implicitly concedes that seven gate structures are absent from Becker and Greenway when he opines that “[a]dding more gridlines and gate structures . . . would be mere duplication.” RX-0007C at Q/A 845.

Admittedly, this element is found in a prior art reference, namely, one of the designs for the Penryn chip. *See* RX-0007C at Q/A 375 (citing RDX-0009C at *107C (showing at least eleven gridlines on which gate structures are disposed)). But Respondents do not cite this reference in combination with Becker and Greenway, and a skilled artisan’s knowledge that “mere duplication” might work is not a substitute for actually identifying a prior art element. So, again, Respondents have not shown “all the elements of [claim 1] are found in a combination of prior art references,” and the combination of Becker and Greenway, in view of “(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, [and] (3) the differences between the claimed invention and the prior art,” does not make out a prima facie case of obviousness of claim 1. *Velandar*, 348 F.3d at 1363; *Scanner Techs.*, 528 F.3d at 1379.

6. Secondary Considerations

The secondary considerations of non-obviousness are equivocal at best. Tela offers essentially no evidence of skepticism by others and commercial success. *See* CIB at 95-97. At most it points to joint research and development projects with three entities that did not result in a commercial product. *See id.*; CX-1231C at Q/A 1820-1851. As for failure by others, Tela cites one instance of such failure, in which a company “attempted to make lithographic friendly designs” in a manner different from the 334 patent’s claims, but could not reduce the chip area enough. *See* CX-1231C at Q/A 1818-1819. Any long-felt but unmet need seemingly was satisfied by the Intel

[REDACTED]

45nm Products, which used two-dimensional first metal structures. *See* RX-0007C at Q/A 422-423; RDX-0009C at *125.

There is evidence of copying by Intel, but it is limited to linear first-metal structures oriented perpendicular to the gates. *See* CX-1231C at Q/A 1855-1861. There is also evidence that licensing resulted in substantial revenues for Tela. *See* CX-1231C at Q/A 1852-1854. Nonetheless, it is not clear to what extent the licensing was connected to the claims of the 334 patent, as opposed to other licensed patents, or simply to resolve litigation. *See* RIB at 119-120. So on balance, the secondary considerations of non-obviousness do not change the ultimate conclusion: Respondents have not carried their burden of proving that claim 1 is invalid as obvious, and, by extension, claims 2, 5, and 15, which depend therefrom. *Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358, 1365 (Fed. Cir. 2008) (citing *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992)) (“But if claim 1 is not obvious then claims 6-8 also cannot be obvious because they all depend from a nonobvious claim.”).

7. Covenant Not to Sue

In addition to theories of invalidity, Respondents contend there can be no infringement of the 334 patent in light of a [REDACTED] covenant not to sue (hereafter, “CNTS”) between Tela and respondent Intel. RIB at 120-121. Respondents argue “Tela agreed [REDACTED]

[REDACTED]

[REDACTED] *Id.* (citing RX-0003C at Q/A 43; RX-0054C at *1-2. Because the 334 patent has a priority date of May 13, 2015, Respondents argue it is covered by the CNTS. *Id.* at 121. Respondents further argue the CNTS does not allow for a patent to simply claim priority on its face to a certain date, “but rather that it [must] ‘claim priority’ in general” according to the strictures of 35 U.S.C. §§ 112, 120. *See* RRB at 63-64 (citing RX-0054C at *1).

[REDACTED]

Tela and the Staff correctly point out the fatal flaw in this argument. The CNTS states Tela

[REDACTED]

[REDACTED]

[REDACTED] RX-0054C at *1-2; *see* SIB at 94; CRB at 63. As a matter of contract interpretation, this “claim priority” language is not ambiguous—it refers to claims of priority reflected in an issued patent or application for patent instrument (*see* RX-0054C at *1 (defining “Company Patent Right”), 2 (defining “Patent Rights”)), and not any sort of established priority. *See, e.g., Nat. Alts. Int’l, Inc. v. Iancu*, 904 F.3d 1375, 1380 (Fed. Cir. 2018) (citing *In re NTP, Inc.*, 654 F.3d 1268, 1276 (Fed. Cir. 2011)) (“NAI’s ‘vesting’ argument conflates properly claiming priority and demonstrating entitlement to priority. Patent claims ‘are not entitled to an earlier priority date merely because the patentee claims priority.’”). To be sure, 35 U.S.C. § 120 “requires that the invention ‘be disclosed in the manner provided by the first paragraph of section 112’” (RRB at 64), but the CNTS concerns “claim[s]” of priority, not proof of priority (RX-0054C at *1-2). And to merely claim priority, an application need only “contain[] or [be] amended to contain a specific reference to the earlier filed application.” 35 U.S.C. § 120. There is no dispute that the 334 Patent contains such a reference.

As Respondents’ defense depends on an incorrect interpretation of the CNTS, it is not persuasive and the defense fails.

V. U.S. PATENT NO. 10,186,523

A. Level of Ordinary Skill in the Art

As with the 334 patent, a person having ordinary skill in the art of the 523 patent at the time of invention “would have: (1) a bachelor’s degree in electrical engineering or computer engineering with at least three years of experience in the field of semiconductor layout technology

[REDACTED]

and integrated circuit design; (2) a master’s degree in electrical engineering or computer engineering with at least two years of experience in the same field; (3) a bachelor’s degree in physics or materials science with at least five years of experience in the same field; or (4) a comparable combination of education and experience.” Order No. 34 at 8. The parties do not challenge this determination (*see* RIB at 15; SIB at 24; *see generally* CIB; CRB; RRB; SRB), and it is applied throughout this initial determination.

B. Claims-at-Issue

Claims 1-11, 14-20, and 25-28 of the 523 patent are at issue in this investigation, either through allegations of infringement or of the domestic industry technical prong. *See* CIB at 102, 135.⁸ These claims are reproduced below along with additional claim limitation identifiers:

1. [1a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[1b] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein all gate gridlines extend in a y-direction, wherein adjacent gate gridlines are separated from each other by a gate pitch, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated gate gridline,

[1c] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,

[1d] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one

⁸ Again, Tela does not identify claim 25 as infringed, but it is implicated by asserted dependent claim 26.



transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

[1e] at least six gate contact structures formed within the region of the semiconductor chip, the at least six gate contact structures formed in part utilizing corresponding at least six gate contact structure layout shapes as an input to a lithography process, wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures,

[1f] each of the at least six gate contact structure layout shapes having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in an x-direction, each of the at least six gate contact structure layout shapes positioned and sized to overlap both edges of the gate electrode feature layout shape corresponding to the gate electrode feature to which it is in physical and electrical contact; and

[1g] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[1h] wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process,

[1i] wherein the first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, wherein all first-metal gridlines extend in the x-direction, wherein at least eight of the at least eight first-metal gridlines have at least one first-metal structure layout shape positioned thereon, each first-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner on an associated first-metal gridline,

[1j] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein electrical connections within the logic circuit collectively include at least five first-metal structures corresponding to at least five first-metal structure layout shapes respectively positioned on at least five different first-metal gridlines,

[1k] wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding diffusion region, wherein some diffusion

regions within the region of the semiconductor chip are physically and electrically contacted by at least one diffusion contact structure,

[11] the at least one diffusion contact structure formed in part utilizing corresponding at least one diffusion contact structure layout shape as an input to a lithography process,

[1m] each diffusion contact structure layout shape within the region positioned in a substantially centered manner along an associated diffusion contact gridline of a diffusion contact grid, the diffusion contact grid having a diffusion contact gridline-to-diffusion contact gridline spacing measured in the x-direction equal to the gate pitch.

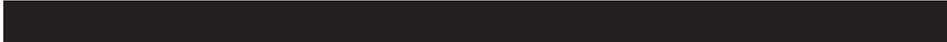
2. [2a] The semiconductor chip as recited in claim 1, further comprising: a second-metal layer formed above the first-metal layer within the region of the semiconductor chip, the second-metal layer positioned second in the stack of metal layers counting upward from top surfaces of the gate electrode features, the second-metal layer separated from the first-metal layer by at least one insulator material,

[2b] the second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to a lithography process, the second-metal layer layout shapes positioned in accordance with a second-metal horizontal grid, the second-metal horizontal grid including at least eight second-metal gridlines,

[2c] wherein all second-metal gridlines extend in the y-direction, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, each second-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline,

[2d] wherein some second-metal structures within the region are electrically connected to at least one first-metal structure within the region through at least one first-metal-to-second-metal via structure, each first-metal-to-second-metal via structure within the region formed in part based on corresponding first-metal-to-second-metal via structure layout shape used as an input to a lithography process, each first-metal-to-second-metal via structure layout shape within the region positioned in a substantially centered manner along an associated second-metal gridline.

3. The semiconductor chip as recited in claim 2, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is either a first width or a second width, the second width different than the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the



first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal layout shape that has the second width.

4. The semiconductor chip as recited in claim 3, wherein at least one gate electrode feature within the region that forms at least one gate electrode of at least one transistor of the first transistor type and does not form a gate electrode of a transistor of the second transistor type is electrically connected to at least one gate electrode feature within the region that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type through an electrical connection that includes at least one first-metal structure and at least one second-metal structure.

5. The semiconductor chip as recited in claim 2, wherein the at least six gate contact structure layout shapes are positioned in accordance with a contact vertical grid, the contact vertical grid including contact gridlines extending in the x-direction, each of the at least six gate contact structure layout shapes positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six gate contact structure layout shapes positioned to also extend lengthwise in the x-direction in a substantially centered manner along a corresponding first-metal gridline.

6. [6a] The semiconductor chip as recited in claim 2, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is one of a plurality of widths, the plurality of widths including a first width and a second width, the first width smaller than the second width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the second width,

[6b] wherein each first-metal-to-second-metal via structure that contacts a first-metal structure formed in part by a first-metal structure layout shape having the first width is formed at least in part by a first-metal-to-second-metal via structure layout shape that is intersected by a corresponding first-metal gridline.

7. The semiconductor chip as recited in claim 6, wherein each first-metal-to-second-metal via structure layout shape is intersected by a corresponding first-metal gridline.

8. The semiconductor chip as recited in claim 2, wherein adjacent second-metal gridlines are separated from each other by a second-metal pitch, the second-metal pitch equal to the gate pitch, the second-metal horizontal grid aligned with the diffusion contact grid.

9. The semiconductor chip as recited in claim 8, wherein all second-metal structure layout shapes in the region of the semiconductor chip have a same width as measured in the x-direction.

10. [10a] The semiconductor chip as recited in claim 9, further comprising: a third-metal layer formed above the second-metal layer within the region of the semiconductor chip, the third-metal layer positioned third in the stack of metal layers counting upward from top surfaces of the gate electrode features, the third-metal layer separated from the second-metal layer by at least one insulator material,

[10b] the third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a lithography process, the third-metal layer layout shapes positioned in accordance with a third-metal vertical grid, the third-metal vertical grid including at least eight third-metal gridlines,

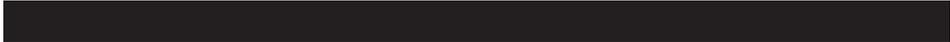
[10c] wherein all third-metal gridlines extend in the x-direction, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, each third-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline,

[10d] wherein some third-metal structures within the region are electrically connected to at least one second-metal structure within the region through at least one second-metal-to-third-metal via structure, each second-metal-to-third-metal via structure within the region formed in part based on corresponding second-metal-to-third-metal via structure layout shape used as an input to a lithography process, wherein at least one second-metal-to-third-metal via structure layout shape within the region is positioned in a substantially centered manner along an associated third-metal gridline.

11. The semiconductor chip as recited in claim 10, wherein each second-metal-to-third-metal via structure layout shape is intersected by a corresponding second-metal gridline.

....

14. The semiconductor chip as recited in claim 1, wherein at least one of the at least six gate contact structures is in physical and electrical contact with, and is substantially centered in the x-direction on, a gate electrode feature within the region that forms at least one gate electrode of at least one transistor of the first transistor type and that does not form a gate electrode of a transistor of the second transistor type.



15. The semiconductor chip as recited in claim 1, wherein each of the at least six gate contact structure layout shapes is intersected by a corresponding gate gridline.

16. The semiconductor chip as recited in claim 1, wherein the first-metal layer includes at least eight first-metal structure layout shapes positioned on four first-metal layer gridlines such that a different two of the at least eight first-metal structure layout shapes is positioned on each of the four first-metal layer gridlines, wherein each of the at least eight first-metal structure layout shapes is positioned next to and spaced apart from at least one other first-metal structure layout shape at a first-metal pitch.

17. The semiconductor chip as recited in claim 1, wherein the at least eight of the at least eight first-metal gridlines that have at least one first-metal structure layout shape positioned thereon are spaced at a first-metal pitch.

18. [18a] The semiconductor chip as recited in claim 1, further comprising: a second-metal layer formed above the first-metal layer within the region of the semiconductor chip, the second-metal layer positioned second in the stack of metal layers counting upward from top surfaces of the gate electrode features, the second-metal layer separated from the first-metal layer by at least one insulator material, the second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to a lithography process, the second-metal structure layout shapes positioned in accordance with a second-metal horizontal grid, the second-metal horizontal grid including at least eight second-metal gridlines, wherein all second-metal gridlines extend in the y-direction, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, each second-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline; and

[18b] a third-metal layer formed above the second-metal layer within the region of the semiconductor chip, the third-metal layer positioned third in the stack of metal layers counting upward from top surfaces of the gate electrode features, the third-metal layer separated from the second-metal layer by at least one insulator material, the third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a lithography process, the third-metal structure layout shapes positioned in accordance with a third-metal vertical grid, the third-metal vertical grid including at least eight third-metal gridlines, wherein all third-metal gridlines extend in the x-direction, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, each third-metal structure layout shape in the region having a substantially rectangular shape

and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline.

19. [19a] The semiconductor chip as recited in claim 18, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is one of a plurality of widths, the plurality of widths including a first width and a second width, the first width smaller than the second width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the second width,

[19b] wherein each first-metal-to-second-metal via structure that contacts a first-metal structure formed in part by a first-metal structure layout shape having the first width is formed at least in part by a first-metal-to-second-metal via structure layout shape that is intersected by a corresponding first-metal gridline.

20. The semiconductor chip as recited in claim 18, wherein some third-metal structures within the region are electrically connected to at least one second-metal structure within the region through at least one second-metal-to-third-metal via structure, each second-metal-to-third-metal via structure formed at least in part by a second-metal-to-third-metal via structure layout shape that is intersected by a corresponding second-metal gridline.

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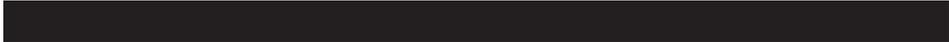
25. The semiconductor chip as recited in claim 1, wherein the at least four transistors of the first transistor type are collectively separated from the at least four transistors of the second transistor type by an inner region that does not include another transistor.

26. The semiconductor chip as recited in claim 25, wherein at least one of the at least six gate contact structure layout shapes is positioned over the inner region and forms a gate contact structure that is in physical and electrical contact with, and is substantially centered in the x-direction on, a gate electrode feature within the region that forms at least one gate electrode of at least one transistor.

27. [27a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip,

[27b] the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[27c] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch,



[27d] each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,

[27e] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,

[27f] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type,

[27g] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

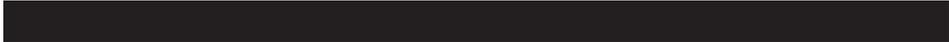
[27h] a number of gate contact structures formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each gate electrode feature that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape,

[27i] wherein each gate contact structure that contacts a given gate electrode feature that forms any transistor gate electrode does not contact another gate electrode feature, wherein any gate contact structure layout shape that has a corresponding length greater than or equal to a corresponding width is oriented to have its corresponding length extend in an x-direction; and

[27j] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[27k] the first-metal layer including first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process,

[27l] wherein each transistor within the region is formed in part by a corresponding diffusion region, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any



transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape,

[27m] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least two first-metal structures form portions of one or more electrical connections within the multiplexer or the latch.

28. [28a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip,

[28b] the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[28c] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes a number of gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch,

[28d] each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,

[28e] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,

[28f] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type,

[28g] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

[28h] a number of gate contact structures formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each of at least six gate electrode features within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape,

[28i] wherein each gate contact structure is centered in an x-direction on the gate electrode feature with which it physical contacts,

[28j] wherein each gate contact structure layout shape that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in the x-direction, wherein each of the number of gate contact structures is in physical contact with only one of any of the gate electrode features; and

[28k] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[28l] the first-metal layer including at least two first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the at least two first-metal structures forming portions of one or more electrical connections within the region of the semiconductor chip,

[28m] wherein each transistor within the region is formed in part by a corresponding diffusion region, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape.

See 523 patent at cls. 1-11, 14-20, 25-28 (annotated).

C. Claim Construction

As part of the *Markman* process, the following terms of the 523 patent were construed, either as agreed between the parties or as determined by Order No. 34:

Claim Term	Construction
“a lithography process”	“a process by which a pattern is imprinted on a resist or semiconductor wafer using light as a mask”
“gate electrode”	“that portion of a gate electrode feature that forms a transistor gate”
“gate electrode feature(s)” / “gate structure(s)”	“a feature comprising a transistor gate”
“diffusion region(s)”	“selected portions of the substrate within which impurities have been introduced to form the



	source or drain of a transistor”
“[gate horizontal / first-metal vertical grid]; [second-metal horizontal] grid; [contact vertical] grid; [third-metal vertical] grid; [diffusion contact] grid”	“projected gridlines used at least during the layout stage of integrated circuit manufacturing”
“[gate / metal / contact] gridline(s)”	“one of the lines making up a grid”
“gate pitch”	“center-to-center separation distance between adjacent gate features”

See generally Order No. 34 at 47, 52, 55, 56, 59, 60, 62. As with the 334 patent, “contact structure(s)” and “gate contact structure(s)” were not construed. *Id.* at 61. The parties do not explicitly identify these terms, or any others, as requiring construction. See RIB at 15-16; SIB at 23-24; see generally CIB; CRB; RRB; SRB. Thus, “contact structure(s)” and “gate contact structure(s)” are addressed below in the infringement and validity determinations to the extent required.

D. Infringement

According to Tela’s post-hearing briefing, the use, manufacture, or sale of the following Accused Products are alleged to infringe the asserted claims of the 523 patent:

Claims	Accused Products Alleged to Infringe
1-11, 14-20, 25, 26	Intel 14nm Products
1-7, 14-20, 25, 26	Intel 10nm Products

See CIB at 102. For the reasons discussed below, Tela has shown infringement for the Broadwell, Skylake, Kaby Lake, Coffee Lake, and Cascade Lake models of Intel 14nm Products under all of the asserted claims, and the Intel 10nm Products under all of the asserted claims.

1. Undisputed Claims

Respondents do not contest Tela's claims of infringement under claims 2-11, 14-20, 25, and 26, apart from their dependency on claim 1, for which infringement is disputed. *See* RIB at 121-44; RRB at 64-79. The Staff similarly has no dispute as to these claims. *See* SIB at 109; SRB at 34-42. In view of the testimony of Dr. Foty that all the relevant Accused Products include the limitations recited in these claims, those identified Accused Products meet the limitations of the dependent claims as alleged. *See* CX-1144C at Q/A 1030-1450, 2135-2385; CIB at 123-135.

2. Disputed Claims

Respondents do, however, contest Tela's claims of infringement of independent claim 1. *See* RIB at 121-144. The Staff similarly contests infringement of this claim. *See* SIB at 98-109. For the reasons discussed below, Tela has shown infringement of claim 1 for the Intel 10nm Products and certain of the Intel 14nm Products.

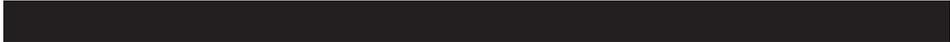
For reference, claim 1 of the 523 patent requires:

1. [1a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[1b] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein all gate gridlines extend in a y-direction, wherein adjacent gate gridlines are separated from each other by a gate pitch, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated gate gridline,

[1c] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,

[1d] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a



gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

[1e] at least six gate contact structures formed within the region of the semiconductor chip, the at least six gate contact structures formed in part utilizing corresponding at least six gate contact structure layout shapes as an input to a lithography process, wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures,

[1f] each of the at least six gate contact structure layout shapes having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in an x-direction, each of the at least six gate contact structure layout shapes positioned and sized to overlap both edges of the gate electrode feature layout shape corresponding to the gate electrode feature to which it is in physical and electrical contact; and

[1g] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[1h] wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process,

[1i] wherein the first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, wherein all first-metal gridlines extend in the x-direction, wherein at least eight of the at least eight first-metal gridlines have at least one first-metal structure layout shape positioned thereon, each first-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner on an associated first-metal gridline,

[1j] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein electrical connections within the logic circuit collectively include at least five first-metal structures corresponding to at least five first-metal structure layout shapes respectively positioned on at least five different first-metal gridlines,

[1k] wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding diffusion region, wherein some diffusion regions within the region of the semiconductor chip are physically and electrically contacted by at least one diffusion contact structure,

[1l] the at least one diffusion contact structure formed in part utilizing corresponding at least one diffusion contact structure layout shape as an input to a lithography process,

[1m] each diffusion contact structure layout shape within the region positioned in a substantially centered manner along an associated diffusion contact gridline of a diffusion contact grid, the diffusion contact grid having a diffusion contact gridline-to-diffusion contact gridline spacing measured in the x-direction equal to the gate pitch.

523 patent at cl. 1 (annotated). Several disputes exist between the parties concerning whether Tela has sufficiently shown the Accused Products meet various limitations of the claim. These are addressed below. In view of the testimony of Dr. Foty that the Accused Products meet those remaining limitations of claim 1 which are not in dispute, the Accused Products have been shown to meet them as alleged. *See* CX-1144C at Q/A 596-1028, 1876-2133; CIB at 102-123.

a. Gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process

First, Respondents and Staff dispute that “the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process” is met in the Intel 14nm Products and the Intel 10nm Products. RIB at 121-132, 143; SIB at 98-105.

For this limitation, Tela, through its expert, identifies certain Intel layout shapes as meeting the “gate electrode feature layout shapes” element. *See* CIB at 102-10 (citing, *inter alia*, CX-1144C at Q/A 683-745), 104 (citing, *inter alia*, CX-1144C at Q/A 1909-1941). One example of these gate electrode layout shapes, for the [REDACTED] cell of certain Intel 14nm Products, is shown below:

CDX-0008C at *2; *see* CX-1144C at Q/A 616. Tela argues “[these] gate electrode feature layout shapes are an input to a lithography process because they are used to generate the set of masks used to pattern the gate electrode features onto the semiconductor chip.” CIB at 103 (citing CX-1144C at Q/A 377-378, 391, 454-456, 675-682). It is these, Tela contends, which are “then used to lithographically pattern features onto a photoresist that is used to define the particular patterns specified by the layout onto the chip through additional processing steps.” *Id.* (citing CX-1144C at Q/A 377-378, 391, 454-456, 675-682); *see* CRB at 67. Tela disputes that the shapes contained on the mask need to correlate or be “essentially identical” to the gate structure layout shapes, as this would be an attempt to limit the claims of the 523 patent to just one of its disclosed embodiments. CIB at 107 (citing *Liebel-Flarsheim*, 358 F.3d 898; 523 patent at Fig. 13A; CX-1144C at Q/A 130; Hr’g Tr. at 853:24-855:8); *see id.* at 108 (“The language ‘formed *in part based on* corresponding gate electrode feature layout shapes,’ merely requires the layout shape to be one part of forming the gate electrode features.”). Lastly, Tela claims “[t]here is no dispute that the gate electrode features in the Intel 14nm and 10nm Products correspond to the gate electrode

[REDACTED]

feature layout shapes specified by the layout” (CIB at 110 (citing CX-1144C at Q/A 391, 427; Hr’g Tr. at 751:19-753:13, 754:4; RX-0007C at Q/A 46)), and notes there is “no dispute that Intel’s M0 layout shapes are an input to a lithography process, despite the fact that [REDACTED] [REDACTED] (CRB at 68 (citing CX-1144C at Q/A 330-348)).

In opposition, Respondents argue Tela’s identification of layout shapes must fail because “it is undisputed that in the accused process nodes Intel [REDACTED] [REDACTED] [REDACTED] RIB at 121-122 (citing Hr’g Tr. at 720:7-11; 980:18-22). Rather, Respondents urge “the dimensions of Intel’s gates are defined using [REDACTED] [REDACTED] [REDACTED] *Id.* at 122 (citing Hr’g Tr. at 719:15-720:11). Respondents reason:

[REDACTED] the identified gate layout shapes are not “used as an input” to a lithography process as claimed, and the Accused Products do not practice this limitation. RX-0014C (Subramanian) at Q/A 295, 325.

Id. Respondents emphasize non-infringement based on the idea that the Asserted Patents, including the 523 patent, are intended to solve problems with a process (lithography) that Intel simply no longer uses because of the small size of its process nodes [REDACTED]

[REDACTED] *See generally id.* at 122-128 (citations omitted), 130; RRB at 64-65.

More specifically, Respondents argue Tela’s identified layout shapes are not those that Intel actually inputs into lithography—those would be the [REDACTED] [REDACTED] shown in the below demonstrative:

[REDACTED]

[REDACTED]

RIB at 128 (citing RDX-0016C at *149). Respondents contend the only “input[s]” to lithography are the shapes on the masks used: “the shapes ‘used as an input to a lithography process’ are those shapes that are actually input into a lithography process, *i.e.*, the shapes on the lithography mask.” See RIB at 130-131 (citing, *inter alia*, RX-1662C at 55:8-18; RX-0014C at Q/A 343-345; RX-1660C at 40:12-15). Yet, Respondents caution, these patterns cannot meet the claims “because they are not the recited *gate* layout shapes,” among other reasons. See RIB at 129 (citing RX-0014C at Q/A 314-316, 320-324); RRB at 69.

Importantly, Respondents claim “[t]he [REDACTED]

[REDACTED]

[REDACTED] CIB at 129 (citing Hr’g Tr. at 720:12-20); RRB at 66 (citing Hr’g Tr. at 716:19-718:4). In their reply brief, they similarly claim “Intel’s gate layout shapes [REDACTED]

[REDACTED]

[REDACTED]

RRB at 65. Respondents argue Intel’s

[REDACTED]

[REDACTED]

[REDACTED] *Id.*

(citing RX-0008C at Q/A 6, 100-102, 122; Hr’g Tr. at 716:19-718:4).

The Staff agrees with each of Respondents’ non-infringement positions. *See generally* SIB at 98-105. The Staff views Tela’s theory as “rel[ying] on drawn poly layouts shapes from the *design* phase to meet this limitation. But it is undisputed that Intel’s drawn poly layout shapes are not used during lithography in the *fabrication* phase.” SIB at 98 (citing Hr’g Tr. at 720:7-11, 980:18-22; RX-0008C at Q/A 110-117) (emphasis in original).

The limitation is met. There is no dispute that the [REDACTED]
[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] *See* RX-0008C at Q/A 6;

CIB at 103 (citing CX-1144C at Q/A 377-378, 391, 454-456, 675-682); RRB at 65-66. In describing the three mask shapes reproduced above in RDX-0016C at *149, Dr. Subramanian correctly states that [REDACTED] (RX-0014C at Q/A 310), but he does not state they [REDACTED]

[REDACTED] Intel witness [REDACTED]

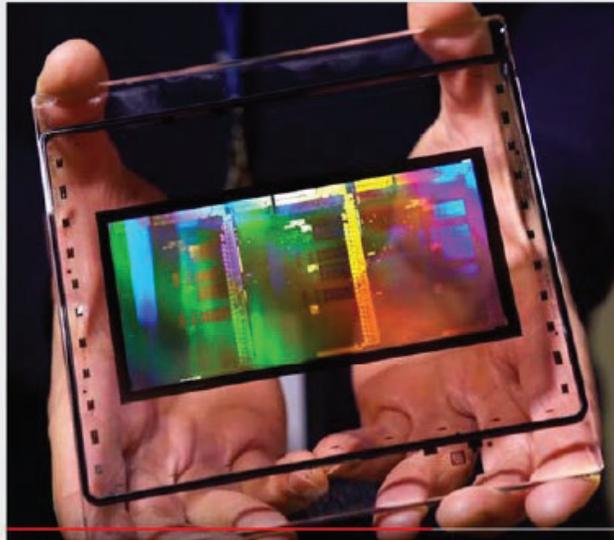
[REDACTED] Hr’g

Tr. at 1014:2-20. Further, Dr. Subramanian himself effectively admitted [REDACTED]

[REDACTED] according to where gate structures are positioned in the

design layout. *Compare* Hr’g Tr. at 913:2-917:11 *with id.* at 918:20-23. Dr. Auth testified similarly. *See id.* at 751:19-756:6 (discussing RDX-0010C at *22). Thus, there is no real merit to

Lithographic Photomask (Mask)



RDX-0018

RDX-0010.0008

Q. How are Intel's masks manufactured?

A. [REDACTED]

Q. You mentioned these masks are fed into a lithography machine. Turning to RDX-0010.0009, what does a lithography machine look like?

A. This is an image captured from a video RDX-0019. It shows the insides of a lithography machine [REDACTED]

[REDACTED] The purple color indicates where light is being shone through a sequence of mirrors, through a mask, and onto a wafer below.

[REDACTED]

RX-0008C at Q/A 24-26; RDX-0010 at *8, 9. Other witnesses testified that there are other inputs to the lithography process, including Tela witnesses John Malecki (RX-1660C at 40:12-15 (“Q. From Tela’s point of view, the input to the lithography process would be the GDS2 files that specify the mask shapes? A. Yes. Yes.”)) and Dhrumil Gandhi (*see* RIB at 131 (citing RX-0014C at Q/A 344; RX-1662C at 55:8-12) (GDSII file shapes are OPC-modified before mask creation)), and Dr. Subramanian (RX-0014C at Q/A 611 (“if OPC is applied, the input to the lithography process would be the OPC shapes to meet the claims”)).

With this understanding, Respondents’ and the Staff’s additional arguments regarding [REDACTED] are irrelevant. The limitation only requires the “gate electrode features” to be “formed in part” by a lithography process which takes into account or “use[s]” gate feature layout shapes (523 patent at cl. 1)—an act which Respondents acknowledge is the first step in the process (*see, e.g.*, RX-0008C at Q/A 103; RX-0014C at Q/A 295; RRB at 65). Thus, the limitation is met in the Accused Products.

[REDACTED]

b. Gate electrode feature layout shapes positioned in accordance with a gate horizontal grid

Second, the Staff, but not Respondents, disputes whether “gate electrode feature layout shapes positioned in accordance with a gate horizontal grid” is met in the Intel 14nm Products and Intel 10nm Products. SIB at 105. Order No. 34 construed “grid” as “projected gridlines used at least during the layout stage of integrated circuit manufacturing.” Order No. 34 at 59.

For this limitation, Tela again refers to Intel’s alleged “1-D gridded approach” and explains that [REDACTED] for the Intel 14nm Products “defines the ‘gate horizontal grid,’ and the gate electrode feature layout shapes are positioned and centered along gate gridlines in the y-direction” (CIB at 102 (citing, inter alia, CX-1144C at Q/A 683-745; CPX-0497C at -762; RX-0008C at Q/A 138; Hr’g Tr. at 801:1-802:7); CRB at 69), and a [REDACTED] similarly defines the grid in the Intel 10nm Products (CIB at 104-105 (citations omitted); CRB at 69). Tela provides the following two examples from 14nm and 10nm layout files:



CIB at 103 (citing CDX-0008C at *12), 105 (citing CDX-0010C at *6).

[REDACTED]

The Staff contends that “[b]ecause Intel designers use a [REDACTED] [REDACTED] to place the gate and metal features in accordance with the pitch and spacing requirements as set forth by the design rules, Intel’s 14nm and 10nm Accused Products do not practice this limitation, as Dr. Foty admits.” SIB at 105 (citing CX-1144C at Q/A 552; Hr’g Tr. at 399:4-400:19).

As determined above with respect to the similar limitation in the 334 patent, this limitation is met in the Accused Products. The layout files cited by Tela and Dr. Foty show [REDACTED] [REDACTED] between the gate electrode feature layout shapes—*i.e.*, their positioning is in a grid. And Intel documentation shows this arrangement, or positioning, was “in accordance” with a planned layout (*i.e.*, not happenstance). That Intel also uses a different, 1nm drawing grid for designers, as the Staff argues, is beside the point. *See* Hr’g Tr. at 399:15-400:9.

c. First-metal structure layout shapes are positioned in accordance with a first-metal vertical grid

Third, Respondents and Staff dispute whether “first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid” is met in the Intel 14nm Products and Intel 10nm Products. RIB at 132-141, 143; SIB at 105-106.

For this limitation, Tela again refers to a “1-D gridded approach” within the Accused products and explains, per design rules, that the first-metal structures are [REDACTED] [REDACTED] CIB at 115 (citing, *inter alia*, CX-1144C at Q/A 330-331, 887-916; CPX-0497C at -780), 117 (citing CX-1144C at Q/A 358-362, 2032-2051; CPX-0341C at -5851; CPX-0097C at -151). Additionally, Tela argues the design rules, as discussed above, specify [REDACTED] [REDACTED] *See id.* at 116, 117 (citations omitted).

[REDACTED]

Respondents argue, as they did with the corresponding limitation of the 334 patent, that the [REDACTED]

[REDACTED] See RIB at 133-136, 143.

Again, Respondents emphasize [REDACTED] (*id.* at 136 (citing Hr’g Tr. at 728:2-16)) as resulting in [REDACTED] [REDACTED] (*id.* (citing Hr’g Tr. at 726:9-727:12; RX-0008C at Q/A 136-144); RRB at 72-73). According to Respondents, “it is undisputed that Intel’s *actual* Metal-0 features [REDACTED] [REDACTED] Accordingly, based on Dr. Foty’s own definition of the function of a ‘grid,’ Intel does not practice the first metal ‘grid’ limitation.” RIB at 137 (citing Hr’g Tr. at 200:1-6) (emphasis in original). Respondents also argue that Dr. Foty and Tela cannot show the presence of a “grid” on layout file images unless the gridlines are a part of those files. *See id.* at 138 (“Given that unavoidable fact, in order to conjure up an alleged grid, Dr. Foty is forced to draw *his own* dotted lines over the shapes”), 141 (“Dr. Foty’s ex-post drawing of dotted lines along shapes that have already been positioned cannot meet a construction that requires Intel to have projected those gridlines during layout.”); RRB at 72 [REDACTED] [REDACTED] Tela has no answer for this fundamental flaw”), 76 (“[T]he point remains the same— [REDACTED] [REDACTED]”), 77-79. The Staff agrees with Respondents’ positions on the issue. *See* SIB at 105-106 (“[T]here is no defined ‘grid’ that shapes must be positioned in accordance with—whether by uniform pitch or otherwise.”); SRB at 40-41 (“In the Staff’s view, because Intel does not define any ‘grid’ for the Metal-0 shapes to be positioned along, the Accused Products also do not satisfy the claimed requirement that the ‘first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid.”).

[REDACTED]

As with the '334 patent, the limitation is met in the Accused Products. The layout files cited by Tela and Dr. Foty show [REDACTED]

[REDACTED] See CX-1144C at Q/A 887-900, 2033-2043; CDX-0008C at *62-67; CDX-0010C at *37-39. As to Respondents' argument that "[u]ltimately, Tela effectively interprets the claims to require nothing more than rectangular, parallel shapes—while improperly ignoring the additional grid limitations, which are indisputably not met" (RRB at 73), there is nothing more to a "grid" than an arrangement of rectangular, parallel shapes. Inasmuch as the term "grid" requires construction, that is its plain and ordinary meaning.

Also as with the 334 patent, requiring a uniform pitch between these layout shapes per a construction of "grid" (*see, e.g.*, RIB at 137 ("it is undisputed that Intel's actual Metal-0 layer does not meet the requirement of having uniformly spaced feature locations (*i.e.*, gridlines)"); RRB at 74 ("Intel does not practice the Metal-0 limitation because it is undisputed that the Metal-0 layer's layout shapes are not restricted to regularly spaced gridlines.)) is inappropriate. The first-metal "grid" of claim 1 is not bound by any such restriction as opposed to, for example, claim 8, which requires a second-metal layer grid defined by "*a* second-metal pitch, the second-metal pitch equal to the gate pitch," and claim 17, which requires eight first-metal gridlines "spaced at *a* first-metal pitch." *Id.* at cls. 8, 17 (emphases added). Under principles of claim differentiation, it would thus be improper to read in *a* pitch (*i.e.*, the same pitch), or any defined amount of pitch, into the basic claim term of "grid." *Curtiss-Wright*, 438 F.3d at 1380; *see Karlin Tech., Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 971-72 (Fed. Cir. 1999) ("different words or phrases used in separate claims" are presumed to indicate "the claims have different meanings and scope"). Accordingly, the limitation is met.

[REDACTED]

d. Each gate gridline has at least one gate electrode feature layout shape positioned thereon

Fourth, Respondents dispute whether “each gate gridline has at least one gate electrode feature layout shape positioned thereon” is met in the Intel 14nm Products and Intel 10nm Products, whereas the Staff only disputes the limitation for the Intel 10nm Products. RIB at 141-144; SIB at 107. For this limitation, Tela incorporates its discussion of the same limitation for the 334 patent. *See* CIB at 110; CRB at 69.

In opposition, Respondents note “gate electrode feature” is construed the same as “gate structure” in the 334 patent—a “feature comprising a transistor gate”—and Tela relies on the same gridlines for the 523 patent as it did for the 334 patent. *See* RIB at 141-142. Respondents thus incorporate their argument as to non-infringement of the 334 patent. *See id.* at 141-144; RRB at 79. The Staff similarly adopts its positions as in the 334 patent—the limitation is met for the Intel 14nm Products but not for the Intel 10nm Products. *See* SIB at 107; SRB at 41. For the Intel 10nm Products, the Staff notes Tela fails to acknowledge that Dr. Foty identified more gridlines than the seven the claim requires, the result of which is a gridline clearly not including a gate electrode feature. *See* SRB at 41 (citing CDX-0010C at *12).

Tela has identified and relies on the same gridlines for each cell as it did under the 334 patent. *See* CX-1144C at Q/A 725-733, 1932-1937; CDX-0008C at *9-21; CDX-0010C at *6-13. Under the same reasoning, given above, the following cells from the Intel 14nm Products have not been shown to meet this limitation: [REDACTED]

[REDACTED] Dr. Foty’s demonstratives indicate the latter three cells comprise the entirety of cells for the Goldmont, Goldmont Plus, Ice Lake Chipset, and Cannon Lake Chipset products. CDX-0012C at *25-26. Thus, the Accused Products including these models do not infringe. The

[REDACTED]

remaining Intel 14nm Products use one or both of [REDACTED] so they meet the limitation. And all of the Intel 10nm Products meet the limitation.

- e. **At least six gate contact structures formed within the region of the semiconductor chip . . . wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures**

Fifth, the Staff, but not Respondents, disputes whether “at least six gate contact structures formed within the region of the semiconductor chip . . . wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures” is met in the Intel 10nm Products. SIB at 107. No party disputes the limitation is met in the Intel 14nm Products.

For this limitation, and the Intel 10nm Products in particular, Tela argues the [REDACTED] gate contact layout shapes are sized and positioned to overlap both edges of the surface of the gate structure to which it is in physical and electrical contact. CIB at 113-114 (citing, *inter alia*, CX-1144C at Q/A 315-319, 1964, 1980-1995; CPX-0341C at -5827-5828; CPX-0030C at -1493; CX-0662 at *7, 9). Tela does not address the limitation in its reply brief. *See generally* CRB at 65-71.

In opposition, the Staff argues that Intel’s [REDACTED]

[REDACTED]

in the Intel 10nm Products. SIB at 107 (citing RX-0014C at Q/A 160-161, 166); SRB at 41.

Given this argument, it is unclear to me on what grounds the Staff is challenging the limitation. The Staff incorporates its argument from the 334 patent (*see* SIB at 107; SRB at 41), but in that discussion acknowledges direct physical contact between gate features and other M0 contact structures in the Intel 10nm Products, stating “[t]he evidence clearly shows that in TEM images of Intel’s 10nm Accused Product, the gate-contacting portion of M0 is the same width as

[REDACTED]

the gate, and thus not ‘sized to overlap both edges of the top surface of the gate structure.’” SIB at 41. To the extent Staff’s concern is that Tela attempts to show this limitation with layout files and other illustrations (*see, e.g.*, SIB at 41) which is insufficient for a limitation concerning actual structures rather than imagery of actual structures (*see, e.g.*, SIB at 41), layout files are circumstantial evidence of actual structure, and the Staff does not dispute that there is physical and electrical contact in the actual structures. In any event, direct teardown evidence confirms the required contact. *See* RDX-0010 at *34; RX-0008C at Q/A 162. Thus, the limitation is met.

f. Diffusion region

Sixth, Respondents and Staff dispute whether “diffusion region” is met in the Intel 14nm Products and Intel 10nm Products. RIB at 142, 144; SIB at 108.

Tela argues that “[t]he diffusion regions are defined by the portions of the diffusion region layout shape to the sides of the gate (poly) layout shape” and “[t]he source and drain regions of the transistors in the Intel 14nm and 10nm Products are formed within the diffusion region specified in the layout.” CIB at 120 (citing CX-1144C at Q/A 127, 267-269, 953, 2081). To be clear, as with the 334 patent, Tela identifies “source and drain regions” in the Accused Products as the claimed “diffusion region[s]”:

Indeed, the Intel documentation describes that [REDACTED] (Tr. (Auth) at 652:6-12; RPX-1997 at 90237DOC0000307 [REDACTED] 90237DOC0000319 [REDACTED] RPX-2021 at 90237DOC0001048, 90237DOC0001060 (same).) As such, *these regions are “diffusion regions” under the ALJ’s construction* because they are “selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor.”

Id. at 120-121 (emphasis added).

[REDACTED]

In opposition, Respondents incorporate their discussion of the same limitation in claim 15 of the 334 patent. RIB at 142, 144; RRB at 79. The Staff incorporates similarly. SIB at 108; SRB at 42.

As determined above in connection with the same limitation in claim 15 of the 334 patent, the Accused Products' [REDACTED] and therefore not literally “substrate” as required by the construction for “diffusion region.” While not explicit on this point, however, Tela’s reply brief contends the [REDACTED] structures qualify as “diffusion region[s]” under the doctrine of equivalents, as in the 334 patent. *See* CRB at 69 (citing CRB at 19-28). As determined above, the evidence supports this assertion. Accordingly, the Accused Products meet this limitation.

g. Diffusion contact structure

Seventh, Respondents and Staff dispute whether “diffusion contact structure” is met in the Intel 14nm Products and Intel 10nm Products. RIB at 142, 144; SIB at 108-109. “Contact structure” was not previously construed, nor was “diffusion contact structure.” *See* Order No. 34 at 61.

For this limitation, Tela argues “[i]n the Intel 14nm and 10nm Products, the diffusion regions are physically and electrically contacted by a diffusion contact structure [REDACTED] which “physically contacts the [REDACTED] source and drain regions to form an electrical connection to other features.” CIB at 121 (citing, *inter alia*, CX-1144C at Q/A 267, 297-300, 311-314, 317, 320, 953, 2081; CPX-0097C at -146; CPX-0341C at -5815-5824; CPX-0497C at -771). Tela also points to Intel documentation on the 10nm process which describes [REDACTED] [REDACTED] *Id.* (citing JX-0239 at *3; Hr’g Tr. at 669:2-670:22); CRB at 70. Tela rejects a requirement that this contact structure must be separate from any other, such as gate contacts, citing Order No. 34. *See* CRB at 70 n.16 (citing Order No. 34 at

[REDACTED]

60-61). Even then, Tela argues, there is at least one diffusion contact structure which is clearly separate from the gate contacts. *See id.* (citing CX-1144C at Q/A 989-1000, 2100-2108).

In opposition, Respondents argue that the Accused Products lack these structures and that those identified by Tela “do not physically and electrically contact the substrate or any diffusion region therein, nor do they otherwise involve ‘diffusion’ of any kind.” RIB at 142 (citing RX-0014C at Q/A 130-133; RX-0008C at Q/A 84-98), 144 (citing RX-0014C at Q/A 130-133; RX-0008C at Q/A 84-98). Respondents allege Tela and Dr. Foty fail to address the requirement “that these be ‘diffusion contact’ structures (as opposed to other types of contact structures)” *Id.* at 142; *see id.* at 144. The Staff agrees and adds, specifically, “Intel’s gate contacts and diffusion contact functionalities are [REDACTED]

[REDACTED] *See* SIB at 108 (citing RX-0014C at Q/A 139-144; *HTC Corp. v. Cellular Commc’ns Equip. LLC*, 701 F. App’x 978, 982 (Fed. Cir. 2017)). This, the Staff argues, is in addition to the fact that these structures do not contact substrate or any diffusion region in the substrate. *See id.* at 108-109 (citing CX-1144C at Q/A 131; RX-0008C at Q/A 84-98).

Respondents’ argument depends on the absence of a “diffusion region” already discussed above, as opposed to actually identifying and discussing what structures the accused [REDACTED] do physically and electrically contact. *See* RX-0014C at Q/A 130-133. And in fact, Respondents’ witness, Dr. Auth, testified that the [REDACTED] sources and drains discussed above. RX-0008C at Q/A 95. This meets the plain and ordinary meaning of “diffusion contact structure” as a structure which contacts what has been alleged as the “diffusion region” under the claim. Inasmuch as construction of this limitation is required, that plain and ordinary meaning is adopted.

[REDACTED]

As to the Staff’s contention that the limitation cannot be met because “Intel’s gate contact and diffusion contact functionalities are [REDACTED] (SIB at 108), Tela correctly points out that the claim requires only “at least one diffusion contact structure” (523 patent at cl. 1) and, assuming a need for separateness, the Staff’s cited evidence does not show all accused diffusion contacts also serve as gate contacts (SIB at 108 (citing RX-0014C at Q/A 139-144; RDX-0016C at *64)). The fact that they may otherwise be in the same “layer” is immaterial and does not conflict with the language of the claims.

Accordingly, the limitation is met in the Accused Products.

E. Domestic Industry – Technical Prong

According to Tela’s post-hearing briefing, the construction or use of the DI Products practice claims 27 and 28 of the 523 patent. *See* CIB at 135. For the reasons discussed below, Tela has not shown by a preponderance of the evidence that the DI Products practice the claims.

1. Product Representativeness

As determined above, Tela has not shown the Exynos 7420 is representative of the other DI Products (S5E7570, S5E7870, S5E7880, S5E7883, and S5E8890) such that practice of the claims of the Asserted Patents by the Exynos 7420 suffices for the other products as well. Nevertheless, the following discussion of particular claim limitations assumes all products are represented by the Exynos 7420.

2. Disputed Claims

Respondents contest Tela’s alleged practice of claim 27 but do not address claim 28. *See* RIB at 145-148; RRB at 79-81. The Staff takes the same position on claim 27, but contends claim 28 is also not practiced on identical grounds. SIB at 110-112. The evidence shows Tela has not shown direct practice of either claim.

a. Claim 27

For reference, claim 27 of the 523 patent requires:

27. [27a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip,

[27b] the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[27c] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes at least seven gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch,

[27d] each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,

[27e] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,

[27f] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type,

[27g] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

[27h] a number of gate contact structures formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each gate electrode feature that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape,

[27i] wherein each gate contact structure that contacts a given gate electrode feature that forms any transistor gate electrode does not contact another gate electrode feature, wherein any gate contact structure layout shape that has a corresponding length greater than or equal to a corresponding width is oriented to have its corresponding length extend in an x-direction; and

[27j] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[27k] the first-metal layer including first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process,

[27l] wherein each transistor within the region is formed in part by a corresponding diffusion region, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape,

[27m] wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least two first-metal structures form portions of one or more electrical connections within the multiplexer or the latch.

523 patent at cl. 27 (annotated). Several disputes exist between the parties concerning whether Tela has shown the DI Products meet the limitations of the claim. These are addressed below. In view of the testimony of Dr. Foty that the DI Products practice those remaining limitations which are not in dispute, the DI Products have been shown to practice them as alleged. *See* CX-1144C at Q/A 2709-2967; CIB at 135-140.

i. Gate electrode feature layout shapes positioned in accordance with a gate horizontal grid

First, as with the 334 patent, Respondents and Staff dispute whether “gate electrode feature layout shapes positioned in accordance with a gate horizontal grid” is met in the DI Products. RIB at 148; SIB at 111.

For this limitation, Tela contends “Samsung’s 14LPP and 14LPC design manuals specify the [REDACTED] which are used as an input to a lithography process to form gate electrode features.” CIB at 135-136 (citing CX-1144C at Q/A

[REDACTED]

2766-2770; CX-0727C at *38, 133; CX-0726C at *46, 162). Tela claims a teardown analysis also shows practice of the limitation (*see id.* at 136; CRB at 71 (“[M]asks are not necessary to show infringement.”)) and Respondents’ expert, Dr. Subramanian, “had no doubt that the Exynos 7420 chip would be manufactured from a layout designed in accordance with Samsung design rules” (CIB at 136 (citing Hr’g Tr. at 937:20-939:5)).

In opposition, Respondents emphasize Tela’s failure to offer any “documents, testimony, or any other evidence describing Samsung’s layout stage at all, let alone establish that any such gridlines were used during layout.” RIB at 148 (citing RX-0014C at Q/A 437, 559-666). “Accordingly,” Respondents argue, “Tela has not met its burden of proving that the alleged DI products practice this limitation.” *Id.*; *see* RRB at 81 (“[N]o evidence of record . . . that the claimed ‘grid’ and ‘gridlines’ are used in the manner claimed.”). The Staff, on the other hand, argues “[t]he DI products do not satisfy this limitation for the same reasons described above for non-infringement by the Intel Accused Products.” SIB at 111; SRB at 43.

As determined above in the context of the 334 patent, the evidence shows the DI Products contain actual gate electrode features positioned in accordance with a gate horizontal grid, based in no small part on actual teardown imagery of the Exynos 7420 showing linear, parallel arrangement to these structures. *See, e.g.*, JX-0215 at *9. This limitation, however, requires not actual structures, but layout shapes, positioned in accordance with a gate horizontal grid. The record supports finding that such layout shapes exist and are so positioned. Dr. Subramanian conceded that the DI Products would be manufactured in accordance with the design rules concerning layout of gate structures. Hr’g Tr. at 937:20-939:5. Those rules are contained in CX-0727C and CX-0726C, and Dr. Foty testified as to how these documents refer to [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]. CX-1144C at Q/A 107, 2657, 2769-2778; *see* CX-0727C at -38, -133. Thus, it is more likely than not the limitation is met, despite the absence of actual layout files in the record. To the extent the Staff argues the limitation is not met because no further specificity on the “grid” is provided in the design rules, or for the lack of an actual, observable projection of a “grid,” those reasons are not persuasive, as discussed in the context of infringement under the 334 patent.

ii. Gate electrode feature layout shapes used as an input to a lithography process

Second, the Staff, but not Respondents, disputes whether “gate electrode feature layout shapes used as an input to a lithography process” is met by the DI Products. SIB at 110-111.

Tela contends “Samsung’s 14LPP and 14LPC design manuals specify the [REDACTED] [REDACTED] which are used as an input to a lithography process to form gate electrode features.” CIB at 135-136 (citing CX-1144C at Q/A 2766-2770; CX-0727C at *38, 133; CX-0726C at *46, 162). Tela claims a teardown analysis also shows practice of the limitation (*see id.* at 136; CRB at 71 (“[M]asks are not necessary to show infringement.”)), and Respondents’ expert, Dr. Subramanian, “had no doubt that the Exynos 7420 chip would be manufactured from a layout designed in accordance with Samsung design rules” (CIB at 136 (citing Hr’g Tr. at 937:20-939:5)).

The Staff criticizes Tela for “offer[ing] no direct evidence regarding Samsung’s design layout or SAS’s mask shapes that are used during Samsung’s lithography process versus the structures in the final product.” SIB at 110. Thus, according to Staff, there is insufficient evidence to show practice of the claim. *See id.* at 110-111 (citing RX-0014C at Q/A 606-612); SRB at 42-43.

The limitation is more likely than not practiced by the DI Products, albeit through circumstantial evidence. As determined above, the evidence supports finding that “gate electrode

[REDACTED]

feature layout shapes” are used by Samsung in the creation of the DI Products, and are positioned in accordance with a grid. Thus, the issue becomes whether these “gate electrode layout shapes” are also used as an input to a lithography process.

As explained in the infringement discussion above, “used as an input” encompasses Intel’s use of design layout shapes as a starting point to create backbone and cut mask shapes for lithography, where that lithography is just the first step in a process called spacer-defined double (or quad) patterning. *See, e.g.*, RX-0008C at Q/A 31-32, 99-115. Dr. Subramanian considered teardown analyses and Samsung’s design rules to conclude that Samsung utilizes the same process. *See* RX-0014C at Q/A 598-606 (“It is my opinion that Samsung likely uses SADP to form its metal gates. In any event, Dr. Foty has not provided evidence to refute that it does.”). Dr. Foty, also considering Samsung’s design rules, points to [REDACTED] as evidence that gate electrode feature layout shapes are created and then used in a lithography process. CX-1144C at Q/A 2769-2770. Thus, on balance, a preponderance of the evidence supports finding the DI Products meet this limitation, essentially in the same way as the Accused Products.

iii. Diffusion Regions

Third, as with the 334 patent, Respondents and Staff dispute that the DI Products have any “diffusion region[s].” RIB at 145; SIB at 111-112. Tela again points to the [REDACTED] in Samsung’s LPP and LPC design manuals, as evidence of this claim element. CIB at 139-140; CRB at 71-72. As determined above, the DI Products’ epitaxially grown sources and drains are new material and therefore not literally “substrate” as required by the construction for “diffusion region.” Again, though, Tela alleges the limitation is practiced under the doctrine of equivalents, which, again, the record supports. CRB at 71-72 (citing CRB at 19-28). Thus, the limitation is practiced.

[REDACTED]

iv. Formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process

Fourth, Respondents and Staff contend that, should the DI Products be found to contain “diffusion region[s],” they are not “formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process.” RIB at 145-148; SIB at 111-112.

For this limitation, Tela contends the [REDACTED] in the DI Products, is “formed in part based on corresponding diffusion layout shapes in, at least, a GDSII file that is used as an input to a lithography process.” CIB at 140 (citing CX-1144C at Q/A 2931-2936; CX-0727C at *37, 138, 141; CX-0726C at *46, 168, 171); *see* CRB at 72.

In opposition, Respondents again note the lack of discovery from non-party Samsung and state “the record does not contain any layout files for Samsung chips.” RIB at 145 (citing RX-0014C at Q/A 616); RRB at 80 (“the ‘GDSII file’ Tela references is purely hypothetical; there is no Samsung GDSII file in the record.”). Thus, according to Respondents, “[t]here is no evidence of which layout shapes, if any, are utilized as an input to lithography,” and Tela cannot meet its burden. RIB at 146; *see* RRB at 80-81. Respondents also note that the acknowledged epitaxially grown source and drain regions are “fundamentally non-lithographic.” RIB at 146 (citing RX-0014C at Q/A 619); *see generally* RIB at 146-148. The Staff agrees with this position. SIB at 111-112; SRB at 43-44.

The limitation is not practiced given the fact, which Respondents allege and Tela does not dispute, that [REDACTED] sources and drains are fundamentally non-lithographic. Indeed, Tela has offered no explanation of how lithography plays a role, even “in part,” in source and drain creation. Thus, in contrast with gate electrode features, which do involve lithography, there can be no diffusion regions “formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process.”

[REDACTED]

v. Substantially rectangular shape

Fifth, Respondents and Staff dispute that the DI Products contain “diffusion region layout shapes” that are “substantially rectangular.” RIB at 145; SIB at 111-112.

Tela contends the [REDACTED] of the DI Products have corresponding diffusion layout shapes within, “at least, a [REDACTED]” CIB at 140. Tela further contends these [REDACTED] are rectangular, [REDACTED] *Id.* (citing CX-1144C at Q/A 2931-2946; CX-0727C at *37, 138, 141; CX-0726C at *46, 168, 171); CRB at 72.

Tela has not sufficiently shown a rectangular shape for these layout shapes. Given the absence of actual layout files, the shape of “*each* diffusion region” for “*each* transistor” within the overall “region of the semiconductor chip” in satisfaction of the claim (*see* 523 patent at cl. 27) cannot be drawn from brief imagery on the cited pages of Samsung’s LPP and LPC design rules (CX-0727C at *37, 138, 141; CX-0726C at *46, 168, 171; *see* RIB at 146, 147 (citing RX-0014C at Q/A 618; CX-1144C at Q/A 2934)). Therefore, this limitation is not met by the DI Products.

b. Claim 28

For reference, claim 28 of the 523 patent requires:

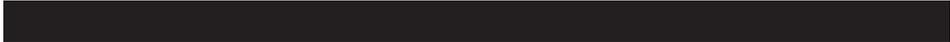
28. [28a] A semiconductor chip, comprising: gate electrode features formed within a region of the semiconductor chip,

[28b] the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a lithography process,

[28c] the gate electrode feature layout shapes positioned in accordance with a gate horizontal grid that includes a number of gate gridlines, wherein adjacent gate gridlines are separated from each other by a gate pitch,

[28d] each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline,

[28e] wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon,



[28f] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type,

[28g] wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

[28h] a number of gate contact structures formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each of at least six gate electrode features within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape,

[28i] wherein each gate contact structure is centered in an x-direction on the gate electrode feature with which it physical contacts,

[28j] wherein each gate contact structure layout shape that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in the x-direction, wherein each of the number of gate contact structures is in physical contact with only one of any of the gate electrode features; and

[28k] a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material,

[28l] the first-metal layer including at least two first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the at least two first-metal structures forming portions of one or more electrical connections within the region of the semiconductor chip,

[28m] wherein each transistor within the region is formed in part by a corresponding diffusion region, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape.



523 patent at cl. 28 (annotated). As noted above, Respondents do not explicitly challenge practice of claim 28, but the Staff does, for all of the same reasons discussed with respect to claim 27: both claims require “diffusion region,” “diffusion region layout shape . . . formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process,” “a substantially rectangular shape,” and “gate electrode feature layout shapes used as an input to a lithography process.” See SIB at 110-112. As determined above, the DI Products do not practice claim 27. Accordingly, the DI Products also have not been shown to practice claim 28.

F. Validity

Respondents and the Staff identify and discuss the following invalidity theories for the 523 patent:

Claims	Theory
1- 11, 14-20, 25, 26, 27, 28	Rendered obvious under 35 U.S.C. § 103 by Kitabayashi (JX-0267) and Intel 45nm Products and/or Maziasz and Hayes (RX-0028)
27	Lack of written description 35 U.S.C. § 112, ¶ 1

See generally RIB at 148-171. The Staff agrees that claim 27 fails the written description requirement, but does not assert obviousness as to any claim. See SIB at 112-114. Claim 27 is pertinent only to the technical prong of domestic industry. See RIB at 148; SIB at 83-84. Thus, because indefiniteness is not an asserted ground of invalidity of claim 27, the parties’ dispute over that claim need not be resolved or otherwise addressed. *Silicon Microphone Packages*, Inv. No. 337-TA-695, Notice at 3. Thus, only the obviousness theory remains.

Before turning to the merits of that theory, the priority date of the 523 patent must be established. The 523 patent claims priority to the 2006 Provisional Application and lacks the new

[REDACTED]

matter added to the 731 Application in 2015. *See* 523 patent at 1:13-28. And Respondents do not allege that its asserted priority date is erroneous. *See* RIB at 149. Therefore, the 523 patent’s presumptive priority date is March 9, 2006.

With this date in mind, Respondents assert three prior art references in an obviousness combination: (1) Kitabayashi; (2) the Intel 45nm Products; and (3) the textbook entitled “Layout Minimization of CMOS Cells” by Maziasz and Hayes. RX-0007C at Q/A 91. Tela does not expressly dispute that Kitabayashi and Maziasz and Hayes are prior art. *See* CIB at 144. Kitabayashi was filed as a U.S. Patent Application in 2004 and issued in 2007, and the earliest date Tela asserts as the 523 patent’s conception date is October 22, 2005, so Kitabayashi is prior art because it is a patent “granted on an application for patent by another filed in the United States before the invention by the applicant for patent.” 35 U.S.C. § 102(e) (2002); RX-0267; *see* CIB at 152. And Maziasz and Hayes was published in 1992, well before the 523 patent’s priority date. *See* RX-0028.

Whether the Intel 45nm Products are prior art under the pre-AIA version of Section 102(g) is a closer question, however, requiring more scrutiny than with the 334 patent. Tela contends that the inventions claimed in the 523 patent were conceived no earlier than October 22, 2005, and constructively reduced to practice by the filing of the 2006 Provisional Application on March 9, 2006. *See* CIB at 152-153. Respondents point to corroborated evidence that the Intel 45nm Products were conceived no later than June 27, 2005, and contend they were actually reduced to practice no later than January 25, 2006. *See* RIB at 78, 80; RX-0007C at Q/A 234. Therefore, the question presented is whether the Intel 45nm Products were actually reduced to practice before March 9, 2006, and not abandoned, suppressed, or concealed; if so, diligence is immaterial. *See Fox Group*, 700 F.3d at 1304.

[REDACTED]

As noted, the Intel 45nm Products consist of the test chip and the Penryn chip. *See* RIB at 77. A press release and a Powerpoint presentation state that Intel successfully demonstrated its test chip no later than June 27, 2005, and that it was “on track to manufacture chips with this technology in 2007.” JX-0278; *see* JX-0275. Tela criticizes this evidence as uncorroborated. *See* CIB at 83 (citing *In re Garner*, 508 F.3d 1376, 1381 (Fed. Cir. 2007)). *Garner*, however, applies a “rule of reason” analysis, where “evidence of surrounding facts and circumstances independent of information received from the inventor” may be sufficient to corroborate reduction to practice. 508 F.3d at 1380 (quoting *Price v. Symsek*, 988 F.3d 1187, 1195 (Fed. Cir. 1993)). Dr. Subramanian itemizes the pertinent design documents, which were written between May 2004 and October 2005. *See* RX-0007C at Q/A 242-253. The timeline of these documents is consistent with what would be expected in the leadup to Intel’s public announcement of a “[f]ully functional” test chip in January 2006, and the announcement itself was supported by photographs of a chip and images of what even Tela describes as a portion of its gate layer. JX-0275 at 3; *see* JX-0278; CIB at 83. To be sure, Respondents offer no test results to explicitly demonstrate that the test chip “would work for its intended purpose,” but the Penryn chip’s commercial release in 2007 (as predicted by Intel in its 2006 press release), combined with the other evidence offered, is adequate to satisfy that standard under a “rule of reason.” *Garner*, 508 F.3d at 1380; *see* RX-0001C at Q/A 34 (“Intel completed testing” by January 2006 “to ensure that it worked for its intended purpose”), 58. And as with the 334 patent, the test chip was not conceived, reduced to practice, or otherwise developed by the 523 patent’s inventors, so necessarily it was reduced to practice “by another.” *See* CIB at 83 (citing *Fox Group*, 700 F.3d at 1304).

So the test chip was reduced to practice prior to March 9, 2006. Tela advances two arguments as to why this does not establish the Intel 45nm Products as prior art. First, Tela argues

[REDACTED]

that the test chip was intentionally abandoned, suppressed, or concealed. *See* CIB at 85; CRB at 52. Inasmuch as the test chip materially differs from the Penryn chip, the evidence supports this argument, because, among other factors, the test chip itself was never commercialized and only some of its “hundreds of [design] rules” have been publicly disclosed. *See* CX-1219C at 261-263. But Respondents contend that the test chip and the Penryn chip, which was commercialized, were part of the same research and development program—the test chip was, in essence, a “prototype” that was “refined, perfected, and improved . . . for commercial release” as the Penryn chip. RIB at 84; *see* RX-0007C at Q/A 220.

Other than a conclusory, nonspecific comment by Dr. Hook, Tela points to no evidence to counter this contention. *See* CX-1231C at Q/A 1481 (“the M1 structures differ between the 45nm SRAM test chip and the Penryn”). Respondents’ evidence supports it, however. *See* RX-0001C at Q/A 37 (“The test chip was designed using the same design rules that we developed for the commercial products.”); RX-0007C at Q/A 288 (Dr. Subramanian explains that his claim-by-claim analysis relies on layout files from both the test chip and the Penryn chip). Dr. Auth testified that it took approximately 1,000 Intel engineers about two years of full-time work “for the main part of the project” of developing the Intel 45nm Products, so the delay here between actual reduction to practice and commercialization would be expected. RX-0001C at Q/A 30; *see id.* at Q/A 40 (“Penryn processors . . . are manufactured on Intel’s 45nm process technology”). Even Dr. Hook, who opined that the Intel 45nm Products had not been adequately publicly disclosed, generally treated the test chip and the Penryn chip as one product for purposes of his opinion. *Compare* CX-1231C at Q/A 1217 (“there a lot of design rules” that were not discussed in a 2007 publication by an Intel engineer) *with* Q/A 1204 (Respondents “rel[y] on certain 45nm products using Intel’s Penryn architecture,” and Dr. Hook “refer[s] to these as ‘Intel 45nm products’”).

[REDACTED]

Therefore, the evidence shows that the Penryn chip was the commercial embodiment of the test chip, rather than an entirely different invention, and that the 21-month period between actual reduction to practice and public disclosure through commercialization resulted from continuing research and development efforts, rather than intentional suppression and concealment. In response, Tela presents its second argument for abandonment, suppression, or concealment: that there was no enabling public disclosure. *See* CIB at 83-88. This argument differs from the one advanced regarding the 334 patent, because the 334 patent covers product claims and the 523 patent allegedly covers product-by-process claims. *See* CIB at 144 n.12. And because prior art status for product-by-process claims requires an enabling public disclosure, the argument goes, mere commercialization, without an otherwise enabling disclosure, is insufficient to establish prior art status. *See id.* at 144-45.

As a threshold matter of claim construction, all asserted claims depend from claim 1, which claims a “semiconductor chip” comprising various structures “formed” under certain conditions. *E.g.*, 523 patent at 24:51 (“gate electrode features formed within a region”). Respondents and the Staff seemingly agree that such language articulates a product-by-process claim, and so do I. *See* RIB at 85; SIB at 104. In view of this construction, Tela asserts that “Federal Circuit case law holds that the public disclosure necessary for prior art status to product-by-process claims under § 102(g) must be enabling.” CIB at 144. Tela candidly admits, however, that the “case law” to which it refers is a dissenting opinion in *Fox Group*. *See id.* at 144 n.12. In fact, actual Federal Circuit case law supports Respondents’ position: “a product-by-process claim can be anticipated by a prior art product that does not adhere to the claim’s process limitation,” because “an old product is not patentable even if it is made by a new process.” *Amgen Inc. v. F. Hoffman-La Roche Ltd*, 580 F.3d 1340, 1370 (Fed. Cir. 2009). And as noted above with respect to the product

[REDACTED]

claims of the 334 patent, commercialization of an allegedly prior art product is a “way to prove public disclosure” under Section 102(g), even when that commercialization by itself is non-enabling. *Fox Group*, 700 F.3d at 1306-07.

Therefore, the Intel 45nm Products, and the Penryn chip in particular, are prior art to the 523 patent.

As to the specifics of Respondents’ obviousness theory, Respondents argue the obviousness of the 523 patent in view of two combinations of prior art: Kitabayashi/Intel 45 nm Products and Kitabayashi/Intel 45 nm Products/Maziasz and Hayes. *See* RIB at 149. As with the 334 patent, the combination of Kitabayashi and the Intel 45 nm Products comes close to an embodiment of claim 1 of the 523 patent. Claim 1 covers a semiconductor chip possessing, among other elements, rectangular “gate electrode features” oriented in the y-direction and having a particular pitch, rectangular “gate contact structures” oriented in the x-direction, “at least one diffusion contact structure” positioned on a diffusion contact grid having a spacing equal to the gate pitch, and rectangular “first-metal structures” oriented in the x-direction, all forming multiple transistors. *See generally* 523 patent at 24:50-26:4. Most of these elements and the other elements of claim 1 are found in the Intel 45 nm Products, as Dr. Subramanian opines. *E.g.*, RX-0007C at Q/A 612-13. One of his demonstrative exhibits, for instance, identifies gate electrode features (green), gate contact structures (dark blue), and diffusion contact structures (pink) in the test chip. *See* RDX-0009C at *169. In particular, and contrary to Tela’s contention, Dr. Subramanian identifies multiple regions, generally by reference to cells shown in Intel 45 nm Product layout files, that contain structures that form various logic circuits, including a multiplexer, an inverting multiplexer, and a latch. *See* RX-0007C at Q/A 629-632; RIB at 149 n.42 (“the ‘region’ is the entire cell”); *cf.* CIB at 147 (arguing that Respondents “present[] no evidence” of a region of the

[REDACTED]

semiconductor chip containing features that form a logic circuit). And Kitabayashi discloses rectangular first-metal structures all oriented in the same direction, with “grids” of multiple metal layers, each oriented orthogonally to its vertical neighbors. *See* JX-0267 at 5:46-58, Fig. 9.

Thus, all the elements of claim 1 are seemingly disclosed in the prior art, with two exceptions. The first is, as Tela notes, orienting the gate electrode features and first-metal structures perpendicularly as in the 334 patent.⁹ *See* CIB at 146. Respondents allege that this element would be obvious to a skilled artisan on the same grounds presented before. *See* RIB at 149 (citing RX-0007C at Q/A 537-552 (discussing Intel 45nm Products), 152-153 (citing RX-0007C at Q/A 606-610 (discussing Kitabayashi)). Dr. Subramanian similarly does not expand on the purported motivation to include this arrangement in the prior art combination. RX-0007C at Q/A 610 (“As I discussed earlier, in the combination of Kitabayashi and Intel’s 45nm Products, it would have been obvious to run the wires in M1 to be perpendicular to the direction that poly runs.”). Accordingly, for the same substantive reasons discussed above, Respondents have not clearly and convincingly shown this limitation would be present in the Kitabayashi and Intel 45nm Product combination.

The second exception is the “diffusion region.” Respondents contend that this element is found in the Intel 45nm Products, to the extent “any source or drain is a ‘diffusion region’” under Tela’s infringement theory. RIB at 154 (citing RX-0007C at Q/A 639-642)). But the sources and drains in the Intel 45nm Products are [REDACTED] and do not literally satisfy the “diffusion

⁹ Not all relevant claim terms were construed during the *Markman* proceeding, including, as one example, “grid,” to the extent it means something beyond “projected gridlines” used during a stage of chip manufacturing, and “diffusion contact structure.” Order No. 34 at 59. But Tela does not separately dispute that the various components in the prior art fall within the scope of the unconstrued claim terms, so there is no need to separately construe them. *See Vanderlande Indus. Nederland BV v. Int’l Trade Comm’n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004).

[REDACTED]

region” limitation, as explained above. *See* RX-0007C at Q/A 641. This is the only argument Respondents present regarding this limitation. *See* RIB at 154; RRB at 83-85. Although diffusion regions like those disclosed in the 523 patent are likely readily found in the prior art, Respondents make no effort to demonstrate that it would have been obvious to a skilled artisan to, say, substitute such diffusion regions for the [REDACTED] sources and drains found in the Intel 45 nm Products, or otherwise demonstrate obviousness beyond generally alluding to “Tela’s infringement theory.” RIB at 154. Respondents’ evidence regarding this limitation is not clear and convincing, and accordingly, this limitation is also missing from the prior art relied upon.

Beyond these missing claim elements, Respondents have not presented a clear and convincing case of obviousness in a procedural sense, either. Tela is correct that much of Respondents’ detailed discussion for this patent appears in footnotes. *See* CRB at 73 n.17. Indeed, some of Respondents’ most significant points appear in footnotes. *E.g.*, RIB at 152 n.44 (disputing Dr. Hook’s opinion regarding motivation to combine); RIB at 153 n.48 (arguing that a skilled artisan would have known that “metal 1 can be run orthogonal to poly”). Although Ground Rule 13.1 contemplates the use of footnotes (because it holds that footnotes need not be double spaced), it also states that a “reasonable page limit will be imposed,” with that limit determined on a “case-by-case basis.” Order No. 2, Attachment A. The limit here was 200 pages for the opening brief, as announced in open court at the end of the evidentiary hearing. *See* Hr’g Tr. at 1286:18-19. The large amount of text, the pointedness of the arguments, and the volume of the evidence cited in the relevant footnotes of Respondents’ opening brief may not violate the letter of Ground 13.1, but they plainly violate the spirit, to Tela’s prejudice. *See id.* at 1288:12-18 (“I urge both sides, be judicious about what you put in your post-hearing briefs”). So although the pertinent footnotes

[REDACTED]

have not been “disregarded,” as Tela requests, they have generally been accorded less weight than the main text. CRB at 73 n.17.

Accordingly, Respondents have not carried their burden of proving that claim 1 is invalid as obvious, nor have they proven that the claims depending from it are invalid as obvious. *Ortho-McNeil*, 520 F.3d at 1365.

VI. DOMESTIC INDUSTRY - ECONOMIC PRONG

In a patent-based complaint, a violation of Section 337 can be found “only if an industry in the United States, relating to the articles protected by the patent ... concerned, exists or is in the process of being established.” 19 U.S.C. § 1337(a)(2). Under Commission precedent, this “domestic industry requirement” of Section 337 consists of an economic prong and a technical prong. *Stringed Instruments*, Inv. No. 337-TA-586, Comm’n Op. at 12-14. The complainant bears the burden of establishing that the domestic industry requirement is satisfied. *See Certain Set-Top Boxes and Components Thereof*, Inv. No. 337-TA-454, Initial Determination at 294 (June 21, 2002) (not reviewed in relevant part).

The economic prong of the domestic industry requirement is defined in subsection (a)(3) of Section 337 as follows:

(3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark or mask work concerned --

(A) Significant investment in plant and equipment;

(B) Significant employment of labor or capital; or

(C) Substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3). The economic prong of the domestic industry requirement is satisfied by meeting the criteria of any one of the three factors listed above. Importantly, the Commission has

[REDACTED]

clarified that investments in plant and equipment, labor, and capital that may fairly be considered investments in research and development are eligible for consideration under subsections (A) and (B), in addition to subsection (C). *See Solid State Storage Drives*, Comm’n Op. at 14.

Tela contends the economic prong is met under subsections (A) and (B) through the domestic activities of its licensee SAS. In its opening brief, Tela explains it owns the Asserted Patents and entered into a license with Samsung Electronics Co., Ltd. (“Samsung”) in 2016 which permitted Samsung and its affiliates, such as SAS, to practice the Asserted Patents. CIB at 155-156 (citing JX-0008; JX-0010; CX-1148C at Q/A 6-21; JX-0170C). No party disputes this ownership or the status of SAS as a licensee. *See generally* RIB; RRB; SIB; SRB.

As determined above, Tela has not shown the technical prong of domestic industry is met. Nevertheless, to aid the Commission’s analysis, Tela’s claims of economic prong domestic industry are evaluated below; and for the reasons provided, Tela has not shown “significant” investment in satisfaction of the statute under either subsection (A) or (B). 19 U.S.C. § 1337 (a)(3)(A), (B).

A. Qualifying Expenditures

As noted above in the discussion of procedural history, and prior to the evidentiary hearing, Tela filed a motion for summary determination that it satisfied the economic prong of domestic industry. That motion was granted-in-part with Order No. 38, which, while not finding the matter conclusively established, did establish the qualifying expenditures from Tela’s licensee, SAS, which manufactures the DI Products within the United States. Those expenditures, repeated in Tela’s post-hearing briefing with small changes to Group 3 amounts (*see* CIB at 161 n.17), are as follows:



Subsection (A), "Plant and Equipment"		
	Allocated Depreciation	Allocated Square Footage
Group 1		
Group 2		
Group 3		
Subsection (B), "Labor and Capital"		
	Allocated Salary ¹⁶ + Production Expenses	
Group 1		
Group 2		
Group 3		

(*id.* at 160-161; *see* Order No. 38 at 13). For ease of reference, and as mentioned above, the groups 1-3 refer to the following overlapping sets of products:

Tela's Economic Prong Groups	
Group 1	(7420)
Group 2	Group 1 +
Group 3	Group 1 + Group 2 +

CIB at 160; *see* RIB at 172-173. Accordingly, Tela contends "[i]n light of these findings, the only remaining issue for the ALJ to decide is whether these allocated investments are significant." *Id.* at 154. The Staff's discussion of economic prong reflects the same position. *See* SIB at 116-122.

Respondents and the Staff, on the other hand, do not immediately abandon a contest over Tela's claimed investment amounts. Rather they argue that SAS effectively last produced Group 1 wafers in July 2018 (*see* RIB at 173-174; SIB at 117) and Group 2 wafers in December 2018

[REDACTED]

(see RIB at 174; SIB at 118), meaning that there was no investment in those products at the time of Tela's original complaint (December 2018) or amended complaint (February 2019) (see RIB at 174-175; SIB at 118).

Respondents reason that if this initial determination finds that Group 2 or Group 3 have not been shown to practice the Asserted Patents (as the contrary had been assumed in Order No. 38), that must mean there are no current "qualifying activities" to enable consideration of any "past" Group 1 investment, regardless of whether Group 1 satisfies the technical prong:

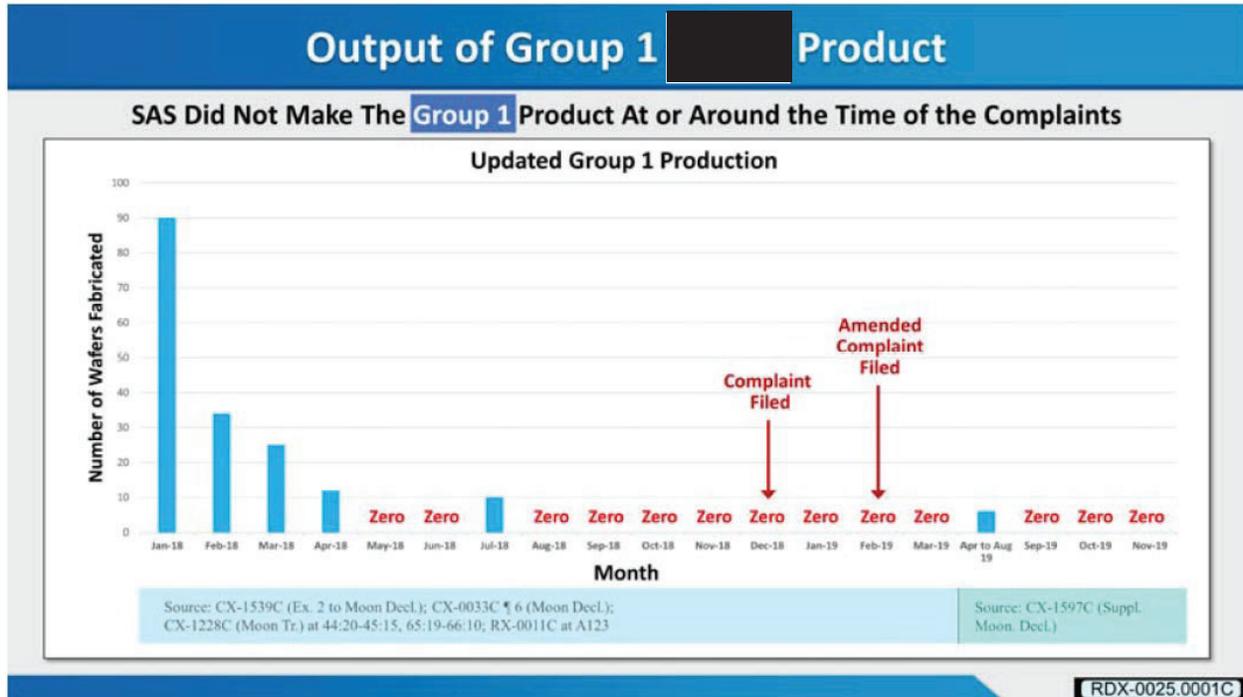
As Order No. 38 recognized, past expenditures could be considered, "so long as those investments pertain to the complainant's industry with respect to articles protected by the asserted IP rights *and the complainant is continuing to make qualifying investments at the time the complaint is filed.*" Order No. 38 at 6-7 (quotes and citation omitted) (emphasis added). While the ALJ noted that "qualifying investments continue to be made for the Group 3 products" (*id.* at 7), products can form the basis of a "qualifying" activity only if they practice the asserted patents. *See Certain Television Sets, Television Receivers, Television Tuners, and Components Thereof*, Inv. No. 337-TA-910, 2015 WL 6755093, Comm'n Op., at *39; *Certain Subsea Telecommunications Sys. and Components Thereof*, Inv. No. 337-TA-1098, Initial Determination at 70 (U.S.I.T.C. Apr. 26, 2019) (qualifying activity must be tied to patent-practicing article). With respect to Group 3, because Tela has not provided any evidence that the unique (non-Exynos 7420) products in Group 3 practice the Asserted Patents, any continuing activities for those products are irrelevant, and SAS's cessation of activities for the Group 1 and 2 products should end the domestic industry inquiry.

Id. at 175; see RRB at 89.

As determined above, Tela has indeed failed to show practice of the Asserted Patents by the Exynos 7420 on the merits, and by the other DI Products through assertions of representativeness. In this way, domestic industry cannot be found. Assuming nonetheless that the Exynos 7420 does practice a claim of an Asserted Patent, Respondents' argument regarding continuing qualifying activities should be addressed.



Respondents’ argument is not persuasive. As shown in their demonstrative below, the Group 1 products had been produced within one year of either Tela’s original or amended complaints:



RIB at 174; RDX-0025C at *1; see CIB at 164 (noting “171 [redacted] wafers represent thousands of Exynos 7420 processors”). Also as shown, an amount of Exynos 7420 products were produced after the filing of the complaint, between April and August 2019. See CRB at 81 (citing CX-1597C). Considering the technology involved and required preparation for manufacture, the Exynos 7420 cannot be deemed a “discontinued” product. Respondents would have me ignore this 2019 production entirely and reach the opposite conclusion under *Certain Thermoplastic-Encapsulated Electric Motors, Components Thereof, and Products and Vehicles Containing Same II*, Inv. No. 337-TA-1073 (see RIB at 176), but that investigation concerned whether post-complaint expenditures could be considered in assessing “significant” investment. Comm’n Op. at 6-8 (Aug. 12, 2019). Here, the post-complaint activity is only considered to show the product

[REDACTED]

is not discontinued, and it is not incorporated into the investment amounts determined in Order No. 38 and evaluated below. *See, e.g., Certain Magnetic Data Storage Tapes and Cartridges Containing the Same*, Inv. No. 337-TA-1012, Comm’n Op. at 112-113 (Apr. 2, 2018) (“*Magnetic Data Storage*”).

Moreover, because the Exynos 7420 was not discontinued at the time of Tela’s complaint, it is not reasonable to compare SAS to the complainant in *Certain Television Sets*, that had shifted its business model and ceased all of its qualifying domestic activity six months before filing its complaint. Inv. No. 337-TA-910, Comm’n Op. at 59 (Oct. 30, 2015). As the Commission in that investigation explained, “[w]hat is at issue in this investigation is not merely a decline in an ailing business or discontinued products, but the lack of evidence that a cognizable domestic industry exists at the time the complaint was filed. . . . Its U.S. business shifted toward patent monetization and away from any research and development, or engineering related to its tuner products.” *Id.* at 74. By contrast, the record here shows that SAS’s plant, equipment, labor and capital which created the Exynos 7420 products continued to function through the date of the complaint. To the extent Respondents and Staff argue for a rule that eliminates consideration of any investment older than six months when there is no investment during the same month, week, or day as the filing of the complaint (*see* RRB at 89 (“Because SAS did not produce any Group 1 wafers at the time of Tela’s complaint, no domestic industry in those products existed, and the inquiry should end there. *See* [*Certain Television Sets*].”); SIB at 118), such a rule is not supported by the cited precedent (*see* RIB at 175; RRB at 89; SIB at 118).

Accordingly, the investment amounts listed for the Group 1 products in Order No. 38, and fairly adjusted by Tela without meaningful dispute (*see* RRB at 88; SRB at 46), are analyzed for significance.

[REDACTED]

B. “Significant” or “Substantial”

The next step in the evaluation of domestic industry is to determine if the investment amounts identified above are “significant,” as in subsections (A) and (B). The most recent precedential decision by the Court of Appeals for the Federal Circuit addressing this determination is *Lelo*, which restated law applicable to a number of issues surrounding the economic prong of domestic industry. *See* 786 F.3d at 883-85. In particular, the Federal Circuit held that the statutory terms “‘significant’ and ‘substantial’ refer to an increase in quantity, or to a benchmark in numbers” and “[a]n ‘investment in plant and equipment’ therefore is characterized quantitatively, *i.e.*, by the amount of money invested in the plant and equipment.” *Id.* at 883. Continuing, the Federal Circuit held “[a]ll of the foregoing requires a quantitative analysis in order to determine whether there is a ‘significant’ increase or attribution by virtue of the claimant’s asserted commercial activity in the United States.” *Id.* In short, “[q]ualitative factors cannot compensate for quantitative data that indicate insignificant investment and employment.” *Id.* at 885. The Commission has since made clear that some sort of comparative analysis must be made before significant or substantial can be found. *See, e.g., Certain Gas Spring Nailer Products and Components Thereof*, Inv. No. 337-TA-1082, Notice of Comm’n Determination at 3 (Dec. 12, 2019) (“*Gas Spring Nailers*”); *Certain Carburetors and Products Containing Such Carburetors*, Inv. No. 337-TA-1123, Comm’n Op. at 17-19 (Oct. 28, 2019) (“*Carburetors*”).

As to the Group 1, [REDACTED] (Exynos 7420) product, Tela points to a number of considerations: the asserted domestic activity is the actual manufacture of the “billions of transistors and other components that enable the logic functions,” which is qualitatively significant (*see* CIB at 166); that manufacture, regardless of the number of wafers made, requires enormous up-front investment in space and equipment (*see id.* at 167; *id.* at 167 n.20 (citing *Magnetic Data*

[REDACTED]

Storage, Inv. No. 337-TA-1012, Comm’n Op. at 115)); that manufacture, considered “front-end” processing, is generally quantitatively significant compared to the overseas, “back-end” processing (*see id.* at 167-170); the claimed labor and depreciation investment is quantitatively significant compared to the cost of the raw materials used by SAS in manufacturing, in a value-added context (*see id.* at 170-171); the value of the sold wafer as compared to raw material cost is quantitatively significant (*see id.* at 171-172); the scope of the Asserted Patents’ claims—that is, the physical implementation of integrated circuit designs—is commensurate with the scope of the work performed by SAS (*see id.* at 172-173); SAS is a quantitatively significant investor in U.S. semiconductor fabrication as compared to the rest of the industry (*see id.* at 173-174); and the claimed investment is quantitatively significant as compared to SAS’s revenue per sold wafer (*see id.* at 175-176).

In its reply brief, Tela contends “[a]t base, Respondents and Staff’s only argument is that SAS’s allocated investments in Groups 1 and 2 are too small.” CRB at 82. This is in error, Tela argues, because the Commission has made clear there is no minimum monetary expenditure to satisfy the domestic industry requirement. *See id.* at 82-83 (citing *Stringed Instruments*, Inv. No. 337-TA-586, Comm’n Op. at 25-26; *Carburetors*, Inv. No. 337-TA-1123, Comm’n Op. at 27). Tela further observes that the parties’ positions on the Group 3 products reveals their application of a minimum investment:

That Respondents and Staff contest the significance of the investments in Groups 1 and 2 – but not Group 3 – demonstrates that they are applying a minimum threshold. The fabrication activities and related expenses are relatively the same for all of the Exynos Products, as indicated by the fact that SAS tracks its costs per wafer at the node level (*e.g.*, 14nm) and not by individual products. (CX-1145C (Greene) at Q/A 171-175 (showing that on average it costs SAS [REDACTED] to fabricate any 14nm wafer).) Thus, the fabrication activities and the per-wafer costs between the three groups, all of which are 14nm Exynos mobile processors, are relatively the same. Group 3, however, contains more models and therefore the absolute value

[REDACTED]

of the allocated Group 3 investments is larger than those of Groups 1 and 2 because the same activities are applied across a greater volume of wafers. A finding that only Group 3 is significant necessarily means that a minimum threshold was applied, because significance only existed once the same activities and costs were multiplied by a sufficient volume of wafers for the aggregate allocated amount to cross some unspecified – and improper – significance threshold.

Id. at 83-84. Tela reemphasizes its views that “domestic industry analysis is not whether the investments are large or small in the absolute sense, but whether they are important to the articles, which is the analysis Mr. Greene performed and Respondents and Staff ignore” (*id.* at 84 (citing Hr’g Tr. at 537:11-16, 543:11-16)), and the massive production of products by SAS other than the Exynos 7420 in 2018 is simply “not pertinent to the analysis” (*id.* at 85). Tela explains:

More importantly, the production volume percentages were just used to quantitatively allocate SAS’s investments. (Tr. (Greene) at 511:24-512:4; 536:21-537:6.) Whether those investments are significant is a separate, multi-faceted inquiry. If an allocation percentage was the measure of significance, there would be no need perform any of the additional evaluations the Commission regularly employs to put the relative value of investments in context. *See Certain Collapsible Sockets for Mobile Electronic Devices and Components Thereof*, Inv. No. 337-TA-1056, Comm’n Op. at 20 n.13 (July 9, 2018) (significance cannot be determined on the sales-based allocation percentage itself); *Carburetors*, Comm’n Op. at 17-18; (Tr. (Greene) at 537:7-10). Respondents argue that Mr. Greene’s statement that production of a single wafer could be significant is absurd. (RIB at 173, 179.) Respondents cite no authority. Considering the Commission evaluates significance of the investment and activities to the articles, placed in the proper context – for example, that production of even a single wafer requires millions of dollars of equipment and facility space, and requires skilled technicians, and results in hundreds of valuable processors – production of a single wafer very well could be significant. (Tr. (Greene) at 543:24-545:8.) Regardless, Tela is not relying on a single wafer so the testimony is irrelevant.

Id.

Respondents oppose a finding of significance. Respondents highlight that the Group 1 product, the Exynos 7420, indisputably made up just 0.02% of all wafers fabricated by SAS in 2018 and argue this cannot be “significant.” RIB at 176 (citing CDX-0014C at *18). Respondents

[REDACTED]

criticize Tela for failing to take into account this minimal volume of wafers produced, and characterize the claim of Tela’s expert, Mr. Greene, that “production of just *one* wafer would qualify as ‘significant,’” as “self-evidently absurd.” *See id.* at 179 (citing Hr’g Tr. at 511:7-12, 535:8-16, 536:10-14). Respondents take the position that it is improper to ignore SAS’s production of other, non-DI Products, because “a domestic industry must be ‘made in the context of the complainant’s size.’” *Id.* at 181 (citing *Certain Kinesiotherapy Devices and Components Thereof*, Inv. No. 337-TA-823, Comm’n Op. at 33 (July 12, 2013), *rev’d on other grounds*, *Lelo*, 786 F.3d 879); RRB at 89-92 (citing, *inter alia*, *Carburetors*, Inv. No. 337-TA-1123, Comm’n Op at 17). As to Tela’s quantitative analysis, Respondents argue there is no evidence on “the processors’ R&D, design, assembly, testing, and packaging—none of which is carried out domestically by SAS, yet all of which contributes to the total cost of producing the processors (with the relevant data presumably being available to Tela from its licensee)” (RRB at 92 (citing Hr’g Tr. at 509:11-510:2, 522:16-525:25)), Tela’s use of Intel data as a proxy suffers from the same problem, and there is no evidence to believe the analogy to Intel is appropriate (*see id.* at 92-93 (citing Hr’g Tr. at 533:9-534:24)).

The Staff agrees with each of Respondents’ points for the Group 1 product. *See* SIB at 117-120. In particular, the Staff notes the labor associated with Group 1 is one half of one employee (*see* SIB at 119 (citing RX-0011C at Q/A 140; Order No. 38 at 8)) and actual profits to SAS from the sale of wafers to Samsung are only [REDACTED] (SRB at 47 (citing CPB at 170-173)). The Staff summarizes: “[a]ll of these numbers are quantitatively small, particularly for large companies like SAS and Samsung” SRB at 47.

The domestic industry investments are not significant. Even accepting Tela’s principal quantitative metric (*i.e.*, SAS’s investments add 100% of the value to the product), [REDACTED]

[REDACTED]

[REDACTED] amounts are not significant. *See* CRB at 82-84. While it is true the Commission made clear in *Stringed Instruments* that “there is no minimum monetary expenditure that a complainant must demonstrate to qualify as a domestic industry” (Inv. No. 337-TA-586, Comm’n Op. at 25), it also explained “[w]e agree with the parties that the requirement for showing the existence of a domestic industry will depend on the industry in question, and the complainant’s relative size” (*id.* at 25-26). In that investigation, for example, a “substantial” or “significant” investment did not exist with investment of \$8500 representing, impliedly, a 100% domestic value-add. *See id.* at 26-27.

Tela does little to explain why [REDACTED] invested in plant and equipment and [REDACTED] in labor is not too small. Indeed, in a section entitled “The Semiconductor Fabrication Industry and Marketplace,” Tela touts the domestic presence and spending of SAS as a whole, and not the [REDACTED] figures at issue. *See* CIB at 173-174; *see also* CRB at 88-89. Tela also emphasizes the limited number of industry actors (CIB at 173 (“[O]nly a handful of companies are able to operate 300mm wafer fabrication facilities in the U.S.”)), the millions of dollars required in equipment and facilities required to start up semiconductor process fabrication (*id.* at 167 “These machines can cost up to \$100 million apiece.”), and SAS’s relative size (*id.* at 173 (“After Intel, SAS is the largest major 14nm supplier in the U.S.”); *id.* at 174 (“[W]hile SAS is comparable to GlobalFoundries in terms of facility size and employee headcount, SAS invested [REDACTED] in U.S. salaries and produced [REDACTED] 14nm wafers in 2018.”).

This approach avoids the crucial question, which is whether [REDACTED] in plant and equipment and [REDACTED] in labor can be considered “significant” in the contexts of the marketplace and SAS itself. In fact, Tela’s approach only serves to emphasize the modesty of these amounts. And that modesty is consistent with the fact that the Exynos 7420 is the processor for the Galaxy

[REDACTED]

S6, Samsung’s flagship smartphone back in 2015—a phone which has since been replaced by newer generations both in the marketplace and in SAS’s production facilities—so domestic industry investment can be expected to be even more modest in the future. *See* CIB at 159-160 (showing investment levels across LPE, LPP, and LPC), 164 (describing Galaxy S6); CX-0629; CX-1230; CX-0632; CX-0631; CX-0630; CX-0633. The Federal Circuit and the Commission have associated modesty with insignificance, an appropriate association here as well. *Lelo*, 786 F.3d at 885 (“The Commission determined that Standard Innovation’s investment and employment under prongs (A) and (B) were quantitatively ‘modest,’ Comm’n Op. at 34, which we take to mean ‘insignificant.’ . . . We agree with the Commission’s finding that investment and employment under prongs (A) and (B) were modest and insignificant.”); *Certain Thermoplastic-Encapsulated Electric Motors, Components Thereof, and Products and Vehicles Containing Same II*, Inv. No. 337-TA-1073, Comm’n Op. at 14 (Aug. 12, 2019) (“IV’s investments are too modest to meet the domestic industry requirement of section 337(a)(3)”) (“*Electric Motors*”); *Electric Motors*, Inv. No. 337-TA-1073, Comm’n Op. at 17 (“IV has failed to show how these expenditures are significant in any appropriate context, particularly in light of the alleged difficulty of making these pumps.”). That there was a large up-front investment years ago changes nothing, because the domestic industry presently devoted to the Exynos 7420 is virtually defunct, and even massive investments cannot be allocated to domestic industry if they possess no nexus to a domestic industry product. *See, e.g. Certain Subsea Telecommunication Systems and Components Thereof*, Inv. No. 337-TA-1098, Comm’n Op. at 41 (Oct. 21, 2019) (“The Commission has found that complainants have not satisfied the domestic industry requirement where the complainant failed to allocate expenses to account for non-domestic industry products that do not practice the patent.”).

[REDACTED]

In sum, SAS’s commitment to producing semiconductors in the United States even though “global capacity for fabrication has generally shifted to Asia” (CIB at 174) is commendable. The record does not show, however, that the Exynos 7420 is a significant part of SAS’s plan; nor does it show SAS’s investment of [REDACTED] in plant and equipment and [REDACTED] in labor can be considered “significant” under the statute. Accordingly, Tela has not met the economic prong of the domestic industry requirement even assuming the Exynos 7420 is found to practice a claim of the Asserted Patents.

VII. CONCLUSIONS OF LAW

1. The Commission has *in rem* jurisdiction over the accused products, integrated circuits and products containing same.
2. The importation or sale requirement of Section 337 is satisfied for all respondents.
3. Tela, through its licensee, has not been shown to practice any claims of U.S. Patent No. 10,141,334.
4. The domestic industry requirement is not satisfied with respect to the 334 patent.
5. Tela, through its licensee, has not been shown to practice any claims of U.S. Patent No. 10,186,523.
6. The domestic industry requirement is not satisfied with respect to the 523 patent.
7. Respondents directly infringe claims 1, 2, and 5 of the 334 patent.
8. Respondents directly infringe claims 1-11, 14-20, 25, and 26 of the 523 patent.
9. Claims 1, 2, and 5 of the 334 patent have been shown to be invalid under 35 U.S.C. § 102. No claims of the 334 patent have been shown to be invalid under 35 U.S.C. § 103.
10. Claims 1, 2, 5, and 15 of the 334 patent have been shown to be invalid under 35 U.S.C. § 112.
11. No claims of the 523 patent have been shown to be invalid under 35 U.S.C. § 103.
12. No claims of the 523 patent have been shown to be invalid under 35 U.S.C. § 112.
13. Tela is not contractually barred from enforcing the 334 patent against respondent Intel or its customers.



14. There is no violation of Section 337 with respect to the 334 patent.
15. There is no violation of Section 337 with respect to the 523 patent.

VIII. RECOMMENDED DETERMINATION ON REMEDY AND BOND

The Commission's Rules provide that subsequent to an initial determination on the question of violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, the administrative law judge shall issue a recommended determination concerning the appropriate remedy in the event that the Commission finds a violation of section 337, and the amount of bond to be posted by respondent during Presidential review of the Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(1)(ii).

The Commission has broad discretion in selecting the form, scope, and extent of the remedy in a section 337 proceeding. *Viscofan, S.A. v. Int'l Trade Comm'n*, 787 F.2d 544, 548 (Fed. Cir. 1986). Under Section 337(d)(1), if the Commission determines as a result of an investigation that there is a violation of section 337, the Commission is authorized to enter either a limited or a general exclusion order. 19 U.S.C. § 1337(d)(1). A limited exclusion order instructs the U.S. Customs and Border Protection ("CBP") to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the CBP to exclude from entry all articles that are covered by the patent at issue, without regard to source. *Certain Purple Protective Gloves*, Inv. No. 337-TA-500, Comm'n Op. at 5 (Dec. 22, 2004). Under section 337(f)(1), the Commission may issue a cease and desist order in addition to, or instead of, an exclusion order. 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold, thereby undercutting the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof*

[REDACTED]

and Prods. Containing Same, Including Air Conditioners for Automobiles, Inv. No. 337-TA-334 (Remand), Comm’n Op. at 26-28 (Sept. 10, 1997).

Additionally, during the 60-day period of Presidential review under 19 U.S.C. § 1337(j), “articles directed to be excluded from entry under subsection (d) . . . shall . . . be entitled to entry under bond prescribed by the Secretary in an amount determined by the Commission to be sufficient to protect the complainant from any injury.” *See* 19 U.S.C. § 1337(j)(3). “The Commission typically sets the bond based on the price differential between the imported infringing product and the domestic industry article or based on a reasonable royalty. However, where the available pricing or royalty information is inadequate, the bond may be set at one hundred (100) percent of the entered value of the infringing product.” *Certain Industrial Automation Systems and Components Thereof Including Control Systems, Controllers, Visualization Hardware, Motion and Motor Control Systems, Networking Equipment, Safety Devices, and Power Supplies*, Inv. No. 337-TA-1074, Comm’n Op. at 13 (Apr. 23, 2019) (“*Automation Systems*”) (public version) (citation omitted).

A. Limited Exclusion Order

Should a violation be found, Tela argues “the Commission’s usual practice is to issue relief extending to the boundaries of the Notice of Investigation to exclude any infringing products.” CIB at 190 (citing *Certain Erasable Programmable Read Only Memories, Components Thereof, Prods. Containing Such Memories, and Processes for Making Such Memories*, Inv. No. 337-TA-276, Comm’n Op. at 9-11 (Aug. 1, 1991)). Thus, Tela contends a limited exclusion order should issue against all of Respondents’ infringing products. *Id.* In relevant part, Tela opposes any certification provisions because Respondents’ mentions of new processor products “are Intel 14nm or smaller Tri-Gate integrated circuits . . . within the scope of the NOI and subject to exclusion.”

[REDACTED]

CRB at 100. Tela suggests that Respondents should leverage the advisory opinion process for any future products, and that they have not shown the need for warranty or repair exemptions. *See id.* In its public interest discussion, Tela argues any delay on a remedy is not warranted, but if implemented should be limited to six months—the same time Intel claimed in interrogatory responses that it could design around the Asserted Patents. CRB at 95-96 (citing CX-0007C at *1150; CX-1235C at Q/A 216-218, 221).

Respondents do not challenge that a limited exclusion should issue, but argue public interest considerations warrant several adjustments, including: a delay of at least twelve months, the order should not extend to Respondents’ downstream products, and applicability only to products for which respondent Intel is the importer of record. RIB at 196-197; *see* RRB at 100.

As to the delay, Respondents claim it would take [REDACTED]

[REDACTED] RIB at 196-197 (citing CX-1220C at 253:12-19; CX-1223C at 137:17-138:6; RX-0002C at Q/A 165-169).

Respondents also contend it serves “to allow Respondents and other impacted companies time to begin implementing substitute processors and/or moving manufacturing overseas.” RIB at 196; RRB at 100. Additionally, Respondents argue the remedy should allow for: certification provisions, Government exemptions under 19 U.S.C. § 1337(l), and service and repair exemptions. *See* RIB at 197.

The Staff emphasizes that “[t]he Commission has ‘broad discretion in selecting the form, scope and extent of the remedy.’” SIB at 123 (citing *Viscofan, S.A. v. Int’l Trade Comm’n*, 787 F.2d 544, 548 (Fed. Cir. 1986); *Fuji Photo Film v. Int’l Trade Comm’n*, 386 F.3d 1095, 1106-1107 (Fed. Cir. 2004)). The Staff does not support downstream product exemptions as described by Respondents (*id.* at 124), or service, repair, and replacement exceptions (*id.* at 124-125

[REDACTED]

(“Respondents also ask for a repair exemption, although they cite only scant evidence of repair and maintenance activities.”). The Staff does support including the Commission’s standard certification provision (*id.* at 125) and a delay to the effective date by several months to alleviate the impact on third parties (*id.* at 132). On this latter point, the Staff notes, as Tela did, that “Respondents admit that a design-around could be completed in as little as six months.” *Id.* (citing CX-0007C at *1150).

The record supports imposition of a limited exclusion order with a delay of 12 months and a standard certification provision. Respondents’ consideration of EPROMs factors and their requests for certification provisions and service and repair modifications are explained only through an incorporation by reference of their pre-hearing brief, which violates Ground Rule 13.5. *See* RIB at 197 (citing RPB at 393-396); Order No. 2; *see generally* RRB at 93-100. As such, these arguments are not considered. The government exemption under 19 U.S.C. § 1337(l) is included in exclusion orders as a matter of course and need not be discussed. As to service and repair exceptions, no other party supports them, and I do not recommend they be included in any exclusion orders.

As to a delay, should an exclusion order issue, Tela and the Staff largely draw upon Respondents’ contentions in this investigation for their six-month figure, but the contentions state a redesign would take *at least* 6 months. CX-0007C at *1150 (“Intel would likely need to change the early stages or lower level of the wafer fabrication process to avoid the adjudicated scope of Tela’s asserted patent claims. The lower level the modification, the longer the redesign will take, because a low level modification has ripple effects for all subsequent levels of the fabrication process. Thus, a redesign of Intel Accused Products would likely take at least 6 months to complete.”). It seems unlikely that designs could change, in ways acceptable to fabrication and

[REDACTED]

performance needs, in that timeframe. That six-month figure also does not appear to take into account the changes non-party customers would need to implement subsequent to the redesign, or the time needed to switch processor suppliers. Credible testimony on this point supports accommodating at least an additional six months. *See* CX-1220C at 253:12-257:7; CX-1223C at 137:14-139:9.

Finally, as to certification provisions, the Commission has instructed that “[c]ertification provisions aid U.S. Customs and Border Protection (‘CBP’) in enforcing Commission orders but ‘do not mandate that CBP accept certification as proof that the articles in question are not covered’ by the limited exclusion order.” *Certain Robotic Vacuum Cleaning Devices and Components Thereof Such as Spare Parts*, Inv. No. 337-TA-1057, Comm’n Op. at 55 (Feb. 1, 2019). Additionally, “[t]he standard provision does not allow an importer to simply certify that it is not violating the exclusion order. Rather, CBP only accepts a certification that the goods have been previously determined by CBP or the Commission not to violate the exclusion order” and “it has been Commission practice for the past several years to include certification provisions in its exclusion orders to aid CBP.” *See Road Milling Machines*, Inv. No. 337-TA-1067, Comm’n Op. at 15, 15 n. 5 (citations omitted). Respondents do not appear to argue for any non-standard certification provision, so it is my recommendation that any limited exclusion order include the Commission’s standard certification provision.

B. Cease and Desist Order

Should a violation be found, Tela argues cease and desist orders should issue because “[e]ach Respondent stipulated that it maintains a commercially significant inventory of Accused Products in the U.S.” CIB at 191 (citing JX-0017C; JX-0018C; JX-0019C; JX-0020C; JX-0021C; CX-1145C at Q/A 233-278). Tela specifies that the orders should preclude activities including

[REDACTED]

“(1) maintenance, warranty, and repair, (2) sale, including of any inventory, (3) sales and/or marketing, and (4) importation.” *Id.*

Respondents generally apply their argument on exemptions and limitations to an exclusion order to any issuing cease and desist orders. *See* RIB at 196-197; RRB at 100. The Staff supports cease and desist orders should a violation be found, again noting the stipulations entered into by each respondent. SIB at 126-127; SRB at 50. The Staff does, however, question how certain of Tela’s public interest propositions comport with a cease and desist order that prevents Intel from selling to third-parties for later importation. *See* SIB at 127; SRB art 49.

Complainants bear the burden on the issue of cease and desist orders. *Certain Microfluidic Devices*, Inv. No. 337-TA-1068, Comm’n Op. at 23 (Jan. 10, 2020). Such orders “are generally issued when, with respect to the imported infringing products, respondents maintain commercially significant inventories in the United States or have significant domestic operations that could undercut the remedy provided by an exclusion order.” *Id.* at 22-23 (citations omitted). Given the stipulations referenced above, this inventory requirement is met and it is my recommendation that cease and desist orders should issue against each respondent. It is also my recommendation that the cease and desist orders be delayed for twelve months in parallel with the exclusion orders.

C. Bond

The Commission has held that “[t]he complainant bears the burden of establishing the need for a bond” during the Presidential Review period. *See Robotic Vacuums*, Inv. No. 337-TA-1057, Comm’n Op. at 68. Tela does not seek a bond. *See* CIB at 190-191; RIB at 196 (citing CPB at 386); SIB at 128. Therefore, it is my recommendation that, in the event of a violation, no bond requirement should issue.

D. Public Interest

As determined above, there has been no violation of section 337. Assuming a violation is found, however, it is recommended that the remedial orders include: limited exclusion orders directed to each respondent, including certification provisions and a twelve-month enforcement delay; and cease-and-desist orders, also directed to each respondent and including twelve-month enforcement delays. The remaining issue for this recommended determination is to identify the effects which these orders would have upon the public interest and consider whether those effects are so prejudicial as to justify the denial of any remedy. The Commission has explained:

Section 337 requires the Commission, upon finding a violation of section 337, to issue an LEO “unless, after considering the effect of such exclusion upon the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers, it finds that such articles should not be excluded from entry.” 19 U.S.C. § 1337(d)(1). Similarly, the Commission must consider these public interest factors before issuing a CDO. 19 U.S.C. § 1337(f)(1).

Certain Electronic Nicotine Delivery Systems and Components Thereof, Inv. No. 337-TA-1139, Comm’n Op. at 16 (May 5, 2020). The Respondents contend public interest factors should preclude a remedy; the Staff does not. RIB at 183; *see* SIB at 132; CIB at 177-178. For the reasons discussed below, it is not my recommendation that public interest considerations should preclude the issuance of the recommended remedy.

1. Public Health and Welfare

As to public health and welfare, the record does not weigh one way or the other. Respondents argue the orders would “exclude Intel microprocessors that supply over 95% of the U.S. server market segment and large percentages of the U.S. workstation, supercomputer, and personal computer market segments” leading to reduced output and employment in the U.S., slow the pace of innovation, and disrupt other interests and industries. RIB at 191 (citing RX-0004C at

[REDACTED]

Q/A 94-97, 104-110). Specifically, Respondents predict a massive shortfall of x86 processors in the U.S., with the domestic computer manufacturing industry reducing output by 82% and losing 200,000 jobs (*id.* at 191-192 (citing RX-0004C at Q/A 157-161)), with a loss of sales that would cause Intel to cut its research budget (*id.* at 192 (citing RX-0004C at Q/A 44-48, 139; RX-0006C at Q/A 128-130)). As to other interests, Respondents explain “[t]he Proposed Orders would immediately deprive a broad number of U.S. industries, including healthcare, cloud computing, advanced research, and education, of the cutting-edge technology they require.” RIB at 192 (citing RX-0004C at Q/A 133-172; RX-0011C at Q/A 87-91; RX-0006C at Q/A 54-131)); *see* RIB at 192-193.

On this topic, only Respondents’ discussions of the healthcare, research, and education are material, and Respondents have not explained with particularity why these sectors would be harmed by the exclusion orders as opposed to generally observing that they use Accused Products in support of their missions. *See, e.g.*, RIB at 192-193 (citing Hr’g Tr. at 1040:3-6); Hr’g Tr. at 1039:20-1040:22 (“If those hospitals or those companies weren’t – didn’t have access to the latest advances in technology, we wouldn’t be able to get down to the specific genome in a DNA strand that allows you to target precision medicine for cancer. They wouldn’t be able to do some of the research that they have been able to do around Alzheimer’s. They wouldn’t be able to do early spinal cancer detection.”). The Commission has explained “[t]he relevant issue is not whether there is a public health and welfare benefit provided by blood cholesterol testing generally, but rather whether the exclusion of the Accused Products will negatively impact the public health and welfare.” *Certain Blood Cholesterol Testing Strips and Associated Systems Containing the Same*, Inv. No. 337-TA-1116, Comm’n Op. at 34 (May 1, 2020).

This is a critical omission, because Tela’s expert, Dr. Akemann, persuasively testified that there are acceptable substitute x86 processors from AMD in the same sectors discussed by

[REDACTED]

Respondents. *See* RIB at 182-183 (citations omitted); CX-1146C at Q/A 267-302, 616-620; RRB at 95 (“The accused Intel processors are x86 processors.”). Respondents’ response to substitution by AMD is mainly that they are not drop-in replacements, that AMD is not compatible with some of Intel’s unique features such as Optane memory, and that AMD chips generally “do not support the ecosystem of Intel performance, power, and security features described above.” *See* RIB at 188. These incompatibilities, however, are neither unexpected nor insurmountable and otherwise do not take away from the evidence showing AMD x86 processors could substitute even if they have historically had low market share. *See, e.g.*, CRB at 92-93, RX-0004C at Q/A 104-112. Indeed, many of the non-Intel respondents sell computer products including or intended for AMD processors, and which are comparable to their respective Accused Products (*see, e.g.*, CIB at 181 (citing CX-0426; CX-0427), 182 (citing CX-0451; CX-0905; CX-0115; CX-0116; CX-1473; CX-0969; CX-0215; CX-0585; CX-0214; CX-0353C; CX-0584; CX-0897; JX-0227; CX-0142; RX-0966; RX-0967; RX-0968; RX-0969; RX-0976)), and given the prospective nature of the relief, AMD’s rise in desktop, mobile, and server market share and technological competitiveness is particularly relevant (*see* CIB at 179-180 (citing, *inter alia*, CX-1599 at *2-4; CX-1002; CX-0986; CX-1600; RX-0966; CX-1011; RX-0987; JX-0316; JX-0323C; CX-1407; JX-0186C at *3; RX-0805C at *2)).

As to slowed innovation (RIB at 192), this is limited to Intel and its own financial constraints, and the national security complications Respondents warn of (*id.*) are greatly ameliorated by 19 U.S.C. § 1337(l). Further, it is reasonable to assume at this stage that the impact on public health and welfare from computer manufacturers, software designers, and end users switching to AMD-based products (if even necessary given Respondents’ claims of redesign), and

[REDACTED]

Intel products, the non-x86 spaces will also likely see price increases. The evidence is limited as to the extent of those increases, however. RIB at 196 (citing RX-0004C at Q/A 187-193; RX-0011C at Q/A 115). Respondents' arguments regarding OEMs and ODMs (*see id.*) as actors in the supply chain of downstream devices are not relevant here, because they are not end users.

5. Conclusion

In conclusion, a weighing of the factors above does not support outright preclusion of any remedy should a violation be found. The economic impact upon entities who incorporate the Intel Accused Products into their own computer products, and are not named respondents to this investigation, will have the benefit of a delayed enforcement to prepare their operations. Further, it has not been shown that industries with ties to public health and welfare are particularly dependent on the Accused Products, or that the Accused Products are uniquely suited for their computing needs, other than the fact that Intel currently enjoys dominant market share. Additionally, while there will undoubtedly be significantly decreased competition for x86 processor products, and lesser competition in others, this is a natural consequence of the right to exclude under a patent—even in industries as critical as information technology. *See Certain Personal Data and Mobile Communications Devices and Related Software*, Inv. No. 337-TA-710, Comm'n Op. at 69, 83-84 (Dec. 29, 2011). Further, Tela claims, and Respondents do not dispute, that Intel could theoretically employ the services of licensed semiconductor manufacturers TSMC and Samsung to make Intel-designed products—thereby alleviating much of the supply disruption which is the basis of Respondents' public interest concerns. CIB at 187. Further still, to the extent these remedial orders manage to devastate the public interest in the ways alleged by Respondents, the Commission provides modification proceedings for this exact event, which will undoubtedly be acted upon swiftly. 19 C.F.R. § 210.76 ("Whenever any person believes that changed conditions of fact or law, or the public interest, require that an exclusion order, cease and desist



order, or consent order be modified or set aside . . . the Commission make a determination that the conditions which led to the issuance of an exclusion order, cease and desist order, or consent order no longer exist”).

[REDACTED]

IX. INITIAL DETERMINATION AND ORDER

Based on the foregoing,¹⁰ it is my Initial Determination that there is no violation of Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits and products containing the same, in connection with the asserted claims of U.S. Patent Nos. 10,141,334 and 10,186,523.

Furthermore, it is my determination that a domestic industry in the United States that practices or exploits the asserted patents does not exist.

This Initial Determination, together with the record of the hearing in this investigation consisting of the transcript of the evidentiary hearing, with appropriate corrections as may hereafter be ordered, and the exhibits accepted into evidence in this investigation, is hereby certified to the Commission.¹¹

Pursuant to 19 C.F.R. § 210.42(h), this Initial Determination shall become the determination of the Commission sixty (60) days after the date of service of the Initial Determination, unless a party files a petition for review of the Initial Determination within twelve (12) business days after service of the Initial Determination pursuant to 19 C.F.R. § 210.43(a) or the Commission, pursuant to 19 C.F.R. § 210.44, orders on its own motion, a review of the Initial Determination or certain issues therein. Any issue or argument not raised in a petition for review,

¹⁰ The failure to discuss any matter raised by the parties or any portion of the Record herein does not indicate that said matter was not considered. Rather, any such matter(s) or portion(s) of the Record has/have been determined to be irrelevant, immaterial or meritless. Arguments made on brief which were otherwise unsupported by Record evidence or legal precedent have been accorded no weight.

¹¹ The pleadings of the parties filed with the Secretary need not be certified as they are already in the Commission's possession in accordance with Commission rules.



or response thereto, will be deemed to have been abandoned and may be disregarded by the Commission in reviewing the Initial Determination pursuant to 19 C.F.R. § 210.43(b) and (c).

[REDACTED]

Confidentiality Notice:

This Initial Determination is being issued as confidential, and a public version will be issued pursuant to Commission Rule 210.5(f). Within seven (7) days of the date of this Initial Determination, the parties shall jointly submit: (1) a proposed public version of this opinion with any proposed redactions bracketed in red; and (2) a written justification for any proposed redactions specifically explaining why the piece of information sought to be redacted is confidential and why disclosure of the information would be likely to cause substantial harm or likely to have the effect of impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions.¹²

SO ORDERED.



Cameron Elliot
Administrative Law Judge

¹² Under Commission Rules 210.5 and 201.6(a), confidential business information includes: information which concerns or relates to the trade secrets, processes, operations, style of works, or apparatus, or to the production, sales, shipments, purchases, transfers, identification of customers, inventories, or amount or source of any income, profits, losses, or expenditures of any person, firm, partnership, corporation, or other organization, or other information of commercial value, the disclosure of which is likely to have the effect of either impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions, or causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained, unless the Commission is required by law to disclose such information. *See* 19 C.F.R. § 201.6(a). Thus, to constitute confidential business information the disclosure of the information sought to be designated confidential must likely have the effect of either: (1) impairing the Commission's ability to obtain such information as is necessary to perform its statutory functions; or (2) causing substantial harm to the competitive position of the person, firm, partnership, corporation, or other organization from which the information was obtained.

APPENDIX A

PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND	PROCESSOR#	MMID	INTEL	EXTERNAL PRODUCT MARKETING NAME
1272	14nm	BROADWELL	N/A	5Y10	935385		Intel® Core™ M-5Y10 Processor (4M Cache, up to 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3755U	936718		Intel® Celeron® Processor 3755U (2M Cache, 1.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y70	937141		Intel® Core™ M-5Y70 Processor (4M Cache, up to 2.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	N/A	937248		MBL [BROADWELL] Processor ULV 2.00 GHz, 3M Cache, FC-BGA14F, Tray, 15W, FH8065801620203
1272	14nm	BROADWELL	N/A	N/A	937249		MBL [BROADWELL] Processor ULV 2.00 GHz, 3M Cache, FC-BGA14F, Tray, 15W, FH8065801620403
1272	14nm	BROADWELL	INTEL(R) PENTIUM(R)	3805U	937255		Intel® Pentium® Processor 3805U (2M Cache, 1.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3755U	937258		Intel® Celeron® Processor 3755U (2M Cache, 1.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3205U	937260		Intel® Celeron® Processor 3205U (2M Cache, 1.50 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y70	937262		Intel® Core™ M-5Y70 Processor (4M Cache, up to 2.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y10	937263		Intel® Core™ M-5Y10 Processor (4M Cache, up to 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y10A	937264		Intel® Core™ M-5Y10a Processor (4M Cache, up to 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y10	937418		Intel® Core™ M-5Y10 Processor (4M Cache, up to 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5600U	937723		Intel® Core™ i7-5600U Processor (4M Cache, up to 3.20 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5200U	937726		Intel® Core™ i5-5200U Processor (3M Cache, up to 2.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3215U	937732		Intel® Celeron® Processor 3215U (2M Cache, 1.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5015U	937735		Intel® Core™ i3-5015U Processor (3M Cache, 2.10 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5257U	937776		Intel® Core™ i5-5257U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	N/A	938695		MBL [SKYLAKE] Processor ULV 1.00 GHz, 4M Cache, FC-BGA14C, Tray, 20W, HE8066201922822
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	N/A	938728		DT [SKYLAKE] Processor 2.20 GHz, 8M Cache, FC-LGA14C, Tray, 80W, CM8066202070833
1272	14nm	BROADWELL	N/A	5Y10C	939310		Intel® Core™ M-5Y10c Processor (4M Cache, up to 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y31	939314		Intel® Core™ M-5Y31 Processor (4M Cache, up to 2.40 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y51	939327		Intel® Core™ M-5Y51 Processor (4M Cache, up to 2.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	5Y71	939331		Intel® Core™ M-5Y71 Processor (4M Cache, up to 2.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5600U	939359		Intel® Core™ i7-5600U Processor (4M Cache, up to 3.20 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5500U	939360		Intel® Core™ i7-5500U Processor (4M Cache, up to 3.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5300U	939361		Intel® Core™ i5-5300U Processor (3M Cache, up to 2.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5200U	939362		Intel® Core™ i5-5200U Processor (3M Cache, up to 2.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5010U	939363		Intel® Core™ i3-5010U Processor (3M Cache, 2.10 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5020U	939364		Intel® Core™ i3-5020U Processor (3M Cache, 2.20 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3765U	939366		Intel® Celeron® Processor 3765U (2M Cache, 1.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CELERON(R)	3215U	939367		Intel® Celeron® Processor 3215U (2M Cache, 1.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5005U	939368		Intel® Core™ i3-5005U Processor (3M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5015U	939369		Intel® Core™ i3-5015U Processor (3M Cache, 2.10 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	3825U	939519		Intel® Pentium® Processor 3825U (2M Cache, 1.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	3825U	939531		Intel® Pentium® Processor 3825U (2M Cache, 1.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5650U	939655		Intel® Core™ i7-5650U Processor (4M Cache, up to 3.20 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5350U	939656		Intel® Core™ i5-5350U Processor (3M Cache, up to 2.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5550U	939658		Intel® Core™ i7-5550U Processor (4M Cache, up to 3.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5250U	939660		Intel® Core™ i5-5250U Processor (3M Cache, up to 2.70 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	17-5557U	939662		Intel® Core™ i7-5557U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5287U	939670		Intel® Core™ i5-5287U Processor (3M Cache, up to 3.30 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	15-5257U	939672		Intel® Core™ i5-5257U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5157U	939674		Intel® Core™ i3-5157U Processor (3M Cache, 2.50 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	N/A	13-5005U	940707		Intel® Core™ i3-5005U Processor (3M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	N/A	942317		MBL [SKYLAKE] Processor ULV 1.60 GHz, 4M Cache, FC-BGA14C, Tray, 15W, FJ8066201930823
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1540	942392		Intel® Xeon® Processor D-1540 (12M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1520	942393		Intel® Xeon® Processor D-1520 (6M Cache, 2.20 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	17-6500U	942759		Intel® Core™ i7-6500U Processor (4M Cache, up to 3.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	15-6300U	942760		Intel® Core™ i5-6300U Processor (3M Cache, up to 3.00 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	15-6200U	942761		Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	M3-6Y30	942802		Intel® Core™ m3-6Y30 Processor (4M Cache, up to 2.20 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	M7-6Y75	942808		Intel® Core™ m7-6Y75 Processor (4M Cache, up to 3.00 GHz) FC-BGA14C, Tray

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1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	M5-6Y57	942810		Intel® Core™ m5-6Y57 Processor (4M Cache, up to 2.80 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) CORE(TM) I5	I5-5675C	942888		Intel® Core™ i5-5675C Processor (4M Cache, up to 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400T	943084		Intel® Core™ i5-6400T Processor (6M Cache, up to 2.80 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700	943086		Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	943093		Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	943095		Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500T	943096		Intel® Core™ i5-6500T Processor (6M Cache, up to 3.10 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) PROCESSOR	I3-6100U	943140		Intel® Core™ i3-6100U Processor (3M Cache, 2.30 GHz) FC-BGA14C, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	N/A	943307		SRV [KNIGHTS LANDING] Processor 1.20 GHz, 30M Cache, FC-LGA14B, Tray, 215W, HJ8066702268801
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5775C	943363		Intel® Core™ i7-5775C Processor (6M Cache, up to 3.70 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) CORE(TM) I5	I5-5675R	943366		Intel® Core™ i5-5675R Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CORE(TM) I5	I5-5575R	943367		Intel® Core™ i5-5575R Processor (4M Cache, up to 3.30 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5775R	943368		Intel® Core™ i7-5775R Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E3-1270LV4	943401		Intel® Xeon® Processor E3-1270L v4 (6M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E3-1285LV4	943403		Intel® Xeon® Processor E3-1285L v4 (6M Cache, 3.40 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E3-1265LV4	943404		Intel® Xeon® Processor E3-1265L v4 (6M Cache, 2.30 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E3-1284LV4	943407		Intel® Xeon® Processor E3-1284L v4 (6M Cache, 2.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5850HQ	943430		Intel® Core™ i7-5850HQ Processor (6M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5950HQ	943431		Intel® Core™ i7-5950HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5700HQ	943450		Intel® Core™ i7-5700HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700K	943463		Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400T	943464		Intel® Core™ i5-6400T Processor (6M Cache, up to 2.80 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700	943466		Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	943467		Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600	943468		Intel® Core™ i5-6600 Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	943469		Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	943470		Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500T	943471		Intel® Core™ i5-6500T Processor (6M Cache, up to 3.10 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600T	943472		Intel® Core™ i5-6600T Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	943473		Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1280V5	943544		Intel® Xeon® Processor E3-1280 v5 (8M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240V5	943545		Intel® Xeon® Processor E3-1240 v5 (8M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1230V5	943546		Intel® Xeon® Processor E3-1230 v5 (8M Cache, 3.40 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1270V5	943547		Intel® Xeon® Processor E3-1270 v5 (8M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1220V5	943548		Intel® Xeon® Processor E3-1220 v5 (8M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1260LV5	943549		Intel® Xeon® Processor E3-1260L v5 (8M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1225V5	943550		Intel® Xeon® Processor E3-1225 v5 (8M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1275V5	943551		Intel® Xeon® Processor E3-1275 v5 (8M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1245V5	943552		Intel® Xeon® Processor E3-1245 v5 (8M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1235LV5	943553		Intel® Xeon® Processor E3-1235L v5 (8M Cache, 2.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240LV5	943554		Intel® Xeon® Processor E3-1240L v5 (8M Cache, 2.10 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6440HQ	943599		Intel® Core™ i5-6440HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E3-1285V4	943660		Intel® Xeon® Processor E3-1285 v4 (6M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5775C	943661		Intel® Xeon® Processor E3-1270L v4 (6M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-5775C	943887		Boxed Intel® Core™ i7-5775C Processor (6M Cache, up to 3.70 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	943907		Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	943908		Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1541	943943		Intel® Xeon® Processor D-1541 (12M Cache, 2.10 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1548	943950		Intel® Xeon® Processor D-1548 (12M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1528	943953		Intel® Xeon® Processor D-1528 (9M Cache, 1.90 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1541	944000		Intel® Xeon® Processor D-1541 (12M Cache, 2.10 GHz) FC-BGA14C, Tray

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1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1521	944001		Intel® Xeon® Processor D-1521 (6M Cache, 2.40 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1531	944002		Intel® Xeon® Processor D-1531 (9M Cache, 2.20 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1539	944005		Intel® Xeon® Processor D-1539 (1.2M Cache, 1.60 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1548	944006		Intel® Xeon® Processor D-1548 (1.2M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1527	944007		Intel® Xeon® Processor D-1527 (6M Cache, 2.20 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1528	944008		Intel® Xeon® Processor D-1528 (9M Cache, 1.90 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Pentium(R)	D1519	944009		Intel® Pentium® Processor D1519 (6M Cache, 1.50 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1518	944010		Intel® Xeon® Processor D-1518 (6M Cache, 2.20 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Pentium(R)	D1507	944011		Intel® Pentium® Processor D1507 (3M Cache, 1.20 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Pentium(R)	D1508	944012		Intel® Pentium® Processor D1508 (3M Cache, 2.20 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1529	944013		Intel® Xeon® Processor D-1529 (6M Cache, 1.30 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	17-6820EQ	944028		Intel® Core™ i7-6820EQ Processor (8M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6400	944035		Boxed Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6440EQ	944037		Intel® Core™ i5-6440EQ Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I3	I3-6100E	944045		Intel® Core™ i3-6100E Processor (3M Cache, up to 2.80 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	17-6822EQ	944047		Intel® Core™ i7-6822EQ Processor (8M Cache, up to 2.80 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I3	I3-6102E	944050		Intel® Core™ i3-6102E Processor (3M Cache, up to 2.70 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6442EQ	944051		Intel® Core™ i5-6442EQ Processor (6M Cache, up to 2.70 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1505LV5	944067		Intel® Xeon® Processor E3-1505LV5 (8M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)CORE(TM)I7	17-5700EQ	944074		Intel® Xeon® Processor E3-1278LV4 (6M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E3-1278LV4	944075		Intel® Xeon® Processor E3-1278LV4 (6M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)CORE(TM)I7	17-5850EQ	944076		Intel® Xeon® Processor E3-1258LV4 (6M Cache, 1.80 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E3-1258LV4	944077		Intel® Xeon® Processor E3-1258LV4 (6M Cache, 1.80 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E3-1283LV4	944090		Intel® Xeon® Processor E3-1283LV4 (6M Cache, 2.90 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)M	M5-6Y57	944320		Intel® Core™ m5-6Y57 Processor (4M Cache, up to 2.80 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)M	M7-6Y75	944321		Intel® Core™ m7-6Y75 Processor (4M Cache, up to 3.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)M	M5-6Y54	944325		Intel® Core™ m5-6Y54 Processor (4M Cache, up to 2.70 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)M	M3-6Y30	944326		Intel® Core™ m3-6Y30 Processor (4M Cache, up to 2.20 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)Pentium(R)	4405Y	944330		Intel® Pentium® Processor 4405Y (2M Cache, 1.50 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I3	I3-6100U	944334		Intel® Core™ i3-6100U Processor (3M Cache, 2.30 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CELERON(R)	3855U	944335		Intel® Celeron® Processor 3855U (2M Cache, 1.60 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CELERON(R)	3955U	944336		Intel® Celeron® Processor 3955U (2M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)Pentium(R)	4405U	944337		Intel® Pentium® Processor 4405U (2M Cache, 2.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6200U	944338		Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6500U	944339		Intel® Core™ i7-6500U Processor (4M Cache, up to 3.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6300U	944340		Intel® Core™ i5-6300U Processor (3M Cache, up to 3.00 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6600U	944341		Intel® Core™ i7-6600U Processor (4M Cache, up to 3.40 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	17-6820HK	944356		Intel® Core™ i7-6820HK Processor (8M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1535MV5	944365		Intel® Xeon® Processor E3-1535M v5 (8M Cache, 2.90 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1505MV5	944366		Intel® Xeon® Processor E3-1505M v5 (8M Cache, 2.80 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6300HQ	944367		Intel® Core™ i5-6300HQ Processor (6M Cache, up to 3.20 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6700HQ	944368		Intel® Core™ i7-6700HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I3	I3-6100H	944369		Intel® Core™ i3-6100H Processor (3M Cache, 2.70 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6440HQ	944370		Intel® Core™ i5-6440HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6920HQ	944371		Intel® Core™ i7-6920HQ Processor (8M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	17-6820HQ	944372		Intel® Core™ i7-6820HQ Processor (8M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	D-1537	944377		Intel® Xeon® Processor D-1537 (1.2M Cache, 1.70 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)CORE(TM)I5	I5-5675C	944383		Intel® Core™ i5-5675C Processor (4M Cache, up to 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6700K	944458		Boxed Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I7	I7-6700	944459		Boxed Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6600K	944460		Boxed Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R)CORE(TM)I5	I5-6600	944461		Boxed Intel® Core™ i5-6600 Processor (6M Cache, up to 3.90 GHz) FC-LGA14C

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1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	944462		Boxed Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	944464		Boxed Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700K	944469		Boxed Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700	944470		Boxed Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	944472		Boxed Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600	944473		Boxed Intel® Core™ i5-6600 Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	944474		Boxed Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	944475		Boxed Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, for China
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1537	944484		Intel® Xeon® Processor D-1537 (1.2M Cache, 1.70 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) PENTIUM(R)	D1517	944485		Intel® Pentium® Processor D1517 (6M Cache, 1.60 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240V5	944496		Boxed Intel® Xeon® Processor E3-1240 v5 (8M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1230V5	944497		Boxed Intel® Xeon® Processor E3-1230 v5 (8M Cache, 3.40 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1270V5	944498		Boxed Intel® Xeon® Processor E3-1270 v5 (8M Cache, 3.60 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1275V5	944499		Boxed Intel® Xeon® Processor E3-1275 v5 (8M Cache, 3.60 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1245V5	944500		Boxed Intel® Xeon® Processor E3-1245 v5 (8M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1220V5	944506		Boxed Intel® Xeon® Processor E3-1220 v5 (8M Cache, 3.00 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1225V5	944507		Boxed Intel® Xeon® Processor E3-1225 v5 (8M Cache, 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900E	944534		Intel® Celeron® Processor G3900E (2M Cache, 2.40 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3902E	944537		Intel® Celeron® Processor G3902E (2M Cache, 1.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) CORE(TM) I5	I5-5675C	944548		Boxed Intel® Core™ i5-5675C Processor (4M Cache, up to 3.60 GHz) FC-LGA14C
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2695V4	944676		Intel® Xeon® Processor E5-2695 v4 (45M Cache, 2.10 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2696V4	944679		Intel® Xeon® Processor E5-2696 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6300	944894		Intel® Core™ i3-6300 Processor (4M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6300T	944897		Intel® Core™ i3-6300T Processor (3M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100T	944899		Intel® Core™ i3-6100T Processor (3M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100	944901		Intel® Core™ i3-6100 Processor (3M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	944906		Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400T	944925		Intel® Pentium® Processor G4400T (3M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900T	944927		Intel® Celeron® Processor G3900T (2M Cache, 2.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6260U	945073		Intel® Core™ i5-6260U Processor (4M Cache, up to 2.90 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6320	945192		Intel® Core™ i3-6320 Processor (4M Cache, 3.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6300	945193		Intel® Core™ i3-6300 Processor (4M Cache, 3.80 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6300T	945205		Intel® Core™ i3-6300T Processor (4M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100T	945206		Intel® Core™ i3-6100T Processor (3M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100	945208		Intel® Core™ i3-6100 Processor (3M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4500	945269		Intel® Pentium® Processor G4500 (3M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4520	945298		Intel® Pentium® Processor G4520 (3M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400T	945362		Intel® Pentium® Processor G4400T (3M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4500T	945382		Intel® Pentium® Processor G4500T (3M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900T	945383		Intel® Celeron® Processor G3900T (2M Cache, 2.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900	945385		Intel® Celeron® Processor G3900 (2M Cache, 2.80 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3920	945387		Intel® Celeron® Processor G3920 (2M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	N/A	I5-5200U	945390		Intel® Core™ i5-5200U Processor (3M Cache, up to 2.70 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2695V4	945399		Intel® Xeon® Processor E5-2695 v4 (45M Cache, 2.10 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2696V4	945449		Intel® Xeon® Processor E5-2696 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2695V4	945450		Intel® Xeon® Processor E5-2695 v4 (45M Cache, 2.10 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	N/A	945460		SRV [BROADWELL] Processor 2.10 GHz, 20M Cache, 8.000 GT/s Intel® QPI, FC-LGA14A, Tray, 85W, CMR8066002032201
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I3	I3-6300	945508		Boxed Intel® Core™ i3-6300 Processor (4M Cache, 3.80 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6300T	945509		Boxed Intel® Core™ i3-6300T Processor (3M Cache, 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100T	945510		Boxed Intel® Core™ i3-6100T Processor (3M Cache, 3.20 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100	945511		Boxed Intel® Core™ i3-6100 Processor (3M Cache, 3.70 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900	945512		Boxed Intel® Celeron® Processor G3900 (2M Cache, 2.80 GHz) FC-LGA14C

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1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3920	945913		Boxed Intel® Celeron® Processor G3920 (2M Cache, 2.90 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6300	945914		Boxed Intel® Core™ i3-6300 Processor (4M Cache, 3.80 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6100T	945917		Boxed Intel® Core™ i3-6100T Processor (3M Cache, 3.20 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6100	945918		Boxed Intel® Core™ i3-6100 Processor (3M Cache, 3.70 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900	945919		Boxed Intel® Celeron® Processor G3900 (2M Cache, 2.80 GHz) FC-LGA14C, for China
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2683V4	945949		Intel® Xeon® Processor E5-2683 v4 (40M Cache, 2.10 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2698V4	945951		Intel® Xeon® Processor E5-2698 v4 (50M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	946002		Boxed Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4500	946003		Boxed Intel® Pentium® Processor G4500 (3M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	946004		Boxed Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4520	946006		Boxed Intel® Pentium® Processor G4520 (3M Cache, 3.60 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	946007		Boxed Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4500	946008		Boxed Intel® Pentium® Processor G4500 (3M Cache, 3.50 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	G4400	946009		Boxed Intel® Pentium® Processor G4400 (3M Cache, 3.30 GHz) FC-LGA14C, for China
1272	14nm	BROADWELL	INTEL(R) PENTIUM(R)	D1509	946072		Intel® Pentium® Processor D1509 (3M Cache, 1.50 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6320	946089		Boxed Intel® Core™ i3-6320 Processor (4M Cache, 3.90 GHz) FC-LGA14C
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2690V4	946091		Intel® Xeon® Processor E5-2690 v4 (35M Cache, 2.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2660V4	946093		Intel® Xeon® Processor E5-2660 v4 (35M Cache, 2.00 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2680V4	946098		Intel® Xeon® Processor E5-2680 v4 (35M Cache, 2.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2650LV4	946099		Intel® Xeon® Processor E5-2650L v4 (35M Cache, 1.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2658V4	946107		Intel® Xeon® Processor E5-2658 v4 (35M Cache, 2.30 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6560U	946138		Intel® Core™ i7-6560U Processor (4M Cache, up to 3.20 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6167U	946143		Intel® Core™ i3-6167U Processor (4M Cache, up to 2.90 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3	I3-6006U	946153		Intel® Core™ i3-6006U Processor (3M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6567U	946157		Intel® Core™ i7-6567U Processor (3M Cache, 2.70 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I5	I5-6287U	946159		Intel® Core™ i5-6287U Processor (4M Cache, up to 3.50 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I5	I5-6267U	946162		Intel® Core™ i5-6267U Processor (4M Cache, up to 3.30 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6660U	946161		Intel® Core™ i7-6660U Processor (4M Cache, up to 3.40 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I5	I5-6360U	946162		Intel® Core™ i5-6360U Processor (4M Cache, up to 3.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6785R	946208		Intel® Core™ i7-6785R Processor (8M Cache, up to 3.90 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2699V4	946675		Intel® Xeon® Processor E5-2699 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2683V4	946676		Intel® Xeon® Processor E5-2683 v4 (40M Cache, 2.10 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2697V4	946678		Intel® Xeon® Processor E5-2697 v4 (45M Cache, 2.30 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2698V4	946679		Intel® Xeon® Processor E5-2698 v4 (50M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2676V4	946681		Intel® Xeon® Processor E5-2676 v4 (40M Cache, 2.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2697AV4	946684		Intel® Xeon® Processor E5-2697A v4 (40M Cache, 2.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2682V4	946687		Intel® Xeon® Processor E5-2682 v4 (40M Cache, 2.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2679V4	946688		Intel® Xeon® Processor E5-2679 v4 (50M Cache, 2.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2689V4	946690		Intel® Xeon® Processor E5-2689 v4 (25M Cache, 3.10 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2686V4	946691		Intel® Xeon® Processor E5-2686 v4 (45M Cache, 2.30 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6650U	946722		Intel® Core™ i7-6650U Processor (4M Cache, up to 3.40 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2673V4	946773		Intel® Xeon® Processor E5-2673 v4 (50M Cache, 2.30 GHz) FC-LGA14A, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	28330	947028		Intel® Atom™ x5-28330 Processor (2M Cache, up to 1.92 GHz) FC-BGA15F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2609V4	947112		Intel® Xeon® Processor E5-2609 v4 (20M Cache, 1.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2637V4	947115		Intel® Xeon® Processor E5-2637 v4 (15M Cache, 3.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2667V4	947117		Intel® Xeon® Processor E5-2667 v4 (25M Cache, 3.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-1603V4	947135		Intel® Xeon® Processor E5-1603 v4 (10M Cache, 2.80 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6700K	947200		Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I5	I5-6400T	947201		Intel® Core™ i5-6400T Processor (6M Cache, up to 2.80 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6700	947202		Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6700T	947203		Intel® Core™ i7-6700T Processor (8M Cache, up to 3.60 GHz) FC-LGA14C, Tray

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1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	947204		Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600	947205		Intel® Core™ i5-6600 Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	947206		Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	947207		Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500T	947208		Intel® Core™ i5-6500T Processor (6M Cache, up to 3.10 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600T	947209		Intel® Core™ i5-6600T Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1280V5	947224		Intel® Xeon® Processor E3-1280 v5 (8M Cache, 3.70 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240V5	947225		Intel® Xeon® Processor E3-1240 v5 (8M Cache, 3.50 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1230V5	947228		Intel® Xeon® Processor E3-1230 v5 (8M Cache, 3.40 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1270V5	947229		Intel® Xeon® Processor E3-1270 v5 (8M Cache, 3.60 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1220V5	947230		Intel® Xeon® Processor E3-1220 v5 (8M Cache, 3.00 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1260LV5	947234		Intel® Xeon® Processor E3-1260L v5 (8M Cache, 2.90 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1225V5	947247		Intel® Xeon® Processor E3-1225 v5 (8M Cache, 3.30 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1275V5	947248		Intel® Xeon® Processor E3-1275 v5 (8M Cache, 3.60 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1245V5	947249		Intel® Xeon® Processor E3-1245 v5 (8M Cache, 3.50 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1235LV5	947250		Intel® Xeon® Processor E3-1235L v5 (8M Cache, 2.00 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240LV5	947252		Intel® Xeon® Processor E3-1240L v5 (8M Cache, 2.10 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700TE	947253		Intel® Core™ i7-6700TE Processor (8M Cache, up to 3.40 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1268LV5	947254		Intel® Xeon® Processor E3-1268L v5 (8M Cache, 2.40 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500TE	947257		Intel® Core™ i5-6500TE Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6100TE	947268		Intel® Core™ i3-6100TE Processor (4M Cache, 2.70 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) PENTIUM(M) R	G4000TE	947270		Intel® Pentium® Processor G4000TE (3M Cache, 2.40 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	G3900TE	947271		Intel® Celeron® Processor G3900TE (2M Cache, 2.30 GHz) FC-LGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1581	947370		Intel® Xeon® Processor D-1581 (24M Cache, 1.80 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1571	947371		Intel® Xeon® Processor D-1571 (24M Cache, 1.30 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1587	947372		Intel® Xeon® Processor D-1587 (24M Cache, 1.70 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1577	947373		Intel® Xeon® Processor D-1577 (24M Cache, 1.30 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1567	947374		Intel® Xeon® Processor D-1567 (18M Cache, 2.10 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1557	947375		Intel® Xeon® Processor D-1557 (18M Cache, 1.50 GHz) FC-BGA14C, Tray	
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1559	947376		Intel® Xeon® Processor D-1559 (18M Cache, 1.50 GHz) FC-BGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1240V5	947516		Boxed Intel® Xeon® Processor E3-1240 v5 (8M Cache, 3.50 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1230V5	947517		Boxed Intel® Xeon® Processor E3-1230 v5 (8M Cache, 3.40 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1270V5	947518		Boxed Intel® Xeon® Processor E3-1270 v5 (8M Cache, 3.60 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1220V5	947519		Boxed Intel® Xeon® Processor E3-1220 v5 (8M Cache, 3.00 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1225V5	947521		Boxed Intel® Xeon® Processor E3-1225 v5 (8M Cache, 3.30 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1275V5	947522		Boxed Intel® Xeon® Processor E3-1275 v5 (8M Cache, 3.60 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	E3-1245V5	947523		Boxed Intel® Xeon® Processor E3-1245 v5 (8M Cache, 3.50 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400T	947546		Boxed Intel® Core™ i5-6400T Processor (6M Cache, up to 2.80 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700T	947547		Boxed Intel® Core™ i7-6700T Processor (8M Cache, up to 3.60 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500T	947548		Boxed Intel® Core™ i5-6500T Processor (6M Cache, up to 3.10 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600T	947549		Boxed Intel® Core™ i5-6600T Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700K	947558		Boxed Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700	947559		Boxed Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	947560		Boxed Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	947561		Boxed Intel® Core™ i5-6500 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	947562		Boxed Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	947563		Boxed Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700K	947565		Boxed Intel® Core™ i7-6700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6700	947566		Boxed Intel® Core™ i7-6700 Processor (8M Cache, up to 4.00 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600K	947567		Boxed Intel® Core™ i5-6600K Processor (6M Cache, up to 3.90 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6600	947568		Boxed Intel® Core™ i5-6600 Processor (6M Cache, up to 3.60 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6500	947569		Boxed Intel® Core™ i5-6500 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, for China	

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1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6400	947570	Intel®	Boxed Intel® Core™ i5-6400 Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, for China
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7250	947605	Intel®	Intel® Xeon Phi™ Processor 7250 (16GB, 1.40 GHz, 68 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	N/A	947606	Intel®	Intel® Xeon Phi™ Processor 7210 (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7210	947607	Intel®	Intel® Xeon Phi™ Processor 7210 (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7230	947609	Intel®	Intel® Xeon Phi™ Processor 7230 (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2690V4	947614	Intel®	Intel® Xeon® Processor E5-2690 v4 (35M Cache, 2.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2650V4	947616	Intel®	Intel® Xeon® Processor E5-2650 v4 (30M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2660V4	947617	Intel®	Intel® Xeon® Processor E5-2660 v4 (35M Cache, 2.00 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2680V4	947620	Intel®	Intel® Xeon® Processor E5-2680 v4 (35M Cache, 2.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2650LV4	947622	Intel®	Intel® Xeon® Processor E5-2650 v4 (35M Cache, 1.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2666V4	947623	Intel®	Intel® Xeon® Processor E5-2666 v4 (30M Cache, 2.80 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2687WV4	947624	Intel®	Intel® Xeon® Processor E5-2687 v4 (30M Cache, 3.00 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2658V4	947636	Intel®	Intel® Xeon® Processor E5-2658 v4 (35M Cache, 2.30 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2628LV4	947637	Intel®	Intel® Xeon® Processor E5-2628 v4 (30M Cache, 1.90 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2648LV4	947638	Intel®	Intel® Xeon® Processor E5-2648 v4 (35M Cache, 1.80 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2671V4	947639	Intel®	Intel® Xeon® Processor E5-2671 v4 (35M Cache, 2.30 GHz) FC-LGA14A, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700	947686	Intel®	Intel® Core™ i7-7700 Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500	947688	Intel®	Intel® Core™ i5-7500 Processor (6M Cache, up to 3.80 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700T	947690	Intel®	Intel® Core™ i7-7700T Processor (8M Cache, up to 3.80 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600T	947691	Intel®	Intel® Core™ i5-7600T Processor (6M Cache, up to 3.70 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500T	947692	Intel®	Intel® Core™ i5-7500T Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400T	947693	Intel®	Intel® Core™ i5-7400T Processor (6M Cache, up to 3.00 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2695V4	947739	Boxed Intel®	Boxed Intel® Xeon® Processor E5-2695 v4 (45M Cache, 2.10 GHz) FC-LGA14A
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2660V4	947734	Boxed Intel®	Boxed Intel® Xeon® Processor E5-2660 v4 (35M Cache, 2.00 GHz) FC-LGA14A
1273	14nm	APOLLO LAKE	GENUINE INTEL (R) CPU	N/A	947983	DT [APOLLO LAKE]	DT [APOLLO LAKE] Processor ULV, 2M Cache, FC-BGA15F, Tray, 10W, FH8066802588601
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6402P	947992	Intel®	Intel® Core™ i5-6402P Processor (6M Cache, up to 3.40 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2683V4	948034	Boxed Intel®	Boxed Intel® Xeon® Processor E5-2683 v4 (40M Cache, 2.10 GHz) FC-LGA14A
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2697V4	948035	Boxed Intel®	Boxed Intel® Xeon® Processor E5-2697 v4 (45M Cache, 2.30 GHz) FC-LGA14A
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2695V4	948059	Boxed Intel®	Boxed Intel® Xeon® Processor E5-2695 v4 (45M Cache, 2.10 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6098P	948062	Intel®	Intel® Core™ i3-6098P Processor (3M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6198DU	948065	Intel®	Intel® Core™ i5-6198DU Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-6498DU	948066	Intel®	Intel® Core™ i7-6498DU Processor (4M Cache, up to 3.10 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6402P	948102	Intel®	Intel® Core™ i5-6402P Processor (6M Cache, up to 3.40 GHz) FC-LGA14C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM) I5	N/A	948107	EMB [APOLLO LAKE]	EMB [APOLLO LAKE] Processor ULV, 2M Cache, FC-BGA15C, Tray, 13W, LH8066802599101
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	N/A	948116	EMB [APOLLO LAKE]	EMB [APOLLO LAKE] Processor ULV, 2M Cache, FC-BGA15C, Tray, 13W, LH8066802599203
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2640V4	948123	Intel®	Intel® Xeon® Processor E5-2640 v4 (25M Cache, 2.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2603V4	948124	Intel®	Intel® Xeon® Processor E5-2603 v4 (15M Cache, 1.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2609V4	948125	Intel®	Intel® Xeon® Processor E5-2609 v4 (20M Cache, 1.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2630LV4	948126	Intel®	Intel® Xeon® Processor E5-2630 v4 (25M Cache, 1.80 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2637V4	948127	Intel®	Intel® Xeon® Processor E5-2637 v4 (15M Cache, 3.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2643V4	948128	Intel®	Intel® Xeon® Processor E5-2643 v4 (20M Cache, 3.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2667V4	948129	Intel®	Intel® Xeon® Processor E5-2667 v4 (25M Cache, 3.20 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-1620V4	948130	Intel®	Intel® Xeon® Processor E5-1620 v4 (10M Cache, 3.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-1650V4	948131	Intel®	Intel® Xeon® Processor E5-1650 v4 (15M Cache, 3.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-1680V4	948132	Intel®	Intel® Xeon® Processor E5-1680 v4 (20M Cache, 3.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2608LV4	948136	Intel®	Intel® Xeon® Processor E5-2608 v4 (20M Cache, 1.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6950X	948137	Intel®	Intel® Core™ i7-6950X Processor Extreme Edition (25M Cache, up to 3.50 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6900K	948138	Intel®	Intel® Core™ i7-6900K Processor (20M Cache, up to 3.70 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6850K	948139	Intel®	Intel® Core™ i7-6850K Processor (15M Cache, up to 3.80 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6800K	948140	Intel®	Intel® Core™ i7-6800K Processor (15M Cache, up to 3.60 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2618LV4	948141	Intel®	Intel® Xeon® Processor E5-2618 v4 (25M Cache, 2.20 GHz) FC-LGA14A, Tray

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1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-1630V4	948142	Intel® Xeon® Processor E5-1630 v4 (10M Cache, 3.70 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-1603V4	948143	Intel® Xeon® Processor E5-1603 v4 (10M Cache, 2.80 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-1607V4	948144	Intel® Xeon® Processor E5-1607 v4 (10M Cache, 3.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2623V4	948145	Intel® Xeon® Processor E5-2623 v4 (10M Cache, 2.60 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-1660V4	948146	Intel® Xeon® Processor E5-1660 v4 (20M Cache, 3.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2690V4	948197	Boxed Intel® Xeon® Processor E5-2690 v4 (35M Cache, 2.60 GHz) FC-LGA14A	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2650V4	948198	Boxed Intel® Xeon® Processor E5-2650 v4 (30M Cache, 2.20 GHz) FC-LGA14A	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2660V4	948199	Boxed Intel® Xeon® Processor E5-2660 v4 (35M Cache, 2.00 GHz) FC-LGA14A	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2680V4	948200	Boxed Intel® Xeon® Processor E5-2680 v4 (35M Cache, 2.40 GHz) FC-LGA14A	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2687V4	948206	Boxed Intel® Xeon® Processor E5-2687 v4 (30M Cache, 3.00 GHz) FC-LGA14A	
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6700HQ	948244	Intel® Core™ i7-6700HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6402P	948516	Boxed Intel® Core™ i5-6402P Processor (6M Cache, up to 3.40 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I3	I3-6098P	948517	Boxed Intel® Core™ i3-6098P Processor (3M Cache, 3.60 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6402P	948518	Boxed Intel® Core™ i5-6402P Processor (6M Cache, up to 3.40 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I3	I3-6098P	948520	Boxed Intel® Core™ i3-6098P Processor (3M Cache, 3.60 GHz) FC-LGA14C, for China	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2609V4	948609	Boxed Intel® Xeon® Processor E5-2609 v4 (20M Cache, 1.70 GHz) FC-LGA14A	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1515MV5	948619	Intel® Xeon® Processor E3-1515M v5 (8M Cache, 2.80 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1545MV5	948620	Intel® Xeon® Processor E3-1545M v5 (8M Cache, 2.90 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1575MV5	948621	Intel® Xeon® Processor E3-1575M v5 (8M Cache, 3.00 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6970HQ	948622	Intel® Core™ i7-6970HQ Processor (8M Cache, up to 3.70 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6870HQ	948623	Intel® Core™ i7-6870HQ Processor (8M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-6770HQ	948624	Intel® Core™ i7-6770HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6350HQ	948625	Intel® Core™ i5-6350HQ Processor (6M Cache, up to 3.20 GHz) FC-BGA14F, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2630V4	948649	Intel® Xeon® Processor E5-2630 v4 (25M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2620V4	948659	Intel® Xeon® Processor E5-2620 v4 (20M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-2630V4	948660	Intel® Xeon® Processor E5-2630 v4 (25M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1565LV5	948665	Intel® Xeon® Processor E3-1565L v5 (8M Cache, 2.50 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1585LV5	948666	Intel® Xeon® Processor E3-1585L v5 (8M Cache, 3.00 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	E3-1585V5	948668	Intel® Xeon® Processor E3-1585 v5 (8M Cache, 3.50 GHz) FC-BGA14F, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8870V4	948733	Intel® Xeon® Processor E7-8870 v4 (50M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-4850V4	948735	Intel® Xeon® Processor E7-4850 v4 (40M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-4830V4	948737	Intel® Xeon® Processor E7-4830 v4 (35M Cache, 2.00 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-4820V4	948738	Intel® Xeon® Processor E7-4820 v4 (25M Cache, 2.00 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-4820V4	948739	Intel® Xeon® Processor E7-4820 v4 (25M Cache, 2.00 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-4809V4	948741	Intel® Xeon® Processor E7-4809 v4 (20M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8867V4	948742	Intel® Xeon® Processor E7-8867 v4 (45M Cache, 2.40 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8880V4	948743	Intel® Xeon® Processor E7-8880 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8880V4	948745	Intel® Xeon® Processor E7-8880 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8860V4	948747	Intel® Xeon® Processor E7-8860 v4 (45M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E7-8855V4	948749	Intel® Xeon® Processor E7-8855 v4 (35M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4650V4	948752	Intel® Xeon® Processor E5-4650 v4 (35M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4628LV4	948754	Intel® Xeon® Processor E5-4628L v4 (35M Cache, 1.80 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4640V4	948756	Intel® Xeon® Processor E5-4640 v4 (30M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4660V4	948758	Intel® Xeon® Processor E5-4660 v4 (40M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4610V4	948762	Intel® Xeon® Processor E5-4610 v4 (25M Cache, 1.80 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4667V4	948764	Intel® Xeon® Processor E5-4667 v4 (45M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4669V4	948767	Intel® Xeon® Processor E5-4669 v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4655V4	948768	Intel® Xeon® Processor E5-4655 v4 (30M Cache, 2.50 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4655V4	948769	Intel® Xeon® Processor E5-4655 v4 (30M Cache, 2.50 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4620V4	948771	Intel® Xeon® Processor E5-4620 v4 (25M Cache, 2.10 GHz) FC-LGA14A, Tray	
1272	14nm	BROADWELL	INTEL(R)Xeon(R)	E5-4627V4	948865	Intel® Xeon® Processor E5-4627 v4 (25M Cache, 2.60 GHz) FC-LGA14A, Tray	

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1272	14nm	BROADWELL	INTEL(R)XEON(R)	E7-8891V4	948869		Intel® Xeon® Processor E7-8891 v4 (60M Cache, 2.80 GHz) FC-LGA144, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E7-8893V4	948871		Intel® Xeon® Processor E7-8893 v4 (60M Cache, 3.20 GHz) FC-LGA144, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E7-8890V4	948872		Intel® Xeon® Processor E7-8890 v4 (60M Cache, 2.20 GHz) FC-LGA144, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E7-8890V4	948873		Intel® Xeon® Processor E7-8890 v4 (60M Cache, 2.20 GHz) FC-LGA144, Tray
1273	14nm	APOLLO LAKE	INTEL(R)PENTIUM®	N4200	948985		Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2630V4	949003		Boxed Intel® Xeon® Processor E5-2630 v4 (25M Cache, 2.20 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2640V4	949004		Boxed Intel® Xeon® Processor E5-2640 v4 (25M Cache, 2.40 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON®	E5-2603V4	949005		Boxed Intel® Xeon® Processor E5-2603 v4 (15M Cache, 1.70 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2609V4	949006		Boxed Intel® Xeon® Processor E5-2609 v4 (20M Cache, 1.70 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-1620V4	949007		Boxed Intel® Xeon® Processor E5-1620 v4 (10M Cache, 3.50 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6850K	949174		Intel® Core™ i7-6850K Processor (15M Cache, up to 3.80 GHz) FC-LGA144, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6800K	949175		Intel® Core™ i7-6800K Processor (15M Cache, up to 3.60 GHz) FC-LGA144, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2689V4	949319		Intel® Xeon® Processor E5-2689 v4 (25M Cache, 3.10 GHz) FC-LGA144, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	N/A	949356		SRV [KNIGHTS LANDING] Processor 1.50 GHz, 36M Cache, FC-LGA14B, Tray, 230W, H18066702974700
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	N/A	949367		SRV [KNIGHTS LANDING] Processor 1.30 GHz, 32M Cache, FC-LGA14B, Tray, 230W, H18066702975000
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400	949415		Intel® Core™ i5-7400 Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2620V4	949499		Boxed Intel® Xeon® Processor E5-2620 v4 (20M Cache, 2.10 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2630V4	949500		Boxed Intel® Xeon® Processor E5-2630 v4 (25M Cache, 2.20 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-2699CV4	949756		Intel® Xeon® Processor E5-2699C v4 (55M Cache, 2.20 GHz) FC-LGA144, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100	949784		Intel® Core™ i3-7100 Processor (3M Cache, 3.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R)PENTIUM(R)	G4600	949788		Intel® Pentium® Processor G4600 (3M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930	949799		Intel® Celeron® Processor G3930 (2M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100T	949805		Intel® Core™ i3-7100T Processor (3M Cache, 3.40 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R)PENTIUM(R)	G4600T	949807		Intel® Pentium® Processor G4600T (3M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930T	949811		Intel® Celeron® Processor G3930T (2M Cache, 2.70 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R)XEON(R)	E3-1578LV5	949901		Intel® Xeon® Processor E3-1578L v5 (8M Cache, 2.00 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R)XEON(R)	E3-1558LV5	949904		Intel® Xeon® Processor E3-1558L v5 (8M Cache, 1.90 GHz) FC-BGA14F, Tray
1273	14nm	APOLLO LAKE	INTEL(R)ATOM(TM)	E3900	950313		Intel Atom® Processor E3900 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R)ATOM(TM)	E3900	950318		Intel Atom® Processor E3900 (2M Cache, up to 2.40 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R)ATOM(TM)	E3900	950321		Intel Atom® Processor E3900 (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R)ATOM(TM)	E3900	950325		Intel Atom® Processor E3900 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	D-1526	950400		Intel® Xeon® Processor D-1526 (6M Cache, 1.80 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6950X	950624		Boxed Intel® Core™ i7-6950X Processor Extreme Edition (25M Cache, up to 3.50 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6900K	950625		Boxed Intel® Core™ i7-6900K Processor (20M Cache, up to 3.70 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6800K	950626		Boxed Intel® Core™ i7-6800K Processor (15M Cache, up to 3.80 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6800K	950627		Boxed Intel® Core™ i7-6800K Processor (15M Cache, up to 3.60 GHz) FC-LGA144
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6950X	950628		Boxed Intel® Core™ i7-6950X Processor Extreme Edition (25M Cache, up to 3.50 GHz) FC-LGA144, for China
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6900K	950629		Boxed Intel® Core™ i7-6900K Processor (20M Cache, up to 3.70 GHz) FC-LGA144, for China
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6850K	950630		Boxed Intel® Core™ i7-6850K Processor (15M Cache, up to 3.80 GHz) FC-LGA144, for China
1272	14nm	BROADWELL	INTEL (R) CORE (TM) I7	I7-6800K	950631		Boxed Intel® Core™ i7-6800K Processor (15M Cache, up to 3.60 GHz) FC-LGA144, for China
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I3	I3-6006U	950664		Intel® Core™ i3-6006U Processor (3M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R)XEON(R)	E5-1650V4	950795		Boxed Intel® Xeon® Processor E5-1650 v4 (15M Cache, 3.60 GHz) FC-LGA144
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	950936		Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7500U	950937		Intel® Core™ i7-7500U Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100U	950938		Intel® Core™ i3-7100U Processor (3M Cache, 2.40 GHz) FC-BGA14F, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7290	951260		Intel® Xeon Phi™ Processor 7290 (16GB, 1.50 GHz, 72 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7290F	951262		Intel® Xeon Phi™ Processor 7290F (16GB, 1.50 GHz, 72 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7250F	951264		Intel® Xeon Phi™ Processor 7250F (16GB, 1.40 GHz, 68 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7250	951266		Intel® Xeon Phi™ Processor 7250 (16GB, 1.40 GHz, 68 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7230F	951268		Intel® Xeon Phi™ Processor 7230F (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7230	951270		Intel® Xeon Phi™ Processor 7230 (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7210	951272		Intel® Xeon Phi™ Processor 7210 (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray

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1272	14nm	KNIGHTS LANDING	INTEL(R) XEON PHI(TM)	7210F	951274	INTEL® Xeon Phi™	Processor 7210F (16GB, 1.30 GHz, 64 core) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) i3	i3-6157U	951298	Intel® Core™ i3-6157U	Processor (3M Cache, 2.40 GHz) FC-BGA14C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3940	951358	Intel Atom®	Processor A3940 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3950	951366	Intel Atom®	Processor A3950 (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3930	951369	Intel Atom®	Processor A3930 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3960	951370	Intel Atom®	Processor A3960 (2M Cache, up to 2.40 GHz) FC-BGA15C, Tray
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3324	951429	Intel Atom®	Processor C3324 (4M Cache, up to 1.70) FC-BGA15Z, Tray
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3754	951434	Intel Atom®	Processor C3754 (16M Cache, up to 1.70) FC-BGA15Z, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1530	951482	Intel® Xeon®	Processor D-1530 (6M Cache, 2.40 GHz) FC-BGA14C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951483	Intel® Pentium®	Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951484	Intel® Celeron®	Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951485	Intel® Celeron®	Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	J3355	951489	Intel® Celeron®	Processor J3355 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	J3455	951490	Intel® Celeron®	Processor J3455 (2M Cache, up to 2.30 GHz) FC-BGA15F, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	P-8136	951549	Intel® Xeon®	Platinum P-8136 Processor (38.5M Cache, 2.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	P-8124	951607	Intel® Xeon®	Platinum P-8124 Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	P-8136	951616	Intel® Xeon®	Platinum P-8136 Processor (38.5M Cache, 2.00 GHz) FC-LGA14B, Tray
1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium®	Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron®	Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron®	Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	J3355	951841	Intel® Celeron®	Processor J3355 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	J4205	951842	Intel® Celeron®	Processor J4205 (2M Cache, up to 2.60 GHz) FC-BGA15F, Tray
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	J4205	951956	Intel® Pentium®	Processor J4205 (2M Cache, up to 2.60 GHz) FC-BGA15F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7775	951957	Intel® Core™ i7-7775	Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	i5-7200U	951957	Intel® Core™ i5-7200U	Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7500U	951958	Intel® Core™ i7-7500U	Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3	i3-7100U	951959	Intel® Core™ i3-7100U	Processor (3M Cache, 2.40 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) M	M3-7Y30	951961	Intel® Core™ m3-7Y30	Processor (4M Cache, up to 2.60 GHz) FC-BGA14F, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2699AV4	952190	Intel® Xeon®	Processor E5-2699A v4 (55M Cache, 2.40 GHz) FC-LGA14A, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	E5-2699RV4	952514	Intel® Xeon®	Processor E5-2699R v4 (55M Cache, 2.20 GHz) FC-LGA14A, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1280V6	952786	Intel® Xeon®	Processor E3-1280 v6 (8M Cache, 3.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1270V6	952787	Intel® Xeon®	Processor E3-1270 v6 (8M Cache, 3.80 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1240V6	952788	Intel® Xeon®	Processor E3-1240 v6 (8M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1230V6	952789	Intel® Xeon®	Processor E3-1230 v6 (8M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1220V6	952792	Intel® Xeon®	Processor E3-1220 v6 (8M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1275V6	952791	Intel® Xeon®	Processor E3-1275 v6 (8M Cache, 3.80 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1245V6	952792	Intel® Xeon®	Processor E3-1245 v6 (8M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1225V6	952793	Intel® Xeon®	Processor E3-1225 v6 (8M Cache, 3.30 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1205V6	952794	Intel® Xeon®	Processor E3-1205 v6 (8M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7600U	952861	Intel® Core™ i7-7600U	Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	i5-7300U	952866	Intel® Core™ i5-7300U	Processor (3M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3865U	952874	Intel® Celeron®	Processor 3865U (2M Cache, 1.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1505MV6	952949	Intel® Xeon®	Processor E3-1505M (8M Cache, 3.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1505MV6	952951	Intel® Xeon®	Processor E3-1505M (8M Cache, 3.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7920HQ	952952	Intel® Core™ i7-7920HQ	Processor (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7820HQ	952954	Intel® Core™ i7-7820HQ	Processor (8M Cache, up to 3.90 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7820HQ	952955	Intel® Core™ i7-7820HQ	Processor (8M Cache, up to 3.90 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	i7-7700HQ	952957	Intel® Core™ i7-7700HQ	Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	i5-7440HQ	952958	Intel® Core™ i5-7440HQ	Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	i5-7300HQ	952959	Intel® Core™ i5-7300HQ	Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3	i3-7100H	952960	Intel® Core™ i3-7100H	Processor (3M Cache, 3.00 GHz) FC-BGA14F, Tray

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1272	14nm	BROADWELL	INTEL(R)XEON(R)	E7-8894V4	952962	INTEL® Xeon® Processor E7-8894 v4 (60M Cache, 2.40 GHz) FC-LGA14A, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600K	952985	Intel® Core™ i5-7600K Processor (6M Cache, up to 4.20 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400	952986	Intel® Core™ i5-7400 Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4560	952994	Intel® Pentium® Processor G4560 (3M Cache, 3.50 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7101E	952995	Intel® Core™ i3-7101E Processor (3M Cache, 3.90 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400T	952998	Intel® Core™ i5-7400T Processor (6M Cache, up to 3.00 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600	953000	Intel® Core™ i5-7600 Processor (6M Cache, up to 4.10 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500	953001	Intel® Core™ i5-7500 Processor (6M Cache, up to 3.80 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600T	953002	Intel® Core™ i5-7600T Processor (6M Cache, up to 3.70 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500T	953003	Intel® Core™ i5-7500T Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700	953004	Intel® Core™ i7-7700 Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700T	953005	Intel® Core™ i7-7700T Processor (8M Cache, up to 3.80 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700K	953006	Intel® Core™ i7-7700K Processor (8M Cache, up to 4.50 GHz) FC-LGA14C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3940	953082	Intel Atom® Processor A3940 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	E3940	953083	Intel Atom® x5-E3940 Processor (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3950	953084	Intel Atom® Processor A3950 (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	E3950	953085	Intel Atom® x7-E3950 Processor (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	E3930	953086	Intel Atom® x5-E3930 Processor (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3930	953087	Intel Atom® Processor A3930 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3960	953096	Intel Atom® Processor A3960 (2M Cache, up to 2.40 GHz) FC-BGA15C, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7757	953348	Intel® Core™ i7-7757 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7Y57	953349	Intel® Core™ i5-7Y57 Processor (4M Cache, up to 3.30 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7600U	953350	Intel® Core™ i7-7600U Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7300U	953351	Intel® Core™ i5-7300U Processor (3M Cache, up to 3.50 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7500U	953352	Intel® Core™ i7-7500U Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100U	953354	Intel® Core™ i3-7100U Processor (3M Cache, 2.40 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7Y54	953356	Intel® Core™ i5-7Y54 Processor (4M Cache, up to 3.20 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) M	M3-7Y32	953357	Intel® Core™ m3-7Y32 Processor (4M Cache, up to 3.00 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) M	M3-7Y30	953358	Intel® Core™ m3-7Y30 Processor (4M Cache, up to 2.60 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	4415U	953359	Intel® Pentium® Processor 4415U (2M Cache, 2.30 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3865U	953360	Intel® Celeron® Processor 3865U (2M Cache, 1.80 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3965U	953361	Intel® Celeron® Processor 3965U (2M Cache, 2.20 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	4410Y	953362	Intel® Pentium® Processor 4410Y (2M Cache, 1.50 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700K	953654	Boxed Intel® Core™ i7-7700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700	953655	Boxed Intel® Core™ i7-7700K Processor (8M Cache, up to 4.20 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600K	953680	Boxed Intel® Core™ i5-7600K Processor (6M Cache, up to 4.20 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400	953681	Boxed Intel® Core™ i5-7400 Processor (6M Cache, up to 4.20 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600	953682	Boxed Intel® Core™ i5-7600 Processor (6M Cache, up to 3.50 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500	953683	Boxed Intel® Core™ i5-7500 Processor (6M Cache, up to 3.80 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600K	953700	Boxed Intel® Core™ i5-7600K Processor (6M Cache, up to 4.20 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400	953701	Boxed Intel® Core™ i5-7400 Processor (6M Cache, up to 3.50 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600	953702	Boxed Intel® Core™ i5-7600 Processor (6M Cache, up to 4.10 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500	953703	Boxed Intel® Core™ i5-7500 Processor (6M Cache, up to 3.80 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700	953712	Boxed Intel® Core™ i7-7700 Processor (8M Cache, up to 4.20 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700K	953713	Boxed Intel® Core™ i7-7700K Processor (8M Cache, up to 4.50 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINIUM	8124M	953855	Intel® Xeon® Platinum 8124M Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5117	953878	Intel® Xeon® Gold 5117 Processor (19.25M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7820EQ	953940	Intel® Core™ i7-7820EQ Processor (8M Cache, up to 3.70 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7440EQ	953941	Intel® Core™ i5-7440EQ Processor (6M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7442EQ	953942	Intel® Core™ i5-7442EQ Processor (6M Cache, up to 2.90 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100E	953943	Intel® Core™ i3-7100E Processor (3M Cache, 2.90 GHz) FC-BGA14F, Tray	

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1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7102E	953944	INTEL	Intel® Core™ i3-7102E Processor (3M Cache, 2.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1505LV6	953947	INTEL	Intel® Xeon® Processor E3-1505L v6 (8M Cache, 2.20 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7320	954022	INTEL	Intel® Core™ i3-7320 Processor (4M Cache, 4.10 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7300	954023	INTEL	Intel® Core™ i3-7300 Processor (4M Cache, 4.00 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7350K	954030	INTEL	Intel® Core™ i3-7350K Processor (4M Cache, 4.20 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100	954033	INTEL	Intel® Core™ i3-7100 Processor (3M Cache, 3.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4620	954035	INTEL	Intel® Pentium® Processor G4620 (3M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4600	954039	INTEL	Intel® Pentium® Processor G4600 (3M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3950	954042	INTEL	Intel® Celeron® Processor G3950 (2M Cache, 3.00 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930	954043	INTEL	Intel® Celeron® Processor G3930 (2M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7300T	954045	INTEL	Intel® Core™ i3-7300T Processor (4M Cache, 3.50 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100T	954047	INTEL	Intel® Core™ i3-7100T Processor (3M Cache, 3.40 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4600T	954049	INTEL	Intel® Pentium® Processor G4600T (3M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G4560T	954051	INTEL	Intel® Pentium® Processor G4560T (3M Cache, 2.70 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7287U	954104	INTEL	Intel® Core™ i5-7287U Processor (4M Cache, up to 3.70 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7167U	954106	INTEL	Intel® Core™ i3-7167U Processor (3M Cache, 2.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7267U	954107	INTEL	Intel® Core™ i5-7267U Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7260U	954110	INTEL	Intel® Core™ i5-7260U Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7560U	954111	INTEL	Intel® Core™ i7-7560U Processor (4M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7567U	954112	INTEL	Intel® Core™ i7-7567U Processor (4M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7660U	954113	INTEL	Intel® Core™ i7-7660U Processor (4M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3338	954194	INTEL	Intel Atom® Processor C3338 (4M Cache, up to 2.20 GHz) FC-BGA15C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400T	954219	Boxed Intel	Boxed Intel® Core™ i5-7400T Processor (6M Cache, up to 3.00 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600T	954220	Boxed Intel	Boxed Intel® Core™ i5-7600T Processor (6M Cache, up to 3.70 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500T	954221	Boxed Intel	Boxed Intel® Core™ i5-7500T Processor (6M Cache, up to 3.30 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700T	954222	Boxed Intel	Boxed Intel® Core™ i7-7700T Processor (8M Cache, up to 3.80 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7400T	954225	Boxed Intel	Boxed Intel® Core™ i5-7400T Processor (6M Cache, up to 3.00 GHz) FC-LGA14C, for China
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7600T	954227	Boxed Intel	Boxed Intel® Core™ i5-7600T Processor (6M Cache, up to 3.70 GHz) FC-LGA14C, for China
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7500T	954228	Boxed Intel	Boxed Intel® Core™ i5-7500T Processor (6M Cache, up to 3.30 GHz) FC-LGA14C, for China
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-7700T	954229	Boxed Intel	Boxed Intel® Core™ i7-7700T Processor (8M Cache, up to 3.80 GHz) FC-LGA14C, for China
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7300	954311	Boxed Intel	Boxed Intel® Core™ i3-7300 Processor (4M Cache, 4.00 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7100	954312	Boxed Intel	Boxed Intel® Core™ i3-7100 Processor (3M Cache, 3.90 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4560	954313	Boxed Intel	Boxed Intel® Pentium® Processor G4560 (3M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4600	954315	Boxed Intel	Boxed Intel® Pentium® Processor G4600 (3M Cache, 3.60 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1270V6	954318	Boxed Intel	Boxed Intel® Xeon® Processor E3-1270 v6 (8M Cache, 3.80 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1240V6	954319	Boxed Intel	Boxed Intel® Xeon® Processor E3-1240 v6 (8M Cache, 3.70 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1230V6	954320	Boxed Intel	Boxed Intel® Xeon® Processor E3-1230 v6 (8M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1275V6	954321	Boxed Intel	Boxed Intel® Xeon® Processor E3-1275 v6 (8M Cache, 3.80 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1245V6	954323	Boxed Intel	Boxed Intel® Xeon® Processor E3-1245 v6 (8M Cache, 3.70 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1220V6	954324	Boxed Intel	Boxed Intel® Xeon® Processor E3-1220 v6 (8M Cache, 3.00 GHz) FC-LGA14C
1272	14nm	KABY LAKE	INTEL(R)Xeon(R)	E3-1225V6	954325	Boxed Intel	Boxed Intel® Xeon® Processor E3-1225 v6 (8M Cache, 3.30 GHz) FC-LGA14C
1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	954360	INTEL	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON®	N3450	954361	INTEL	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	954362	INTEL	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3940	954396	INTEL	Intel Atom® Processor A3940 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3950	954399	INTEL	Intel Atom® Processor A3950 (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	E3950	954401	INTEL	Intel Atom® x7-E3950 Processor (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	E3930	954402	INTEL	Intel Atom® x5-E3930 Processor (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3930	954403	INTEL	Intel Atom® Processor A3930 (2M Cache, up to 1.80 GHz) FC-BGA15C, Tray
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3960	954404	INTEL	Intel Atom® Processor A3960 (2M Cache, up to 2.40 GHz) FC-BGA15C, Tray

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1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6126F	954691	Intel® Xeon® Gold 6126F Processor (19.25M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7320	954808	Boxed Intel® Core™ i3-7320 Processor (4M Cache, 4.10 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7300	954809	Boxed Intel® Core™ i3-7300 Processor (4M Cache, 4.00 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7350K	954810	Boxed Intel® Core™ i3-7350K Processor (4M Cache, 4.20 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7100	954811	Boxed Intel® Core™ i3-7100 Processor (3M Cache, 3.90 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4560	954812	Boxed Intel® Pentium® Processor G4560 (3M Cache, 3.50 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4620	954813	Boxed Intel® Pentium® Processor G4620 (3M Cache, 3.70 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4600	954814	Boxed Intel® Pentium® Processor G4600 (3M Cache, 3.60 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3950	954815	Boxed Intel® Celeron® Processor G3950 (2M Cache, 3.00 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930	954816	Boxed Intel® Celeron® Processor G3930 (2M Cache, 2.90 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	I3-7300	954817	Boxed Intel® Core™ i3-7300 Processor (4M Cache, 4.00 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7350K	954818	Boxed Intel® Core™ i3-7350K Processor (4M Cache, 4.20 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7100	954819	Boxed Intel® Core™ i3-7100 Processor (3M Cache, 3.90 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4560	954821	Boxed Intel® Pentium® Processor G4560 (3M Cache, 3.50 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	G4600	954822	Boxed Intel® Pentium® Processor G4600 (3M Cache, 3.60 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930	954823	Boxed Intel® Celeron® Processor G3930 (2M Cache, 2.90 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1285V6	955012	Intel® Xeon® Processor E3-1285 v6 (8M Cache, 4.10 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7101TE	955013	Intel® Core™ i3-7101TE Processor (3M Cache, 3.40 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8180	955028	Intel® Xeon® Platinum 8180 Processor (38.5M Cache, 2.50 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8176	955028	Intel® Xeon® Platinum 8176 Processor (38.5M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8170	955035	Intel® Xeon® Platinum 8170 Processor (35.75M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8168	955036	Intel® Xeon® Platinum 8168 Processor (33M Cache, 2.70 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6150	955037	Intel® Xeon® Gold 6150 Processor (24.75M Cache, 2.70 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8173M	955108	Intel® Xeon® Platinum 8173M Processor (38.5M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8124M	955109	Intel® Xeon® Platinum 8124M Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5117	955110	Intel® Xeon® Gold 5117 Processor (19.25M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8180M	955111	Intel® Xeon® Platinum 8180M Processor (38.5M Cache, 2.50 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8176M	955112	Intel® Xeon® Platinum 8176M Processor (38.5M Cache, 2.10 GHz) FC-LGA14B, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3958	955144	Intel Atom® Processor C3958 (16M Cache, up to 2.0 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3538	955146	Intel Atom® Processor C3538 (8M Cache, up to 2.10 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3750	955157	Intel Atom® Processor C3750 (16M Cache, up to 2.40 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3850	955159	Intel Atom® Processor C3850 (12M Cache, up to 2.40 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3558	955160	Intel Atom® Processor C3558 (8M Cache, up to 2.20 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3758	955161	Intel Atom® Processor C3758 (16M Cache, up to 2.20 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3858	955162	Intel Atom® Processor C3858 (12M Cache, up to 2.0 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3338	955163	Intel Atom® Processor C3338 (4M Cache, up to 2.20 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3808	955164	Intel Atom® Processor C3808 (12M Cache, up to 2.0 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3308	955165	Intel Atom® Processor C3308 (4M Cache, up to 2.10 GHz) FC-BGA15C, Tray	
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3708	955167	Intel Atom® Processor C3708 (16M Cache, up to 1.70 GHz) FC-BGA15C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930E	955177	Intel® Celeron® Processor G3930E (2M Cache, 2.90 GHz) FC-LGA14C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	G3930TE	955178	Intel® Celeron® Processor G3930TE (2M Cache, 2.70 GHz) FC-LGA14C, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8167M	955233	Intel® Xeon® Platinum 8167M Processor (35.75M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7300T	955324	Boxed Intel® Core™ i3-7300T Processor (4M Cache, 3.50 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7100T	955325	Boxed Intel® Core™ i3-7100T Processor (3M Cache, 3.40 GHz) FC-LGA14C	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7300T	955326	Boxed Intel® Core™ i3-7300T Processor (4M Cache, 3.50 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7100T	955327	Boxed Intel® Core™ i3-7100T Processor (3M Cache, 3.40 GHz) FC-LGA14C, for China	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8173M	955508	Intel® Xeon® Platinum 8173M Processor (38.5M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6150	955514	Intel® Xeon® Gold 6150 Processor (24.75M Cache, 2.70 GHz) FC-LGA14B, Tray	
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3754	955790	Intel Atom® Processor C3754 (16M Cache, up to 1.70) FC-BGA15Z, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6134	955887	Intel® Xeon® Gold 6134 Processor (24.75M Cache, 3.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6134M	955889	Intel® Xeon® Gold 6134M Processor (24.75M Cache, 3.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5122	955974	Intel® Xeon® Gold 5122 Processor (16.5M Cache, 3.60 GHz) FC-LGA14B, Tray	

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1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8156	955978	Intel® Xeon® Platinum 8156 Processor (16.5M Cache, 3.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6140	955989	Intel® Xeon® Gold 6140 Processor (24.75M Cache, 2.30 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6142	955993	Intel® Xeon® Gold 6142 Processor (22M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6140M	955996	Intel® Xeon® Gold 6140M Processor (24.75M Cache, 2.30 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8160	955998	Intel® Xeon® Platinum 8160 Processor (33M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	6142M	956000	Intel® Xeon® Gold 6142M Processor (22M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6136	956002	Intel® Xeon® Gold 6136 Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6126	956004	Intel® Xeon® Gold 6126 Processor (19.25M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6152	956006	Intel® Xeon® Gold 6152 Processor (30.25M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6138	956008	Intel® Xeon® Gold 6138 Processor (27.5M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6148	956010	Intel® Xeon® Gold 6148 Processor (27.5M Cache, 2.40 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8158	956012	Intel® Xeon® Platinum 8158 Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8160M	956014	Intel® Xeon® Platinum 8160M Processor (33M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6130	956018	Intel® Xeon® Gold 6130 Processor (22M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6130	956019	Intel® Xeon® Gold 6130 Processor (22M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8153	956021	Intel® Xeon® Platinum 8153 Processor (22M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8164	956023	Intel® Xeon® Platinum 8164 Processor (35.75M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8170M	956027	Intel® Xeon® Platinum 8170M Processor (35.75M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) XEON(R) PLATINUM	E3-1501LV6	956300	Intel® Xeon® Processor E3-1501LV6 (6M Cache, up to 2.90 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) XEON(R)	E3-1501MV6	956301	Intel® Xeon® Processor E3-1501MV6 (6M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	DENVERTON	INTEL(R) PROCESSOR	C3955	956392	Intel Atom® Processor C3955 (16M Cache, up to 2.40 GHz) FC-BGA15C, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7740X	957005	Intel® Core™ i7-7740X X-series Processor (8M Cache, up to 4.50 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7740X	957006	Intel® Core™ i7-7740X X-series Processor (8M Cache, up to 4.50 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7640X	957007	Intel® Core™ i5-7640X X-series Processor (6M Cache, up to 4.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4110	957188	Intel® Xeon® Silver 4110 Processor (11M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8175M	957279	Intel® Xeon® Platinum 8175M Processor (33M Cache, 2.50 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8163	957286	Intel® Xeon® Platinum 8163 Processor (33M Cache, 2.50 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6149	957292	Intel® Xeon® Gold 6149 Processor (22M Cache, 3.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6151	957296	Intel® Xeon® Gold 6151 Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6161	957297	Intel® Xeon® Gold 6161 Processor (30.25M Cache, 2.20 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	4415Y	957336	Intel® Pentium® Processor 4415Y (2M Cache, 1.60 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5115	957337	Intel® Xeon® Gold 5115 Processor (13.75M Cache, 2.40 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5120T	957338	Intel® Xeon® Gold 5120T Processor (19.25M Cache, 2.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5120	957339	Intel® Xeon® Gold 5120 Processor (19.25M Cache, 2.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5118	957341	Intel® Xeon® Gold 5118 Processor (16.5M Cache, 2.30 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3965Y	957364	Intel® Celeron® Processor 3965Y (2M Cache, 1.50 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4110	957416	Intel® Xeon® Silver 4110 Processor (11M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4108	957417	Intel® Xeon® Silver 4108 Processor (11M Cache, 1.80 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4114	957418	Intel® Xeon® Silver 4114 Processor (13.75M Cache, 2.20 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE	3106	957419	Intel® Xeon® Bronze 3106 Processor (11M Cache, 1.70 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE	3104	957420	Intel® Xeon® Bronze 3104 Processor (8.25M Cache, 1.70 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4112	957421	Intel® Xeon® Silver 4112 Processor (8.25M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4109T	957422	Intel® Xeon® Silver 4109T Processor (12M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4116	957661	Intel® Xeon® Silver 4116 Processor (16.5M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6132	958178	Intel® Xeon® Gold 6132 Processor (19.25M Cache, 2.60 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6128	958179	Intel® Xeon® Gold 6128 Processor (19.25M Cache, 3.40 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6154	958186	Intel® Xeon® Gold 6154 Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8160T	958187	Intel® Xeon® Platinum 8160T Processor (33M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6138T	958188	Intel® Xeon® Gold 6138T Processor (27.5M Cache, 2.00 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6130T	958189	Intel® Xeon® Gold 6130T Processor (22M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6126T	958190	Intel® Xeon® Gold 6126T Processor (19.25M Cache, 2.60 GHz) FC-LGA14B, Tray	

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1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6129	958220	Intel® Xeon®	Gold 6129 Processor (22M Cache, 2.30 GHz) FC-LGA14B, Tray
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3508	958405	Intel Atom®	Processor C3508 (8M Cache, up to 1.50 GHz) FC-BGA15C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7130U	958406	Intel® Core™	I3-7130U Processor (3M Cache, 2.70 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6130F	958465	Intel® Xeon®	Gold 6130F Processor (22M Cache, 2.10 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6126F	958466	Intel® Xeon®	Gold 6126F Processor (19.25M Cache, 2.60 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8160F	958468	Intel® Xeon®	Platinum 8160F Processor (33M Cache, 2.10 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6142F	958469	Intel® Xeon®	Gold 6142F Processor (22M Cache, 2.60 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6148F	958470	Intel® Xeon®	Gold 6148F Processor (27.5M Cache, 2.40 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6138F	958471	Intel® Xeon®	Gold 6138F Processor (27.5M Cache, 2.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5117F	958478	Intel® Xeon®	Gold 5117F Processor (19.25M Cache, 2.00 GHz) FC-LGA14B, Tray
1273	14nm	DENVERTON	INTEL(R) PROCESSOR	C3908	958484	Intel Atom®	Processor C3908 (16M Cache, up to 2.00 GHz) FC-BGA15C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1533N	958597	Intel® Xeon®	Processor D-1533N (9M Cache, 2.10 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1553N	958598	Intel® Xeon®	Processor D-1553N (12M Cache, 2.30 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1513N	958600	Intel® Xeon®	Processor D-1513N (6M Cache, 1.60 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1543N	958602	Intel® Xeon®	Processor D-1543N (12M Cache, 1.90 GHz) FC-BGA14C, Tray
1272	14nm	SKY MEADOW	INTEL(R) XEON(R)	N/A	958704	[Missing External Name]	CD8067303204102
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7900X	958960	Intel® Core™	I9-7900X X-series Processor (13.75M Cache, up to 4.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-7800X	958962	Intel® Core™	I7-7800X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I7	I7-7820X	958963	Intel® Core™	I7-7820X X-series Processor (11M Cache, up to 4.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8180	958969	Boxed Intel® Xeon®	Platinum 8180 Processor (38.5M Cache, 2.50 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8176	958970	Boxed Intel® Xeon®	Platinum 8176 Processor (38.5M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8170	958971	Boxed Intel® Xeon®	Platinum 8170 Processor (35.75M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8164	958973	Boxed Intel® Xeon®	Platinum 8164 Processor (35.75M Cache, 2.00 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6134	958974	Boxed Intel® Xeon®	Gold 6134 Processor (24.75M Cache, 3.20 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5122	958975	Boxed Intel® Xeon®	Gold 5122 Processor (16.5M Cache, 3.60 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6140	958976	Boxed Intel® Xeon®	Gold 6140 Processor (24.75M Cache, 2.30 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6142	958977	Boxed Intel® Xeon®	Gold 6142 Processor (22M Cache, 2.60 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6152	958978	Boxed Intel® Xeon®	Gold 6152 Processor (30.25M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6138	958979	Boxed Intel® Xeon®	Gold 6138 Processor (27.5M Cache, 2.00 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6148	958981	Boxed Intel® Xeon®	Gold 6148 Processor (27.5M Cache, 2.40 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6130	958982	Boxed Intel® Xeon®	Gold 6130 Processor (22M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	I5-8350U	959020	Intel® Core™	I5-8350U Processor (6M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1273	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	C3538	959047	Intel Atom®	Processor C3538 (8M Cache, up to 2.10 GHz) FC-BGA15C, Tray
1272	14nm	DENVERTON	INTEL(R) PROCESSOR	I3-8100	959053	Intel® Core™	I3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I3	I3-8100	959053	Intel® Core™	I3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	I7-8650U	959152	Intel® Core™	I7-8650U Processor (8M Cache, up to 4.20 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8350U	959155	Intel® Core™	I5-8350U Processor (6M Cache, up to 3.60 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-7740X	959157	Boxed Intel® Core™	I5-7640X X-series Processor (6M Cache, up to 4.50 GHz) FC-LGA14B
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7640X	959158	Boxed Intel® Core™	I5-7640X X-series Processor (6M Cache, up to 4.20 GHz) FC-LGA14B
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-7740X	959159	Boxed Intel® Core™	I7-7740X X-series Processor (8M Cache, up to 4.50 GHz) FC-LGA14B
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™	I5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7640X	959161	Intel® Core™	I5-7640X X-series Processor (6M Cache, up to 4.20 GHz) FC-LGA14B, for China
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959162	Intel® Core™	I5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-8550U	959163	Intel® Core™	I5-7640X X-series Processor (6M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	I7-8550U	959162	Intel® Core™	I7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™	I3-7020U Processor (3M Cache, 2.30 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2102	959167	Intel® Xeon®	W-2102 Processor (8.25M Cache, 2.90 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2104	959168	Intel® Xeon®	W-2104 Processor (8.25M Cache, 3.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2123	959169	Intel® Xeon®	W-2123 Processor (8.25M Cache, 3.60 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2140B	959170	Intel® Xeon®	W-2140B Processor (11M Cache, 3.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2133	959171	Intel® Xeon®	W-2133 Processor (8.25M Cache, 3.60 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2125	959172	Intel® Xeon®	W-2125 Processor (8.25M Cache, 4.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2135	959173	Intel® Xeon®	W-2135 Processor (8.25M Cache, 3.70 GHz) FC-LGA14B, Tray

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1272	14nm	SKYLAKE	INTEL(R)XEON(R)	W-2145	959175		Intel® Xeon® W-2145 Processor (11M Cache, 3.70 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)XEON(R)	W-2155	959176		Intel® Xeon® W-2155 Processor (13.75M Cache, 3.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)XEON(R)	W-2150B	959177		Intel® Xeon® W-2150B Processor (13.75M Cache, 3.00 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8171M	959466		Intel® Xeon® Platinum 8171M Processor (35.75M Cache, 2.60 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8151	959467		Intel® Xeon® Platinum 8151 Processor (24.75M Cache, 3.40 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6133	959468		Intel® Xeon® Gold 6133 Processor (27.5M Cache, 2.50 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6137	959470		Intel® Xeon® Gold 6137 Processor (24.75M Cache, 3.90 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6143	959474		Intel® Xeon® Gold 6143 Processor (22M Cache, 2.80 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8165	959475		Intel® Xeon® Platinum 8165 Processor (33M Cache, 2.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6146	959503		Intel® Xeon® Gold 6146 Processor (24.75M Cache, 3.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6144	959504		Intel® Xeon® Gold 6144 Processor (24.75M Cache, 3.50 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6144	959504		Intel® Xeon® Gold 6144 Processor (24.75M Cache, 3.50 GHz) FC-LGA14B, Tray
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3314	959594		EMB [DENVERTON] Processor C3314 1.20 GHz, 4M Cache, FC-BGA15Z, T&R, 9W, HW8076502693601
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3324	959595		EMB [DENVERTON] Processor C3324 1.70 GHz, 4M Cache, FC-BGA15Z, T&R, 10W, HW8076502693701
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8176F	959636		Intel® Xeon® Platinum 8176F Processor (38.5M Cache, 2.10 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5120	959684		Boxed Intel® Xeon® Gold 5120 Processor (19.25M Cache, 2.20 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4116	959685		Boxed Intel® Xeon® Silver 4116 Processor (16.5M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4114T	959707		Intel® Xeon® Silver 4114T Processor (13.75M Cache, 2.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE	3106	959761		Boxed Intel® Xeon® Bronze 3106 Processor (11M Cache, 1.70 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE	3104	959762		Boxed Intel® Xeon® Bronze 3104 Processor (8.25M Cache, 1.70 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4110	959763		Boxed Intel® Xeon® Silver 4110 Processor (11M Cache, 2.10 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4108	959764		Boxed Intel® Xeon® Silver 4108 Processor (11M Cache, 1.80 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4114	959765		Boxed Intel® Xeon® Silver 4114 Processor (13.75M Cache, 2.20 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6128	959766		Boxed Intel® Xeon® Gold 6128 Processor (19.25M Cache, 2.60 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	5119T	959780		Boxed Intel® Xeon® Gold 5119T Processor (19.25M Cache, 1.90 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6127M	959783		Intel® Xeon® Gold 6127M Processor (22M Cache, 2.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4116T	959790		Intel® Xeon® Silver 4116T Processor (16.5M Cache, 2.10 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-7900X	959986		Boxed Intel® Core™ i9-7900X X-series Processor (13.75M Cache, up to 4.30 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-7800X	959987		Boxed Intel® Core™ i7-7800X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-7820X	959988		Boxed Intel® Core™ i7-7820X X-series Processor (11M Cache, up to 4.30 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-7900X	959989		Boxed Intel® Core™ i9-7900X X-series Processor (13.75M Cache, up to 4.30 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-7800X	959991		Boxed Intel® Core™ i7-7800X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-7820X	959993		Boxed Intel® Core™ i7-7820X X-series Processor (11M Cache, up to 4.30 GHz) FC-LGA14B, for China
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	17-8700	960006		Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	17-8700	960011		Intel® Core™ i3-8350K Processor (8M Cache, 4.00 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	13-8100	960012		Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	13-7020U	960019		Intel® Core™ i3-7020U Processor (3M Cache, 2.30 GHz) FC-LGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-7920X	960064		Intel® Core™ i9-7920X X-series Processor (16.5M Cache, up to 4.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-8000X	960065		Intel® Core™ i7-8000X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	17-8700K	960617		Intel® Core™ i7-8700K Processor (12M Cache, up to 4.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	17-8700	960618		Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8400	960619		Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8600K	960620		Intel® Core™ i5-8600K Processor (9M Cache, up to 4.30 GHz) FC-LGA14C, Tray
1272	14nm	STRIKE RIDGE	INTEL(R) XEON PHI(TM)		960869		SRV [STRIKE RIDGE] Processor 2.20 GHz, 2M Cache, FC-LGA14B, Tray, 300W, HI8069303810101
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	13-8350K	961059		Boxed Intel® Core™ i3-8350K Processor (8M Cache, 4.00 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	13-8100	961060		Boxed Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	13-8350K	961083		Boxed Intel® Core™ i3-8350K Processor (8M Cache, 4.00 GHz) FC-LGA14C, for China
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	13-8100	961084		Boxed Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, for China
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	17-8706G	961153		Intel® Core™ i7-8706G Processor with Radeon™ RX Vega M GL graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	17-8705G	961154		Intel® Core™ i7-8705G Processor with Radeon™ RX Vega M GL graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8305G	961161		Intel® Core™ i5-8305G Processor with Radeon™ RX Vega M GL graphics (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	17-8709G	961162		Intel® Core™ i7-8709G Processor with Radeon™ RX Vega M GH graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray

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1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7920X	961170		Boxed Intel® Core™ i9-7920X X-series Processor (16.5M Cache, up to 4.30 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7920X	961171		Boxed Intel® Core™ i9-7920X X-series Processor (16.5M Cache, up to 4.30 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7940X	961191		Intel® Core™ i9-7940X X-series Processor (19.25M Cache, up to 4.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7960X	961201		Intel® Core™ i9-7960X X-series Processor (22M Cache, up to 4.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7980XE	961202		Intel® Core™ i9-7980XE Extreme Edition Processor (24.75M Cache, up to 4.20 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2191B	961299		Intel® Xeon® W-2191B Processor (24.75M Cache, 2.30 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2195	961300		Intel® Xeon® W-2195 Processor (24.75M Cache, 2.30 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700K	961566		Boxed Intel® Core™ i7-8700K Processor (12M Cache, up to 4.70 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700	961567		Boxed Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400	961568		Boxed Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600K	961570		Boxed Intel® Core™ i5-8600K Processor (9M Cache, up to 4.30 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700K	961573		Boxed Intel® Core™ i7-8700K Processor (12M Cache, up to 4.70 GHz) FC-LGA14C, for China
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700	961574		Boxed Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, for China
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400	961575		Boxed Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C, for China
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600K	961576		Boxed Intel® Core™ i5-8600K Processor (9M Cache, up to 4.30 GHz) FC-LGA14C, for China
1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638		Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639		Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640		Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	J5005	961642		Intel® Pentium® Silver J5005 Processor (4M Cache, up to 2.80 GHz) FC-BGA15F, Tray
1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	J4105	961643		Intel® Celeron® J4105 Processor (4M Cache, up to 2.50 GHz) FC-BGA15F, Tray
1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	J4005	961644		Intel® Celeron® J4005 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2123	961844		Boxed Intel® Xeon™ W-2123 Processor (8.25M Cache, 3.60 GHz) FC-LGA14B
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-7020U	961968		Intel® Core™ i3-7020U Processor (3M Cache, 2.30 GHz) FC-LGA14F, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-7800X	962010		Boxed Intel® Core™ i7-7800X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	I7-7800X	962011		Boxed Intel® Core™ i7-7800X X-series Processor (8.25M Cache, up to 4.00 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6144	962201		Intel® Xeon® Gold 6144 Processor (24.75M Cache, 3.50 GHz) FC-LGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2135	962353		Boxed Intel® Xeon™ W-2135 Processor (8.25M Cache, 3.70 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7940X	962502		Boxed Intel® Core™ i9-7940X Processor (19.25M Cache, up to 4.30 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7960X	962502		Boxed Intel® Core™ i9-7960X Processor (22M Cache, up to 4.20 GHz) FC-LGA14B
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7940X	962506		Boxed Intel® Core™ i9-7940X Processor (19.25M Cache, up to 4.30 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7960X	962507		Boxed Intel® Core™ i9-7960X Processor (22M Cache, up to 4.20 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7980XE	962508		Boxed Intel® Core™ i9-7980XE Extreme Edition Processor (24.75M Cache, up to 4.20 GHz) FC-LGA14B, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	I9-7980XE	962509		Boxed Intel® Core™ i9-7980XE Extreme Edition Processor (24.75M Cache, up to 4.20 GHz) FC-LGA14B
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3754	962679		Intel® Atom™ Processor C3754 (16M Cache, 1.70 GHz) FC-BGA15Z, Tray
1272	14nm	KNIGHTS MILL	INTEL(R) XEON PHI(TM)	7295	962788		Intel® Xeon Phi™ Processor 7295 (16GB, 1.5 GHz, 72 Core) FC-LGA14B, Tray
1272	14nm	KNIGHTS MILL	INTEL(R) XEON PHI(TM)	7285	962808		Intel® Xeon Phi™ Processor 7285 (16GB, 1.3 GHz, 68 Core) FC-LGA14B, Tray
1272	14nm	KNIGHTS MILL	INTEL(R) XEON PHI(TM)	7235	962809		Intel® Xeon Phi™ Processor 7235 (16GB, 1.3 GHz, 64 Core) FC-LGA14B, Tray
1272	14nm	KNIGHTS MILL	INTEL(R) XEON PHI(TM)	7255	962810		Intel® Xeon Phi™ Processor 7255 (16GB, 1.1 GHz, 68 Core) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5400	962838		Intel® Pentium® Gold G5400 Processor (4M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500	962883		Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER	4123	963002		Intel® Xeon® Silver 4123 Processor (11M Cache, 3.00 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	N/A	I5-8300H	963136		Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I3	I3-8130U	963178		Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	W-2175	963214		Intel® Xeon™ W-2175 Processor (19.25M Cache, 2.50 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	W-2170B	963214		Intel® Xeon® Processor W-2170B (19.25M Cache, 2.50 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4900	963375		Intel® Celeron® Processor G4900 (2M Cache, 3.10 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2124G	963428		Intel® Xeon® E-2124G Processor (8M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2144G	963429		Intel® Xeon® E-2144G Processor (8M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2174G	963430		Intel® Xeon® E-2174G Processor (8M Cache, up to 4.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2134	963443		Intel® Xeon® E-2134 Processor (8M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2124	963447		Intel® Xeon® E-2124 Processor (8M Cache, up to 4.30 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2186G	963448		Intel® Xeon® E-2186G Processor (12M Cache, up to 4.70 GHz) FC-LGA14C, Tray

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1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2176G	963450		Intel® Xeon® E-2176G Processor (12M Cache, up to 4.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2146G	963454		Intel® Xeon® E-2146G Processor (12M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2126G	963464		Intel® Xeon® E-2126G Processor (12M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2104G	963465		Intel® Xeon® Processor E-2104G (8M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2136	963466		Intel® Xeon® E-2136 Processor (12M Cache, up to 4.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700T	963506		Intel® Core™ i7-8700T Processor (12M Cache, up to 4.00 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600	963534		Intel® Core™ i5-8600 Processor (9M Cache, up to 4.30 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600T	963537		Intel® Core™ i5-8600T Processor (9M Cache, up to 3.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400T	963540		Intel® Core™ i5-8400T Processor (9M Cache, up to 3.30 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	G5400	963543		Intel® Pentium® Gold G5400 Processor (4M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5400T	963566		Intel® Pentium® Gold G5400T Processor (4M Cache, 3.10 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500T	963592		Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500	963598		Intel® Core™ i5-8500 Processor (8M Cache, 3.70 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	I3-8300	963643		Intel® Core™ i3-8300 Processor (8M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	I3-8300T	963646		Intel® Core™ i3-8300T Processor (6M Cache, 3.10 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	I3-8100T	963660		Intel® Core™ i3-8100T Processor (6M Cache, 3.10 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5600	963663		Intel® Pentium® Gold G5600 Processor (4M Cache, 3.90 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5500	963670		Intel® Pentium® Gold G5500 Processor (4M Cache, 3.80 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5500T	963678		Intel® Pentium® Gold G5500T Processor (4M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4920	963694		Intel® Celeron® Processor G4920 (2M Cache, 3.20 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4900T	963697		Intel® Celeron® Processor G4900T (2M Cache, 2.90 GHz) FC-LGA14C, Tray
1272	14nm	COFFEE LAKE	INTEL(R)Xeon	E-2176M	963717		Intel® Xeon® E-2176M Processor (12M Cache, up to 4.40 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718		Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8850H	963719		Intel® Core™ i7-8850H Processor (9M Cache, up to 4.30 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720		Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400H	963721		Intel® Core™ i5-8400H Processor (8M Cache, up to 4.20 GHz) FC-BGA14F, Tray
1272	14nm	SKYLAKE	INTEL(R) Xeon(R) PLATINUM	8174	963757		Intel® Xeon® Platinum 8174 Processor (33M Cache, 3.10 GHz) FC-LGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4900	963823		Boxed Intel® Celeron® Processor G4900 (2M Cache, 3.10 GHz) FC-LGA14C, for China
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4900	963825		Boxed Intel® Celeron® Processor G4900 (2M Cache, 3.10 GHz) FC-LGA14C, for China
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2187NT	964082		Intel® Xeon® D-2187NT Processor (22M Cache, 2.00 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2161I	964083		Intel® Xeon® D-2161I Processor (16.5M Cache, 2.20 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2163IT	964084		Intel® Xeon® D-2163IT Processor (16.5M Cache, 2.10 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2183IT	964085		Intel® Xeon® D-2183IT Processor (22M Cache, 2.20 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2146NT	964087		Intel® Xeon® D-2146NT Processor (11M Cache, 2.30 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2173IT	964088		Intel® Xeon® D-2173IT Processor (19.25M Cache, 1.70 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2145NT	964089		Intel® Xeon® D-2145NT Processor (11M Cache, 1.90 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2143IT	964090		Intel® Xeon® D-2143IT Processor (11M Cache, 2.20 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2141I	964091		Intel® Xeon® D-2141I Processor (11M Cache, 2.20 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2123IT	964092		Intel® Xeon® D-2123IT Processor (8.25M Cache, 2.20 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2166NT	964093		Intel® Xeon® D-2166NT Processor (16.5M Cache, 2.00 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2177NT	964094		Intel® Xeon® D-2177NT Processor (19.25M Cache, 1.90 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2142IT	964095		Intel® Xeon® D-2142IT Processor (11M Cache, 1.90 GHz) FC-BGA14B, Tray
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2191	964672		Intel® Xeon® D-2191 Processor (24.75M Cache, 1.60 GHz) FC-BGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CELERON(R)	G4920	973459		Boxed Intel® Celeron® Processor G4920 (2M Cache, 3.20 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2176G	973773		Boxed Intel® Xeon® E-2176G Processor (12M Cache, 3.70 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL(R)Xeon(R)	E-2146G	974864		Boxed Intel® Xeon® E-2146G Processor (12M Cache, 3.50 GHz) FC-LGA14C
1272	14nm	SKYLAKE	INTEL(R)Xeon(R)	D-2191	974910		Intel® Xeon® D-2191 Processor (24.75M Cache, 1.60 GHz) FC-BGA14B, Tray
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8559U	974938		Intel® Core™ i7-8559U Processor (8M Cache, up to 4.50 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8269U	974943		Intel® Core™ i5-8269U Processor (6M Cache, up to 4.20 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600	974956		Boxed Intel® Core™ i5-8600 Processor (9M Cache, up to 4.30 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500	974957		Boxed Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	I3-8300	974959		Boxed Intel® Core™ i3-8300 Processor (8M Cache, 3.70 GHz) FC-LGA14C

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1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5600	974960	Boxed Intel® Pentium® Gold G5600 Processor (4M Cache, 3.90 GHz) FC-LGA14C	
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5500	974961	Boxed Intel® Pentium® Gold G5500 Processor (4M Cache, 3.80 GHz) FC-LGA14C	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	6162	974994	Intel® Xeon® Platinum 6162 Processor (33M Cache, 1.90 GHz) FC-LGA14B, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD	6122	974995	Intel® Xeon® Gold 6122 Processor (27.5M Cache, 1.80 GHz) FC-LGA14B, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	19-8950HK	975241	Intel® Core™ i9-8950HK Processor (12M Cache, up to 4.80 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2186M	975241	Intel® Xeon® E-2186M Processor (12M Cache, up to 4.80 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I3	I3-8109U	975758	Intel® Core™ i3-8109U Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8259U	975759	Intel® Core™ i5-8259U Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8600	975870	Boxed Intel® Core™ i5-8600 Processor (9M Cache, up to 4.30 GHz) FC-LGA14C, for China	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500	975871	Boxed Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, for China	
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5500	975872	Boxed Intel® Pentium® Gold G5500 Processor (4M Cache, 3.80 GHz) FC-LGA14C, for China	
1274	10nm	CANNON LAKE	INTEL (R) CORE (TM) I3	I3-8121U	975938	Intel® Core™ i3-8121U Processor (4M Cache, up to 3.20 GHz) FC-BGA16F, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R)	D-2191A	976094	Intel® Xeon® D-2191A Processor (24.75M Cache, 1.60 GHz) FC-BGA14B, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8700B	976523	Intel® Core™ i7-8700B Processor (12M Cache, up to 4.60 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500B	976526	Intel® Core™ i5-8500B Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400B	976531	Intel® Core™ i5-8400B Processor (9M Cache, up to 4.00 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5400	976952	Boxed Intel® Pentium® Gold G5400 Processor (4M Cache, 3.70 GHz) FC-LGA14C	
1272	14nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD	G5400	976953	Boxed Intel® Pentium® Gold G5400 Processor (4M Cache, 3.70 GHz) FC-LGA14C, for China	
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2124G	977233	Boxed Intel® Xeon® E-2124G Processor (8M Cache, 3.40 GHz) FC-LGA14C	
1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)	E-2134	977235	Boxed Intel® Xeon® E-2134 Processor (8M Cache, 3.50 GHz) FC-LGA14C	
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8700	977399	Boxed Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, includes Intel® Optane™ Memory (16GB)	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8400	977518	Boxed Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C, includes Intel® Optane™ Memory (16GB)	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8500	977519	Boxed Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, includes Intel® Optane™ Memory (16GB)	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-8706G	978295	Intel® Core™ i7-8706G Processor with Radeon™ Pro WX Vega M GL graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8086K	978581	Boxed Intel® Core™ i7-8086K Processor (12M Cache, up to 5.00 GHz) FC-LGA14C	
1273	14nm	DENVERTON	INTEL(R) ATOM(TM)	C3534	978654	[Missing External Name] FH82CM248	
1273	14nm	DENVERTON	INTEL (R) PROCESSOR	C3336	979019	Intel Atom™ Processor C3336 (4M Cache, 1.50 GHz) FC-BGA15C, Tray	
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-8086K	979349	Boxed Intel® Core™ i7-8086K Processor (12M Cache, up to 5.00 GHz) FC-LGA14C, for China	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8305G	979456	Intel® Core™ i5-8305G Processor with Radeon™ Pro WX Vega M GL graphics (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	MONTAGE(R) JINTIDE(R) C	C2460 1	980100	Montage® Jintide® C 2460 1 Processor (33M Cache, 2.10 GHz) FC-LGA14B, Tray	
1272	14nm	WHISKEY LAKE	N/A	I3-8145U	980656	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	WHISKEY LAKE	N/A	I3-8145U	980657	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM	8124M	980660	Intel® Xeon® Platinum 8124M Processor (24.75M Cache, 3.00 GHz) FC-LGA14B, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	I7-8500Y	980666	Intel® Core™ i7-8500Y Processor (4M Cache, up to 4.20 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8200Y	980667	Intel® Core™ i5-8200Y Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) M	M3-8100Y	980672	Intel® Core™ m3-8100Y Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray	
1272	14nm	KABY LAKE	INTEL (R) CORE (TM) M	M3-8100Y	980678	Intel® Core™ m3-8100Y Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I3	I3-8100B	981451	Intel® Core™ i3-8100B Processor (4M Cache, 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	WHISKEY LAKE	N/A	I7-8565U	982918	Intel® Core™ i7-8565U Processor (8M Cache, up to 4.60 GHz) FC-BGA14F, Tray	
1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982922	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	SKY MEADOW	INTEL(R) XEON®	N/A	982924	SRV [SKY MEADOW] Processor 2.00 GHz, 33M Cache, FC-LGA14B, Tray, 205W, CM8067303405604	
1272	14nm	SKY MEADOW	INTEL(R) XEON(R) GOLD	N/A	982925	SRV [SKY MEADOW] Processor 2.10 GHz, 22M Cache, FC-LGA14B, Tray, 180W, CM8067303409003	
1272	14nm	CASCADE LAKE	INTEL(R) XEON(R) PLATINUM	8263C	982995	Intel Atom™ Processor A3920 (2M Cache, up to 2.00 GHz) FC-BGA15C, Tray	
1272	14nm	CASCADE LAKE	INTEL(R) XEON(R) GOLD	6261	982997	Intel® Core™ i7-8510Y Processor (4M Cache, up to 4.30 GHz) FC-BGA14F, Tray	
1273	14nm	APOLLO LAKE	INTEL(R) ATOM(TM)	A3920	983175	Intel® Core™ i5-8310Y Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray	
1272	14nm	AMBER LAKE	INTEL (R) CORE (TM) I7	I7-8510Y	983287	Intel® Core™ i5-8310Y Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	AMBER LAKE	INTEL(R) CORE(TM) I5	I5-8310Y	983288	Intel® Core™ i5-8310Y Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	AMBER LAKE	INTEL(R) CORE(TM) I5	I5-8210Y	983289	Intel® Core™ i5-8210Y Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray	
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	I9-9900K	983354	Intel® Core™ i9-9900K Processor (16M Cache, up to 5.00 GHz) FC-LGA14A, Tray	
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	I7-9700K	983355	Intel® Core™ i7-9700K Processor (12M Cache, up to 4.90 GHz) FC-LGA14A, Tray	

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1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-9600K	983556		Intel® Core™ i5-9600K Processor (9M Cache, up to 4.60 GHz) FC-LGA14A, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	19-9900K	984503		Boxed Intel® Core™ i9-9900K Processor (16M Cache, up to 5.00 GHz) FC-LGA14A
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-9600K	984505		Boxed Intel® Core™ i5-9600K Processor (9M Cache, up to 4.60 GHz) FC-LGA14C
1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	17-9700K	984509		Boxed Intel® Core™ i7-9700K Processor (12M Cache, up to 4.90 GHz) FC-LGA14A, for China
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-9600K	984512		Boxed Intel® Core™ i5-9600K Processor (9M Cache, up to 4.60 GHz) FC-LGA14A, for China
1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	44117U	984527		Intel® Pentium® Processor 44117U (2M Cache, 2.30 GHz) FC-BGA14F, Tray
1272	14nm	WHISKEY LAKE	INTEL(R) PENTIUM(R)	5405U	984529		Intel® Pentium® Gold 5405U Processor (2M Cache, 2.30 GHz) FC-BGA14F, Tray
1272	14nm	WHISKEY LAKE	INTEL(R) CELERON(R)	4205U	984533		Intel® Celeron® Processor 4205U (2M Cache, 1.80 GHz) FC-BGA14F, Tray
1272	14nm	COFFEE LAKE	INTEL(R) CORE EVO(TM) I7	17-9700K	985083		Boxed Intel® Core™ i7-9700K Processor (12M Cache, up to 4.90 GHz) FC-LGA14A
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1573N	985835		Intel® Xeon® Processor D-1573N (12M Cache, 2.70 GHz) FC-BGA14C, Tray
1272	14nm	BROADWELL	INTEL(R) XEON(R)	D-1563N	985836		Intel® Xeon® Processor D-1563N (12M Cache, 2.00 GHz) FC-BGA14C, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9980X	986447		Intel® Core™ i9-9980X Extreme Edition Processor (24.75M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9960X	986448		Intel® Core™ i9-9960X X-series Processor (22M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9940X	986449		Intel® Core™ i9-9940X X-series Processor (19.25M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9920X	986450		Intel® Core™ i9-9920X X-series Processor (19.25M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9900X	986451		Intel® Core™ i9-9900X X-series Processor (19.25M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9820X	986452		Intel® Core™ i9-9820X X-series Processor (16.5M Cache, up to 4.20 GHz) FC-LGA14A, Tray
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-9800X	986453		Intel® Core™ i7-9800X X-series Processor (16.5M Cache, up to 4.50 GHz) FC-LGA14A, Tray
1272	14nm	CASCADE LAKE	INTEL(R) XEON(R) GOLD	6230	999C00		
1272	14nm	CASCADE LAKE	INTEL(R) XEON(R) GOLD	6248	999C09		
1272	14nm	CASCADE LAKE	INTEL(R) XEON(R) PLATINUM	8280L	999C16		
1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	19-9900K	999AGF		Boxed Intel® Core™ i9-9900K Processor (16M Cache, up to 5.00 GHz) FC-LGA14A, for China
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-9800X	999AC3		Boxed Intel® Core™ i7-9800X X-series Processor (16.5M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	17-9800X	999ACM		Boxed Intel® Core™ i7-9800X X-series Processor (16.5M Cache, up to 4.40 GHz) FC-LGA14A, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9820X	999AC8		Boxed Intel® Core™ i9-9820X X-series Processor (16.5M Cache, up to 4.10 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9900X	999AC1		Boxed Intel® Core™ i9-9900X X-series Processor (19.25M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9900X	999ACK		Boxed Intel® Core™ i9-9900X X-series Processor (19.25M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9920X	999AC6		Boxed Intel® Core™ i9-9920X X-series Processor (19.25M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9920X	999AC9		Boxed Intel® Core™ i9-9920X X-series Processor (19.25M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9940X	999ACG		Boxed Intel® Core™ i9-9940X X-series Processor (19.25M Cache, up to 4.40 GHz) FC-LGA14A, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9960X	999AC7		Boxed Intel® Core™ i9-9960X X-series Processor (22M Cache, up to 4.40 GHz) FC-LGA14A
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9960X	999ACF		Boxed Intel® Core™ i9-9960X X-series Processor (22M Cache, up to 4.40 GHz) FC-LGA14A, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9980X	999ACD		Boxed Intel® Core™ i9-9980X Processor Extreme Edition (24.75M Cache, up to 4.40 GHz) FC-LGA14A, for China
1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I9	19-9980X	999AD1		Boxed Intel® Core™ i9-9980X Processor Extreme Edition (24.75M Cache, up to 4.40 GHz) FC-LGA14A
1273	14nm	LEWISBURG	INTEL(R) C621	949752			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	N/A	951425			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	N/A	951591			[Missing External Name] EY82075PCH
1273	14nm	LEWISBURG	INTEL(R) C628	953061			Intel® C628 chipset (Intel® EY82C628 PCH)
1273	14nm	LEWISBURG	INTEL(R) C627	953062			Intel® C627 chipset (Intel® EY82C627 PCH)
1273	14nm	LEWISBURG	INTEL(R) C621	953098			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	INTEL(R) C621	953999			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	INTEL(R) C621	954859			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	INTEL(R) C628	954859			Intel® C628 chipset (Intel® EY82C628 PCH)
1273	14nm	LEWISBURG	INTEL(R) C627	954860			Intel® C627 chipset (Intel® EY82C627 PCH)
1273	14nm	LEWISBURG	INTEL(R) C626	954861			Intel® C626 chipset (Intel® EY82C626 PCH)
1273	14nm	LEWISBURG	INTEL(R) C625	954862			Intel® C625 chipset (Intel® EY82C625 PCH)
1273	14nm	LEWISBURG	INTEL(R) C622	954863			Intel® C622 chipset (Intel® EY82C622 PCH)
1273	14nm	LEWISBURG	INTEL(R) C624	954864			Intel® C624 chipset (Intel® EY82C624 PCH)
1273	14nm	LEWISBURG	INTEL(R) C621	957625			Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	INTEL(R) C628	957626			Intel® C628 chipset (Intel® EY82C628 PCH)

PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND	PROCESSOR#	MMID	INTEL	EXTERNAL PRODUCT MARKETING NAME
1273	14nm	LEWISBURG	INTEL(R) C627		957627		Intel® C627 chipset (Intel® EY82C627 PCH)
1273	14nm	LEWISBURG	INTEL(R) C626		957628		Intel® C626 chipset (Intel® EY82C626 PCH)
1273	14nm	LEWISBURG	INTEL(R) C625		957629		Intel® C625 chipset (Intel® EY82C625 PCH)
1273	14nm	LEWISBURG	INTEL(R) C622		957630		Intel® C622 chipset (Intel® EY82C622 PCH)
1273	14nm	LEWISBURG	INTEL(R) C621		957631		Intel® EY82C621 Platform Controller Hub
1273	14nm	LEWISBURG	INTEL(R) C624		957632		Intel® C624 chipset (Intel® EY82C624 PCH)
1273	14nm	CANNON LAKE	N/A		964246		Intel® FH82Q370 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964247		Intel® FH82H370 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964256		[Missing External Name] FH82Z390
1273	14nm	CANNON LAKE	N/A		964265		[Missing External Name] FH82H310
1273	14nm	CANNON LAKE	N/A		964268		Intel® FH82C246 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964269		Intel® FH82HM370 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964270		Intel® FH82C242 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964271		Intel® FH82QM370 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964272		Intel® FH82CM246 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		964273		Intel® FH82QMS380 Platform Controller Hub
1273	14nm	CANNON LAKE	N/A		978829		Intel® FH82H310 Platform Controller Hub
1275	10nm	SHUTTLE CREEK	N/A		951940		[Missing External Name] LUZONTCT1
1273	14nm	CHERRY TRAIL	INTEL (R) PROCESSOR	N/A	936018		CE [CHERRY TRAIL] Processor ULV 1.60 GHz, 2M Cache, FC-MB6T, Tray, N/AW, GB8066401885800
1273	14nm	CHERRY TRAIL	GENUINE INTEL (R) CPU	28700	940953		Intel Atom® x7-28700 Processor (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	28500	940954		Intel Atom® x5-28500 Processor (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3150	942230		Intel® Celeron® Processor N3150 (2M Cache, up to 2.08 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3050	942232		Intel® Celeron® Processor N3050 (2M Cache, up to 2.16 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)	N3700	942599		Intel® Pentium® Processor N3700 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3150	942600		Intel® Celeron® Processor N3150 (2M Cache, up to 2.08 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3050	942602		Intel® Celeron® Processor N3050 (2M Cache, up to 2.16 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3000	942603		Intel® Celeron® Processor N3000 (2M Cache, up to 2.08 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	GENUINE INTEL (R) CPU	28700	943102		Intel Atom® x7-28700 Processor (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	28300	943165		Intel Atom® x5-28300 Processor (2M Cache, up to 1.84 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)	N3700	943327		Intel® Pentium® Processor N3700 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3150	943328		Intel Atom® x5-28300 Processor (2M Cache, up to 1.84 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3050	943329		Intel® Celeron® Processor N3050 (2M Cache, up to 2.08 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	Z8100P	944058		Intel Atom® x5-28100P Processor (2M Cache, up to 1.04 GHz) FC-MB6T, T&R
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)		944573		Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	28500	944708		Intel Atom® x5-28500 Processor (2M Cache, up to 2.24 GHz) FC-BGA15F, T&R
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	944993		Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	J3060	944995		Intel® Celeron® Processor J3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	GENUINE INTEL (R) CPU	28750	945048		Intel Atom® x7-28750 Processor (2M Cache, up to 2.56 GHz) FC-BGA15F, Tray
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)		946849		Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA
1273	14nm	CHERRY TRAIL	GENUINE INTEL (R) CPU	28750	947016		Intel Atom® x7-28750 Processor (2M Cache, up to 2.56 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	28550	947017		Intel Atom® x5-28550 Processor (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)	N3710	947020		Intel® Pentium® Processor N3710 (2M Cache, up to 2.56 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3010	947021		Intel® Celeron® Processor N3010 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022		Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023		Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)	J3710	947024		Intel® Pentium® Processor J3710 (2M Cache, up to 2.64 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	J3060	947025		Intel® Celeron® Processor J3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	J3160	947026		Intel® Celeron® Processor J3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	Z8350	947027		Intel Atom® x5-28350 Processor (2M Cache, up to 1.92 GHz) FC-BGA15F, Tray
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)	Z8330	947028		Intel Atom® x5-28330 Processor (2M Cache, up to 1.92 GHz) FC-BGA15F, Tray
1273	14nm	BRASWELL	INTEL(R) ATOM(TM)	E8000	947286		Intel Atom® x5-E8000 Processor (2M Cache, up to 2.00 GHz) FC-BGA15F, Tray

PROCESS CODE		PROCESS NODE	ARCHITECTURE	BRAND	PROCESSOR#	MMID	INTEL	EXTERNAL PRODUCT MARKETING NAME
1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM)		Z8550	947827	INTEL® Atom™ Processor Z8550 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			947911	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			948716	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			949226	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			949336	Intel® Puma™ 7 SoC CE2712 DOCSIS3.1 Entry Level Networking GW	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			949870	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			949871	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			949874	Intel® Puma™ 7 SoC CE2712M DOCSIS3.1 Entry Level Networking GW with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			950572	Intel® Puma™ 7 SoC CE2712 DOCSIS3.1 Entry Level Networking GW	
1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060		951881	Intel® Celeron™ Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952283	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952322	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952331	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952346	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952347	Intel® Puma™ 7 SoC CE2712 DOCSIS3.1 Entry Level Networking GW	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952348	Intel® Puma™ 7 SoC CE2712M DOCSIS3.1 Entry Level Networking GW with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952485	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952487	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952488	Intel® Puma™ 7 SoC CE2712 DOCSIS3.1 Entry Level Networking GW	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952489	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952492	Intel® Puma™ 7 SoC CE2712M DOCSIS3.1 Entry Level Networking GW with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952555	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service) industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			952561	Intel® Puma™ 7 SoC CE2753 DOCSIS3.1 Enterprise Services industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961654	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961655	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961656	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961657	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961659	Intel® Puma™ 7 SoC CE2712M DOCSIS3.1 Entry Level Networking GW with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961661	Intel® Puma™ 7 SoC CE2712 DOCSIS3.1 Entry Level Networking GW	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961663	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961667	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service) industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961668	Intel® Puma™ 7 SoC CE2753 DOCSIS3.1 Enterprise Services industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			961669	Intel® Puma™ 7 SoC CE2753 DOCSIS3.1 Enterprise Services industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			962685	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			963196	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975635	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway with MOCA	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975636	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975639	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service)	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975641	Intel® Puma™ 7 SoC CE2703 DOCSIS3.1 Modem/eMTA (5Gbps service) industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975642	Intel® Puma™ 7 SoC CE2753 DOCSIS3.1 Enterprise Services industrial	
1273	14nm	COUGAR MOUNTAIN	INTEL(R) PUMA(TM)			975644	Intel® Puma™ 7 SoC CE2752 DOCSIS3.1 Services & All-IP Video Gateway	

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EXTERNAL PRODUCT MARKETING NAME

ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MIMID	EXTERNAL PRODUCT MARKETING NAME
N9.GWGWW.005	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
N9.GVGWW.007	ICN93450	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N8450	951833	Intel® Celeron® Processor N8450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
NX.VCYAA.001	C163300U	NOTEBOOK	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) i5	I5-6300U	954340	Intel® Core™ i5-6300U Processor (3M Cache, up to 3.00 GHz) FC-BGA14F, Tray
NX.GQAAA.005	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q2YAA.003	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.EFVWW.004	C18130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GULAA.001	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q2AAA.006	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GNAAA.001	C37100U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3	I3-7100U	953354	Intel® Core™ i3-7100U Processor (3M Cache, 2.40 GHz) FC-BGA14F, Tray
NX.G51AA.001	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NH.Q2BAA.003	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NH.Q2PAA.002	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GL2AA.001	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GV9AA.001	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NT.LDAAA.003	PQCN4200	WINDOWS TABLET-NB	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.G55AA.001	ICN3150	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3150	942600	Intel® Celeron® Processor N3150 (2M Cache, up to 2.08 GHz) FC-BGA15F, Tray
NX.GP6AA.001	CM9385U	NOTEBOOK	1272	14nm	SKYLAKE	INTEL(R) CELERON(R)	3855U	944335	Intel® Core™ i3-6066U Processor (3M Cache, 2.00 GHz) FC-BGA14C, Tray
N9.EFVWW.003	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.H05WW.003	CM9385U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	3865U	953360	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.GPAAA.012	C136006U	NOTEBOOK	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) i3	I3-6006U	950664	Intel® Core™ i3-6006U Processor (3M Cache, 2.00 GHz) FC-BGA14C, Tray
NX.GC7AA.001	ICN93160	NOTEBOOK	1272	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.GTAAA.008	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GNAAA.013	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-7200U	953354	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.GF5AA.004	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GSAAA.008	ICN93350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q2BAL.007	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GVHAL.001	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q2HAL.001	C178520U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959163	Intel® Core™ i5-8250U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.Q2RAL.014	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-7300HQ	952957	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NH.Q29AL.009	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GCJAA.009	ICN93160	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.GJAAA.004	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q2DAA.003	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GTAAA.012	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSAAA.004	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GDAAA.003	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GPTAA.004	ICN93450	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
NX.GQAAA.002	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GP8AA.005	C157300HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-7300HQ	952959	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NX.GHAAA.003	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	952959	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.GTCAA.002	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSAAA.001	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GTCAA.003	C178520U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.GXAAA.004	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.GTCAA.006	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSAAA.002	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GR7AA.004	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GR5AA.005	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.G4AAA.003	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.GTCAA.004	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSAAA.006	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GR7AA.002	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GR5AA.005	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.G4AAA.003	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.GPIAA.001	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.GM8AA.004	ICDN3060	NOTEBOOK	1273	14nm	SKYLAKE	INTEL(R) CORE(TM) i3	I3-6006U	944334	Intel® Core™ i3-6100U Processor (3M Cache, 2.30 GHz) FC-BGA14C, Tray
NT.GDAAA.006	C186100U	Windows Tablet-NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.GY0WW.001	C18250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q2AAA.001	C177700HQ	NOTEBOOK	1273	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GNTAA.005	ICDN3350	NOTEBOOK	1272	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.G55AA.018	ICN93160	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NH.Q2RAA.001	C157300HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5	I5-7300HQ	952959	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NX.SXAAA.006	ICN93450	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA14F, Tray
N9.H1WWW.001	C18130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q2AAA.003	ICDN3350	NOTEBOOK	1272	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q20AA.015	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray

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ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MMID	EXTERNAL PRODUCT MARKETING NAME
NH.Q28AA.005	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NH.LDSAA.001	C157200U/H22	Windows Tablet -NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NH.Q28AA.016	C157300HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-7300HQ	952959	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
N9.GUHWV.016	C17775/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
NX.G55AA.017	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.G55AA.019	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.G55AA.005	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.G59AA.004	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.G54AA.012	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.G54AA.016	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.G54AA.016	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.G2RAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q28AA.005	ICDN3450	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CORE(TM)15	N3450	951833	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
NX.SHXAA.005	ICDN3050	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3050	942600	Intel® Celeron® Processor N3050 (2M Cache, up to 2.16 GHz) FC-BGA15F, Tray
NX.G54AA.016	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
NX.G2RAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.G5YAA.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q28AA.002	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NX.GRYAA.001	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)13	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.G1EAA.003	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
N9.GUHWV.002	C17775/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
N9.G2AWV.002	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.GPAAA.002	C157300HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-7300HQ	952959	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NX.GPAAA.002	C157300HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-7300HQ	952959	Intel® Core™ i5-7300HQ Processor (6M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NH.LCDAA.003	ICDN3350	Windows Tablet -NB	1273	14nm	SKY LAKE	INTEL(R) CORE(TM)13	N3350	951834	Intel® Pentium® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GPAAA.001	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GU7AA.002	ICDN4100	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N4100	947023	Intel® Celeron® Processor N4100 (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GU4AA.001	C17775/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
NX.GU4AA.001	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Pentium® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GU4AA.010	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Pentium® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GP2AA.002	PQCN4200	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NH.Q3XAA.003	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
N9.Q3FWV.001	C178750U	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM)17	I7-8750H	963178	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
N9.H1LWV.003	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Pentium® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q2YAA.002	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.G2RAA.001	C18130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)13	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.G2RAA.006	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.GYAAA.001	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Pentium® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q2DAA.016	C156200U	Notebook	1272	14nm	SKY LAKE	INTEL(R) CORE(TM)15	I5-6200U	944338	Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
NH.Q2YAA.004	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.G55AA.010	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.G2AAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.VCGAA.037	ICDN3160	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 2.24 GHz) FC-BGA15F, Tray
N9.H8VWV.001	ICDN4100	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
N9.H8VWV.002	ICDN4000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
N9.H91VWV.002	ICDN4100	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
N9.H91VWV.001	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	980666	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA15F, Tray
N9.H9VWV.002	PQCN5000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
N9.H9VWV.003	PQCN5000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
NH.EFJAA.010	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
N9.H93VWV.002	ICDN4000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
N9.H93VWV.001	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	980666	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA15F, Tray
N9.H8VWV.002	PQCN5000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
N9.H9VWV.003	PQCN5000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
NH.EFJAA.010	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
N9.H8VWV.002	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)13	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.H8VWV.001	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)13	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.HAZVWV.001	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)13	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GY0AA.001	C178550U	Notebook	1273	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.VH5AA.002	ICDN4000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
N9.H98VWV.002	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)17	I7-8550U	980666	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.GW4AA.001	PQCN4200	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
N9.HAWVWV.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM)15	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray

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ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MMID	EXTERNAL PRODUCT MARKETING NAME
N9.H0WVW.004	PMD4417U	Notebook	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	4417U	984521	Intel® Pentium® Processor 4417U (2M Cache, 2.30 GHz) FC-BGA14F, Tray
N9.HDEWV.001	C158265U	Notebook	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
NH.Q3DAA.001	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NK.GVBA.001	PQCN4200	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NK.VHOAA.001	PQCN5000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
NX.VHRAA.001	ICDN4000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
NH.Q28AA.006	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7700HQ	952937	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NK.VDKAA.192	NX.GVBA.001	Notebook	1272	14nm	SKY LAKE	INTEL(R) CORE (TM) I5	15-8265U	944338	Intel® Core™ i5-8265U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
N9.HUWVW.002	C138145U	Notebook	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5	13-8145U	980656	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.GYVWV.001	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.Q11FAA.001	C177820HK	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8200HK	952955	Intel® Core™ i7-7820HK Processor (8M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.H69VW.001	C158265U	Notebook	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
NX.GTCAA.019	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.GRTAA.003	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NK.GSAAA.006	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NK.GVAAA.009	C156200U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-6200U	944338	Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
NX.VDKAA.196	C156200U	Notebook	1272	14nm	SKY LAKE	INTEL(R) CORE(TM) I5	15-6200U	944338	Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
NH.Q3VAA.011	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NK.GSUAL.003	C177500U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7500U	953352	Intel® Core™ i7-7500U Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NK.H7QAA.001	C158265U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	953352	Intel® Core™ i7-8550U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
NK.GP4AL.015	C177500U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7500U	953352	Intel® Core™ i7-7500U Processor (4M Cache, up to 3.50 GHz) FC-BGA14F, Tray
NX.H3UAA.001	C158265U	Notebook	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.H69VW.003	C178565U	Notebook	1272	14nm	WHISKEY LAKE	N/A	17-8565U	982918	Intel® Core™ i7-8565U Processor (8M Cache, up to 4.60 GHz) FC-BGA14F, Tray
NK.VGAAA.015	ICN31650	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron® Processor N3160 (2M Cache, up to 3.90 GHz) FC-BGA14F, Tray
NX.VCHAA.019	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NH.Q1VAA.002	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7700HQ	952937	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
N9.V8KWW.002	C178565U	Notebook	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982918	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.V9VWV.002	C158265U	Notebook	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.Q32VW.005	C178705G	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8705G	961154	Intel® Core™ i7-8705G Processor with Radeon™ RX Vega M GL graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NH.Q3FAA.001	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NT.LCZAA.003	ATM283350	Windows Tablet -NB	1273	14nm	CHERRY TRAIL	INTEL(R) ATOM(TM) I	28350	947027	Intel Atom™ X5-Z8350 Processor (2M Cache, up to 1.92 GHz) FC-BGA15F, Tray
NK.GZAAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.H04VW.001	C138145U	Notebook	1272	14nm	WHISKEY LAKE	N/A	13-8145U	980656	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz) FC-BGA14F, Tray
N9.V8KWW.003	C178565U	Notebook	1272	14nm	WHISKEY LAKE	N/A	17-8565U	982918	Intel® Core™ i7-8565U Processor (8M Cache, up to 4.60 GHz) FC-BGA14F, Tray
N9.Q32VW.003	C178705G	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8705G	961154	Intel® Core™ i7-8705G Processor with Radeon™ RX Vega M GL graphics (8M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NK.GP4AA.006	C157200U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.GP5AA.004	C157200U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.GTBA.001	C178750H	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NK.GRTAA.012	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GRTAA.013	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.GT0AA.002	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
N9.VJZVW.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NK.HODAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q3NAA.003	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.VG0AA.004	ICN3450	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
N9.VJCVW.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NK.HODAA.001	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.VJCVW.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.GXCAA.017	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NH.GXBA.003	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NK.GNAAA.002	ICN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
N9.GXVWV.001	CM3965U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3965U	953361	Intel® Celeron® Processor 3965U (2M Cache, 2.20 GHz) FC-BGA14F, Tray
N9.H0VWV.002	PQCN4200	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
N9.H0VWV.001	ICN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NK.GZAAA.002	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NK.GZAAA.020	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NK.GNAAA.017	C137100U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5	13-7100U	953354	Intel® Core™ i3-7100U Processor (3M Cache, 2.40 GHz) FC-BGA14F, Tray
NK.GNAAA.013	C157200U/H22	Notebook	1272	14nm	APOLLO LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
N9.H0KVV.002	ICN3450	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron® Processor N3450 (2M Cache, up to 2.20 GHz) FC-BGA15F, Tray
N9.H0KVV.003	ICN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q28AA.003	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7700HQ	952937	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NK.GHAAA.010	ICDN3060	Notebook	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
N9.EFVWV.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
N9.HFVWV.002	CM3865U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3865U	953360	Intel® Celeron® Processor 3865U (2M Cache, 1.80 GHz) FC-BGA14F, Tray
NK.GRTAA.008	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q32AA.001	C158300H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.Q3VAA.001	C158300H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray



ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	EXTERNAL PRODUCT MARKETING NAME	
								ACER	MMID
NX.H09AA.001	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz) FC-8GA15F, Tray
NX.G5FAA.003	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.GR4AL.008	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
N9.H1LWW.001	PQCN4200	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-8GA15F, Tray
N9.H10WW.002	ICDN3450	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron™ Processor N3450 (2M Cache, up to 2.20 GHz) FC-8GA15F, Tray
NX.GVZAA.003	ICDN4000	Notebook	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-8GA15F, Tray
NH.Q28AL.008	C177700HQ	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-8GA14F, Tray
NX.GTQAA.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.H0KAA.003	ICDN3450	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron™ Processor N3450 (2M Cache, up to 2.20 GHz) FC-8GA15F, Tray
NX.GNVAL.005	C157100U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	I3-7100U	953354	Intel® Core™ i3-7100U Processor (3M Cache, 2.40 GHz) FC-8GA14F, Tray
NX.GVAAA.002	C157200U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	I3-7200U	953353	Intel® Core™ i3-7200U Processor (3M Cache, up to 3.10 GHz) FC-8GA14F, Tray
NX.GR4AL.008	ICDN3350	Notebook	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz) FC-8GA15F, Tray
NX.GYVAL.002	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NH.GXBAL.001	C158300H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
N9.Q3PWW.001	C198950HK	Notebook	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I9	I9-8950HK	975241	Intel® Core™ i9-8950HK Processor (12M Cache, up to 4.80 GHz) FC-8GA14F, Tray
N9.VJ5WW.001	C158265U	Notebook	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
N9.Q53WW.001	C158300H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
N9.QSRWW.001	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.GZRAA.008	C138130U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.GTPAA.012	C178550U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NH.Q3ZAA.003	C158300H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NH.LO3AA.004	C178750H	Notebook	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.G51AA.003	C157200U/H22	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.H37AA.002	C158250U	Notebook	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
N9.Q4VWW.001	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
N9.H14WW.002	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
NX.GXAAA.002	PQCN5000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-8GA15F, Tray
NX.H4AAA.001	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
NX.H87AA.001	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
N9.V17WW.001	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
NX.GZAAA.001	PQCN5000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-8GA15F, Tray
NX.GZAAA.001	PQCN5000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-8GA15F, Tray
NX.H5CAL.002	C138145U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I3-8145U	980656	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz) FC-8GA14F, Tray
NX.H8AAA.001	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	I5-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz) FC-8GA14F, Tray
N9.Q4VWW.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
N9.Q4VWW.002	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.VFXAA.007	ICDN3450	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron™ Processor N3450 (2M Cache, up to 2.20 GHz) FC-8GA15F, Tray
NX.GYAL.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
N9.Q5BWW.001	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
N9.Q4VWW.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.VCGAA.006	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron™ Processor N3060 (2M Cache, up to 2.48 GHz) FC-8GA15F, Tray
NX.GR7AA.002	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.GNAAA.001	ICDN3060	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron™ Processor N3060 (2M Cache, up to 2.48 GHz) FC-8GA15F, Tray
NX.GVAAA.001	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz) FC-8GA15F, Tray
N9.Q35WW.001	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NH.Q5AAA.003	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NH.Q4VAA.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NH.LO3FAA.004	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NH.GXAAA.003	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NH.GXAAA.002	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NX.GR8AA.006	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NX.GRMAA.009	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-8GA15F, Tray
N9.Q4VWW.003	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.GTPAA.011	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-8GA14F, Tray
NX.VCSAA.002	C176500U	NOTEBOOK	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7	I7-6500U	944339	Intel® Core™ i7-6500U Processor (4M Cache, up to 3.10 GHz) FC-8GA14C, Tray
N9.Q4VWW.004	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NH.Q3ZAA.002	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NH.Q3FAA.005	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.G29AA.001	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-8GA14F, Tray
NX.GPTAA.001	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-8GA15F, Tray
N9.Q5FVW.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray
NX.GPTAA.002	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz) FC-8GA15F, Tray
N9.Q5DWW.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray

ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MMID	EXTERNAL PRODUCT MARKETING NAME	
									ACER	ACER
N9.05BWW.002	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
N9.HDRWW.001	C138145U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	13-8145U	980556	Intel® Core™ i3-8145U Processor (4M Cache, up to 3.90 GHz)	FC-8GA14F, Tray
C158265U	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	Intel® Core™ i5-8265U Processor (6M Cache, up to 3.90 GHz)	FC-8GA14F, Tray
N9.HEAWW.001	ICD4000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CORE (TM) I7	N4000	961640	Intel® Celeron™ N4000 Processor (4M Cache, up to 2.60 GHz)	FC-8GA15F, Tray
N9.GUHA.002	C17775/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz)	FC-8GA14F, Tray
NH.Q4AAL.003	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NH.Q4AAL.004	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NX.H15AA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GNPA.038	C137020UF	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, 2.30 GHz)	FC-8GA14F, Tray
NX.GR4L.006	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz)	FC-8GA15F, Tray
NX.GR5AL.002	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron™ Processor N3350 (2M Cache, up to 2.40 GHz)	FC-8GA15F, Tray
NX.H5TAA.004	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGTA.003	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGTA.004	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
N9.GZVW.001	PQCNS000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz)	FC-8GA15F, Tray
NX.VGTA.005	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGTA.006	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GUWAL.002	C136006U	NOTEBOOK	1272	14nm	SKY LAKE	INTEL(R) CORE (TM) I3	13-6006U	950664	Intel® Core™ i3-6006U Processor (3M Cache, 2.00 GHz)	FC-8GA14C, Tray
NX.VGUA.003	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGUA.004	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGUA.005	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.VGUA.006	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GC2AA.019	ICDN3160	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron™ Processor N3160 (2M Cache, up to 2.24 GHz)	FC-8GA15F, Tray
NX.GSFAA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GTAA.011	PQCNS4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz)	FC-8GA15F, Tray
NH.Q3NAA.005	C198950HK	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	19-8950HK	975241	Intel® Core™ i9-8950HK Processor (12M Cache, up to 4.80 GHz)	FC-8GA14F, Tray
NX.GNPA.002	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz)	FC-8GA14F, Tray
NX.GSFAA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H2AAL.001	ICDN9450	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3450	951833	Intel® Celeron™ Processor N3450 (2M Cache, up to 2.20 GHz)	FC-8GA15F, Tray
NH.Q2FAA.005	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NH.Q3FAA.006	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NH.Q3DAA.002	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NX.GXAA.003	PQCNS000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz)	FC-8GA15F, Tray
NX.G3AA.003	PQCNS3710	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)	N3710	947020	Intel® Pentium® Processor N3710 (2M Cache, up to 2.56 GHz)	FC-8GA15F, Tray
NX.GTAA.004	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NX.H2AL.002	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NH.Q4AAL.007	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NX.H15AA.002	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.G5AA.007	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H37AA.001	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.G5AA.006	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H20AA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NH.Q2KAL.002	C177700HQ	NOTEBOOK	1273	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz)	FC-8GA14F, Tray
NX.GC2AA.021	ICDN9160	NOTEBOOK	1273	14nm	BRASWELL	INTEL(R) CELERON(R)	N3160	947023	Intel® Celeron™ Processor N3160 (2M Cache, up to 2.24 GHz)	FC-8GA15F, Tray
N9.GZCWW.001	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NH.Q2LAA.002	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz)	FC-8GA14F, Tray
NX.H2MAL.006	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H2MAL.005	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NH.Q3NAA.007	C198950HK	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	19-8950HK	975241	Intel® Core™ i9-8950HK Processor (12M Cache, up to 4.80 GHz)	FC-8GA14F, Tray
NX.GYDAL.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GTAA.003	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	17-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NH.GXBAL.002	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NT.LDSAL.003	C157200U/H22	WINDOWS TABLET-NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	933353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz)	FC-8GA14F, Tray
NH.Q4DAA.001	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz)	FC-8GA14F, Tray
NX.GTAA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NH.Q3MAA.006	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NX.GYAA.002	C138130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	13-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GTAA.013	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.G2AA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GYAA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NH.GXAA.003	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NH.Q3ZAA.005	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NH.Q3ZAA.006	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	17-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz)	FC-8GA14F, Tray
NX.H2AL.003	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H2AL.004	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959163	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.H37AA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
NX.GXAA.005	PQCNS000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz)	FC-8GA15F, Tray
C158250U	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray
C158250U	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz)	FC-8GA14F, Tray

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EXTERNAL PRODUCT MARKETING NAME

ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	M/MID	EXTERNAL PRODUCT MARKETING NAME
NX.GPTAA.002	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.GP0AA.001	ICDN3350	NOTEBOOK	1272	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.VGTRAA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSFAA.005	C158250U	NOTEBOOK	1273	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.G3AAA.005	ICDN3060	NOTEBOOK	1273	14nm	BRAWELL	INTEL(R) CELERON(R)	N3060	947022	Intel® Celeron® Processor N3060 (2M Cache, up to 2.48 GHz) FC-BGA15F, Tray
NX.H0UAA.005	ICDN4000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
NH.GT0AA.003	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GSAAA.010	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GVZAA.006	ICDN4000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4000	961640	Intel® Celeron® N4000 Processor (4M Cache, up to 2.60 GHz) FC-BGA15F, Tray
NH.GXCAA.004	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NH.Q3FAA.007	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NH.Q2AAA.001	C177700HQ	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	I7-7700HQ	952957	Intel® Core™ i7-7700HQ Processor (6M Cache, up to 3.80 GHz) FC-BGA14F, Tray
NH.VGAAA.011	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.VGAAA.012	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NT.LDAAA.002	C157200U/H22	WINDOW5 TABLET-NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NH.Q4HAA.001	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.GRMAA.011	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NH.GXDA.004	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
C158300H	C158300H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	I5-8300H	963720	Intel® Core™ i5-8300H Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.Q3YAA.006	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.VGAAA.002	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.VGAAA.003	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H1WAA.002	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GTCAA.023	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NX.VHJAA.004	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.Q4HAA.005	C178550U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5	I7-8550U	959163	Intel® Core™ i7-8550U Processor (8M Cache, up to 4.00 GHz) FC-BGA14F, Tray
NH.Q3YAA.006	C178750H	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.H1WAA.003	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.VVWAA.002	ICDN4100	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GWSAA.001	ICDN4100	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GVAAA.005	ICDN4100	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	N4100	961639	Intel® Celeron® N4100 Processor (4M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.H37AA.001	C158130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H40AA.002	C158130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H47AA.002	C158130U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.H77AA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NH.H0AAA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GVZAA.007	PQCN5000	NOTEBOOK	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	Intel® Pentium® Silver N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray
NX.G53AA.007	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.G68AA.003	C156200U	NOTEBOOK	1273	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	I5-6200U	944338	Intel® Core™ i5-6200U Processor (3M Cache, up to 2.80 GHz) FC-BGA14C, Tray
NX.GNSAL.003	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GNSALO.015	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GTGH.013	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.GTGH.017	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NX.H2BAL.005	C137020UF	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H2BAL.007	C137020UF	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H2BAL.006	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NX.H2PAL.005	C137020UF	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NH.Q3FAL.007	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NH.Q4HAL.008	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.H15AL.003	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GUWAL.009	C137020UF	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3	I3-7020U	959164	Intel® Core™ i3-7020U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
N9.GUMWWW.004	ICDN3350	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)	N3350	951834	Intel® Celeron® Processor N3350 (2M Cache, up to 2.40 GHz) FC-BGA15F, Tray
NH.Q3NAL.008	C178750H	NOTEBOOK	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	I7-8750H	963718	Intel® Core™ i7-8750H Processor (9M Cache, up to 4.10 GHz) FC-BGA14F, Tray
NX.GJRAA.010	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H5UAA.001	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H5UAA.002	C158265U	NOTEBOOK	1272	14nm	WHISKEY LAKE	INTEL(R) CORE (TM) I3	I3-8130U	963178	Intel® Core™ i3-8130U Processor (4M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GZRAA.011	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GY1AA.001	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.H37AA.006	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.GZAA.011	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-8250U	959160	Intel® Core™ i5-8250U Processor (6M Cache, up to 3.40 GHz) FC-BGA14F, Tray
NX.G3855U	C158250U	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	3855U	944335	Intel® Celeron® Processor 3855U (2M Cache, 1.60 GHz) FC-BGA14C, Tray
NX.GJRAA.001	C17775/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7	I7-7775	953348	Intel® Core™ i7-7775 Processor (4M Cache, up to 3.60 GHz) FC-BGA14F, Tray
NX.H2AAA.001	C157200U/H22	NOTEBOOK	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
N9.GWGWV.008	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.GWAAA.002	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NX.GWAAA.003	PQCN4200	NOTEBOOK	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray
NT.LDAAA.003	C157200U/H22	WINDOW5 TABLET-NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	I5-7200U	953353	Intel® Core™ i5-7200U Processor (3M Cache, up to 3.10 GHz) FC-BGA14F, Tray
NT.LDAAA.004	PQCN4200	WINDOW5 TABLET-NB	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	Intel® Pentium® Processor N4200 (2M Cache, up to 2.50 GHz) FC-BGA15F, Tray

ACER										EXTERNAL PRODUCT MARKETING NAME
ITEM NUMBER	CPU	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MIMID	PROCESSOR#	PROCESSOR	EXTERNAL PRODUCT MARKETING NAME
NX.H60AA.001	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.H62AA.001	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.H22AA.002	C157200U/H22	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	15-7200U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.10 GHz) FC-8GA14F, Tray	
NX.VGAA.000	C158265U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	15-8500U	959163	15-8500U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.00 GHz) FC-8GA14F, Tray	
NX.VGAA.009	PQCIN5000	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	N5000	INTEL(R) SILVER N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray	
NH.GXAA.005	C178750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8750H	963718	17-8750H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NH.Q3WAL.007	C178750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8750H	963718	17-8750H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NH.H0AAA.006	PQCIN5000	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	N5000	INTEL(R) SILVER N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray	
NH.Q3DAL.009	C178750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8750H	963718	17-8750H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NH.GXAA.006	C178750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8750H	963718	17-8750H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.H0AAA.001	PQCIN5000	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	N5000	961638	N5000	INTEL(R) SILVER N5000 Processor (4M Cache, up to 2.70 GHz) FC-BGA15F, Tray	
NX.H1AAA.001	PQCIN4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	N4200	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.H3WAA.001	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.GTAAA.025	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.GTAAA.025	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.EFAA.004	C188130U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	18-8130U	963178	18-8130U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.10 GHz) FC-8GA14F, Tray	
NX.H3JAA.002	C178565U	1272	14nm	WHISKEY LAKE	N/A	17-8565U	982921	17-8565U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA14F, Tray	
NX.H3WAA.001	C158265U	1272	14nm	WHISKEY LAKE	INTEL(R) PENTIUM(R)	N4200	951830	N4200	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA14F, Tray	
NX.GRWAA.004	PQCIN4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	N4200	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA14F, Tray	
NX.H10AA.001	ICDN3350	1273	14nm	WHISKEY LAKE	INTEL(R) CELEBRON(R)	N3350	951834	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.H8AAA.003	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.H2AAA.002	ICDN3160	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3160	947023	N3160	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.GC7AA.003	ICDN3160	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3160	947023	N3160	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.GK4AA.025	C157200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	951957	15-7200U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.10 GHz) FC-8GA14F, Tray	
NX.H9AAA.002	ICDN3450	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3450	951833	N3450	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.H9AAA.003	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.H9AAA.004	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
N9.EFJWW.005	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.H70AA.002	C178565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5	17-8565U	982918	17-8565U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA14F, Tray	
N9.H92WW.001	ICDN4000	1273	14nm	GEMINI LAKE	INTEL(R) CELEBRON(R)	N4000	961640	N4000	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA15F, Tray	
N9.H1WWW.002	C181130U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	18-1130U	963178	18-1130U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
N9.H99WW.003	ICDN3350	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3350	951834	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA15F, Tray	
NX.H4BAA.002	ICDN3350	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3350	951833	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.H4BAA.003	ICDN3450	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3450	951833	N3450	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.H11AA.002	ICDN3450	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3450	951833	N3450	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.H11AA.003	PQCIN4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)	N4200	951830	N4200	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.50 GHz) FC-8GA15F, Tray	
NX.GY3AL.003	ICDN3060_OFF	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3060	951881	N3060	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.GY3AL.004	ICDN3060_OFF	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3060	951881	N3060	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.H2BAL.015	C157200U/H22	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-7200U	953353	15-7200U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.10 GHz) FC-8GA14F, Tray	
NX.GYAL.003	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NH.Q3WAL.010	C183300U	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	18-300H	963720	18-300H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.00 GHz) FC-8GA14F, Tray	
NX.GWAA.004	PQCIN4200	1273	14nm	APOLLO LAKE	INTEL(R) CORE(TM) I5	15-8200U	951830	15-8200U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.50 GHz) FC-BGA15F, Tray	
NX.H3WAA.002	C158265U	1272	14nm	WHISKEY LAKE	INTEL(R) PENTIUM(R)	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA14F, Tray	
NX.G5WAA.004	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.H8AAA.004	C178565U	1272	14nm	WHISKEY LAKE	N/A	17-8565U	982918	17-8565U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.60 GHz) FC-8GA14F, Tray	
NH.Q40AA.001	C158300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8300H	963720	15-8300H	INTEL(R) SILVER N5000 Processor (9M Cache, up to 4.00 GHz) FC-8GA14F, Tray	
NX.GXAAA.012	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.H6AAA.001	PQCIN3710	1272	14nm	BRASWELL	INTEL(R) PENTIUM(R)	N3710	947020	N3710	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.56 GHz) FC-BGA15F, Tray	
NX.GNSAA.013	C182500U	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	N3710	947020	N3710	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.56 GHz) FC-BGA15F, Tray	
NX.H9AAA.006	C181450U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5	18-145U	980656	18-145U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.G4AAA.006	ICDN3060	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3060	947022	N3060	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.H89AA.005	C158265U	1272	14nm	WHISKEY LAKE	N/A	15-8265U	982921	15-8265U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.90 GHz) FC-8GA15F, Tray	
NX.GNSAL.021	ICDN3350	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3350	951834	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.GNPAL.037	C137020UF	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	13-7020U	959164	13-7020U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.G5PAL.026	C137020UF	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	13-7020U	959164	13-7020U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.GNPA.034	C137020UF	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3	13-7020U	959164	13-7020U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.GMBA.006	ICDN3060	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3060	947022	N3060	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.GRAL.012	ICDN3350	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3350	951834	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
N9.G55WW.010	ICDN3060	1273	14nm	BRASWELL	INTEL(R) CELEBRON(R)	N3060	947022	N3060	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.48 GHz) FC-8GA15F, Tray	
NX.VGTPA.011	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.GRAL.007	ICDN3350	1273	14nm	APOLLO LAKE	INTEL(R) CELEBRON(R)	N3350	951834	N3350	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.40 GHz) FC-8GA15F, Tray	
NX.EFAA.005	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.H1WAA.006	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.H4AAA.003	ICDN4000	1273	14nm	GEMINI LAKE	INTEL(R) CELEBRON(R)	N4000	961640	N4000	INTEL(R) SILVER N5000 Processor (9M Cache, up to 2.60 GHz) FC-8GA15F, Tray	
NT.LDTAA.006	C177500U/H22	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	17-7500U	953352	17-7500U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.50 GHz) FC-8GA14F, Tray	
NX.GR7AA.014	C158250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	15-8250U	959160	15-8250U	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.40 GHz) FC-8GA14F, Tray	
NX.G77A.003	C177755/H22	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7	17-7775	953348	17-7775	INTEL(R) SILVER N5000 Processor (9M Cache, up to 3.60 GHz) FC-8GA14F, Tray	

ITEM NUMBER	CPU	PRODUCT TYPE	PROCESS CODE	PROCESS NODE	ARCHITECTURE	PROCESSOR	PROCESSOR#	MMID	EXTERNAL PRODUCT MARKETING NAME
DT.VRDA005	963592		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500T	963592	Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray
DT.VRDA006	963506		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700T	963506	Intel® Core™ i7-8700T Processor (12M Cache, up to 4.00 GHz) FC-LGA14C, Tray
DG.E11AA.012	960619		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8400	960619	Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C, Tray
DG.E11AA.004	960618		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700	960618	Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
DT.BARAA.006	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DT.BARAA.007	960619		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8400	960619	Intel® Core™ i5-8400 Processor (9M Cache, up to 4.00 GHz) FC-LGA14C, Tray
DG.E11AA.014	960618		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700	960618	Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
DQ.VS0AA.001	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DQ.VS0AA.002	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DQ.VS0AA.003	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DQ.VRZAA.001	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DQ.VRZAA.002	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DQ.VRZAA.003	960618		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700	960618	Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
DQ.VRZAA.004	960618		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700	960618	Intel® Core™ i7-8700 Processor (12M Cache, up to 4.60 GHz) FC-LGA14C, Tray
DT.VQVAA.001	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DT.VQVAA.002	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DT.VR0AA.002	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DT.VR0AA.003	960012		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I3	13-8100	960012	Intel® Core™ i3-8100 Processor (6M Cache, 3.60 GHz) FC-LGA14C, Tray
DT.VQVAA.005	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DT.VQVAA.006	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DT.VR0AA.006	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DT.VR0AA.007	963598		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500	963598	Intel® Core™ i5-8500 Processor (9M Cache, up to 4.10 GHz) FC-LGA14C, Tray
DT.VRDA008	963506		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7	17-8700T	963506	Intel® Core™ i7-8700T Processor (12M Cache, up to 4.00 GHz) FC-LGA14C, Tray
DT.VRDA009	963592		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500T	963592	Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray
DT.VRDA010	963592		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500T	963592	Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray
DT.VRDA011	963592		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500T	963592	Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray
DT.VRDA012	963592		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	15-8500T	963592	Intel® Core™ i5-8500T Processor (9M Cache, up to 3.50 GHz) FC-LGA14C, Tray

ASUS						
ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
PE200S	Motherboard	PE200S	E930	14 nm	APOLLO LAKE	INTEL(R) ATOM(TM)
PE200S	Motherboard	PE200S	E940	14 nm	APOLLO LAKE	INTEL(R) ATOM(TM)
PE200S	Motherboard	PE200S	E950	14 nm	APOLLO LAKE	INTEL(R) ATOM(TM)
PRIME J3355I-C	Motherboard	PRIME J3355I-C	J3355	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	E201NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	E203NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	E402NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
E Series	Laptop	E403NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	TP202NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	TP203NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	TP203NAH	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	X540NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
X Series	Laptop	X541NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
Chromebook	Laptop	C213NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
Chromebook	Laptop	C223NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
Chromebook	Laptop	C423NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
Chromebook	Laptop	C523NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
Chromebook	Laptop	C403NA	N3350	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
	Laptop	C223NA	N3350/N4200	14 nm	APOLLO LAKE	INTEL(R) CELERON®, PENTIUM®
VivoBook	Laptop	TP401NA	N3450	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
X Series	Laptop	X541NA	N3450	14 nm	APOLLO LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	E402NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
E Series	Laptop	E403NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
VivoBook	Laptop	TP203NAH	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
VivoBook	Laptop	TP401NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
X Series	Laptop	X541NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
VivoBook	Laptop	X751NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
Chromebook	Laptop	C423NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
Chromebook	Laptop	C523NA	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
ASUSPRO	Laptop	P2540NV	N4200	14 nm	APOLLO LAKE	INTEL(R) PENTIUM®
ASUSPRO	Desktop	E410	Celeron N3150	14 nm	BRASWELL	INTEL(R) CELERON(R)
ASUSPRO	AIO	A4110	J3160	14 nm	BRASWELL	INTEL(R) CELERON(R)
E Series	Laptop	E402SA	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)
X Series	Laptop	X540SA	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)
X Series	Laptop	X553SA	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)
ASUSPRO	Laptop	P552SA	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)
N3050I-C	Motherboard	N3050I-C	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)
N3050T R2.0	Motherboard	N3050T R2.0	N3050	14 nm	BRASWELL	INTEL(R) CELERON(R)

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
N3050T	Motherboard	N3050T	N3050		14 nm	BRASWELL	INTEL(R) CELERON(R)
N3150I-C	Motherboard	N3150I-C	N3050		14 nm	BRASWELL	INTEL(R) CELERON(R)
Chromebook E Series	Laptop	C300SA	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
	Laptop	E402SA	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
	Laptop	E406SA	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
Chromebook	Laptop	C202SA	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
PRIME N3060T	Motherboard	PRIME N3060T	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
N3060I-CM-A	Motherboard	N3060I-CM-A	N3060		14 nm	BRASWELL	INTEL(R) CELERON(R)
E Series	Laptop	E402SA	N3150		14 nm	BRASWELL	INTEL(R) CELERON(R)
ASUSPRO	AIO	A4110	N3150		14 nm	BRASWELL	INTEL(R) CELERON(R)
Chromebook	Laptop	C300SA	N3160		14 nm	BRASWELL	INTEL(R) CELERON(R)
VivoBook	Laptop	X541SA	N3160		14 nm	BRASWELL	INTEL(R) CELERON(R)
N3160TH	Motherboard	N3160TH	N3160		14 nm	BRASWELL	INTEL(R) CELERON(R)
X Series	Laptop	X540SA	N3700		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
X Series	Laptop	X553SA	N3700		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
X Series	Laptop	X751SA	N3700		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
N3700T	Motherboard	N3700T	N3700		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
E Series	Laptop	E402SA	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
	Laptop	E406SA	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
X Series	Laptop	X540SA	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
VivoBook	Laptop	X541SA	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
X Series	Laptop	X751SA	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
Chromebox	Chrome Device	CN62	N3710		14 nm	BRASWELL	INTEL(R) PENTIUM(R)
Chromebox	Chrome Device	CN62	Celeron 3205U		14 nm	BROADWELL	INTEL(R) CELERON(R)
Transformer Book	Laptop	TP300LA	Celeron 3215U		14 nm	BROADWELL	INTEL(R) CELERON(R)
X Series	Laptop	X540LA	i3-5005U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
VivoBook	Laptop	X555LA	i3-5005U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
X Series	Laptop	X751LA	i3-5005U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
ASUSPRO	Laptop	P552LA	i3-5005U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
X Series	Laptop	X455LA	i3-5005U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
Transformer Book	Laptop	TP300LA	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
Transformer Book	Laptop	TP500LA	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
VivoBook	Laptop	X555LA	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
X Series	Laptop	X751LA	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
X Series	Laptop	X455LA	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
Chromebox	Chrome Device	CN62	i3-5010U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
Transformer Book	Laptop	TP300LA	i3-5020U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3
X Series	Laptop	X540LA	i3-5020U		14 nm	BROADWELL	INTEL(R) CORE (TM) I3

ASUS						
ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
VivoBook	Laptop	X555LA	i3-5020U	14 nm	BROADWELL	INTEL (R) CORE (TM) i3
Transformer Book	Laptop	TP300LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
Transformer Book	Laptop	TP300LD	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
Transformer Book	Laptop	TP500LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
Transformer Book	Laptop	TP550LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
ZenBook	Laptop	UX303LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
X Series	Laptop	X540LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
VivoBook	Laptop	X555LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
X Series	Laptop	X751LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
ASUSPRO	Laptop	P552LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
ET2323I	AIO	ET2323I	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
PT2001	AIO	PT2001	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
K/A Series	Laptop	K401LB	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
K Series	Laptop	K501LX	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
	Laptop	N542LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
ZenBook	Laptop	UX305LA	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
X Series	Laptop	X555LB	i5-5200U	14 nm	BROADWELL	INTEL (R) CORE (TM) i5
	Laptop	N591LN	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP300LD	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP500LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP500LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP550LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
ZenBook	Laptop	UX301LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
ZenBook	Laptop	UX303LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
ZenBook	Laptop	UX303LN	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
VivoBook	Laptop	X555LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
X Series	Laptop	X751LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
ASUSPRO	Laptop	P552LA	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
K/A Series	Laptop	K401LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
K Series	Laptop	K501LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
K Series	Laptop	K501LX	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
	Laptop	N591LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP300LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
Transformer Book	Laptop	TP550LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
ZenBook	Laptop	UX303LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
X Series	Laptop	X302LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
X Series	Laptop	X455LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7
X Series	Laptop	X455LN	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) i7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
X Series	Laptop	X540LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
X Series	Laptop	X555LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
X Series	Laptop	X555LJ	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
X Series	Laptop	X7511LB	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
X Series	Laptop	X7511LX	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
Chromebox	Chrome Device	CN62	i7-5500U	14 nm	BROADWELL	INTEL (R) CORE (TM) I7
Transformer Book	Laptop	T300CHI	M-5Y10	14 nm	BROADWELL	Intel® Core™ M-5Y10a
Transformer Book	Laptop	T300FA	M-5Y10	14 nm	BROADWELL	Intel® Core™ M-5Y10a
ZenBook	Laptop	UX305FA	M-5Y10	14 nm	BROADWELL	Intel® Core™ M-5Y10a
Transformer Book	Laptop	T300CHI	M-5Y71	14 nm	BROADWELL	Intel® Core™ M-5Y71
ZenBook	Laptop	UX305FA	M-5Y71	14 nm	BROADWELL	Intel® Core™ M-5Y71
VivoStick	Stick PC	TS10	Z8300	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
Transformer Book	Laptop	T101HA	Z8350	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
Transformer Book	Laptop	T102HA	Z8350	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
Transformer Book	Laptop	T103HAF	Z8350	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
VivoStick	Stick PC	TS10	Z8350	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
Transformer Book	Laptop	T100HA	Z8500	14 nm	CHERRY TRAIL	INTEL(R) ATOM(TM)
VivoMini	Mini PC	VC66-C	Celeron G4900	14 nm	COFFEE LAKE	INTEL(R) ATOM(TM)
VivoMini	Mini PC	VC66-C	i3-8100	14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I3
PB Series	Mini PC	PB60	i3-8100T	14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I3
PB Series	Mini PC	PB60G	i3-8100T	14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I3
TUF	Laptop	FX504GD	i5-8300H	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
TUF	Laptop	FX504GE	i5-8300H	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
TUF	Laptop	FX504GM	i5-8300H	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
TUF	Laptop	FX705GM	i5-8300H	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL503GE	i5-8300H	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
TUF	Desktop	FX10CP	i5-8400	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
ROG	Desktop	GL12CP	i5-8400	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
TUF	Desktop	FX10CS	i5-8400	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC66-C	i5-8400	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
PB Series	Mini PC	PB60	i5-8400T	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
PB Series	Mini PC	PB60G	i5-8400T	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC66-C	i5-8500	14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
ROG	Desktop	G21CN	i7-8700	14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I7
ROG	Desktop	GL12CM	i7-8700	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Desktop	GL12CP	i7-8700	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Desktop	FX10CS	i7-8700	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
VivoMini	Mini PC	VC66-C	i7-8700	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
ROG	Desktop	GL12CM	I7-8700K	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
Zen AiO	AIO	Z2725D	I7-8700T	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
PB Series	Mini PC	PB60	I7-8700T	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
PB Series	Mini PC	PB60G	I7-8700T	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ZenBook	Laptop	UX550GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ZenBook	Laptop	UX550GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
VivoBook	Laptop	X580GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX504GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX504GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX504GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX505GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX705GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX705GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	G703GI	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	G703GS	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL503GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL504GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL504GS	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL703GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL703GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL703GS	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GL704GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GM501GS	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GX501GI	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	GX531GS	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
ROG	Laptop	ZN242GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
Zen AiO	AIO	FX505GE	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
TUF	Laptop	FX705GD	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I8
TUF	Laptop	G703GX	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I9
ROG	Laptop	GL504GV	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I10
ROG	Laptop	GL504GW	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I11
ROG	Laptop	GL704GV	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I12
ROG	Laptop	GL704GW	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I13
ROG	Laptop	GM501GM-GM501GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I14
ROG	Laptop	GM501GM-GU501GM	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I15
ROG	Laptop	GX531GW	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I16
ROG	Laptop	GX531GX	I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I17
ROG	Laptop		I7-8750H	14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I18

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
ROG	Laptop	GX701GX	i7-8750H		14 nm	COFFEE LAKE	INTEL(R) CORE (TM) I19
ROG	Desktop	GL12CX	i7-9700K		14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I7
ProArt Series	Mini PC	PA90	i7-9700K		14 nm	COFFEE LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX550GEX	i9-8950HK		14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
ROG	Laptop	G703GI	i9-8950HK		14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
ROG	Laptop	G703GX	i9-8950HK		14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
ROG	Desktop	GL12CX	i9-9900K		14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
ProArt Series	Mini PC	PA90	i9-9900K		14 nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
VivoMini	Mini PC	VC66-C	Pentium G5400		14 nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD
PB Series	Mini PC	PB60	Pentium G5400T		14 nm	COFFEE LAKE	INTEL(R) PENTIUM(R) GOLD
PN Series	Mini PC	PN40	Celeron J4005		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
PN Series	Mini PC	PN40	Celeron J5005		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
PN Series	Mini PC	PN40	Celeron N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
PN Series	Mini PC	PN40	Celeron N4100		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
PN Series	Mini PC	PN40	Celeron N5000		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
PRIME J4005I-C	Motherboard	PRIME J4005I-C	J4005		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	E203MA	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
	Laptop	E406MA	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	TP401MA	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
X Series	Laptop	X540MA	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
V161	AIO	V161GA	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
PRIME N4000T	Motherboard	PRIME N4000T	N4000		14 nm	GEMINI LAKE	INTEL(R) CELERON(R)
	Laptop	C204MA	N4000/N4100/N5000		14 nm	GEMINI LAKE	INTEL(R) CELERON®, PENTIUM® SILVER
	Laptop	C214MA	N4000/N4100/N5000		14 nm	GEMINI LAKE	INTEL(R) CELERON®, PENTIUM® SILVER
	Laptop	C424MA	N4000/N4100/N5000		14 nm	GEMINI LAKE	INTEL(R) CELERON®, PENTIUM® SILVER
	Laptop	P2540MB	N4000/N4100/N5000		14 nm	GEMINI LAKE	INTEL(R) CELERON®, PENTIUM® SILVER
	Laptop	E406MA	N5000		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
VivoBook	Laptop	TP401MA	N5000		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
X Series	Laptop	X540MA	N5000		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
VivoBook	Laptop	X705MA	N5000		14 nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER
Chromebox	Motherboard	MINING I	3865U		14 nm	KABY LAKE	INTEL(R) CELERON(R)
ASUSPRO	Chrome Device	CN65	Celeron 3865U		14 nm	KABY LAKE	INTEL(R) CELERON(R)
VivoBook	Desktop	E420	Celeron 3865U		14 nm	KABY LAKE	INTEL(R) CELERON(R)
VivoMini	Laptop	X540UA	i3-7020U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
ASUSPRO	Mini PC	VC66	i3-7100		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoBook	Desktop	E520	i3-7100T		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
ZenBook	Laptop	TP510UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
	Laptop	UX430UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
VivoBook	Laptop	X510UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	X541UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
X Series	Laptop	X556UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
X Series	Laptop	X756UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
ASUSPRO	Laptop	P2540UA	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
Chromebox	Chrome Device	CN65	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoMini	Mini PC	UN65U	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoMini	Mini PC	VM65N	i3-7100U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	TP412UA	i3-8130U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
ZenBook	Laptop	UX331UA	i3-8130U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	X540UA	i3-8130U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	X705UA	i3-8130U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
PN Series	Mini PC	PN60-B	i3-8130U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I3
Transformer Book	Laptop	TP301UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP410UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP501UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP501UQ	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX310UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX330UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX360UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX390UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX430UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX430UQ	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX560UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X441UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X510UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X540UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X541UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X556UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X556UQ	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X556UR	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X756UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ASUSPRO	Laptop	B9440UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ASUSPRO	Laptop	P2440UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ASUSPRO	Laptop	P2540UA	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Vivo AIO	AIO	V2211C	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Vivo AIO	AIO	V2411C	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Zen AIO	AIO	ZN2411C	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
VivoMini	Mini PC	UN65U	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VM65N	i5-7200U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL553VD	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL702VI	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL753VD	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X580VD	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
TUF	Laptop	FX503VD	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
TUF	Laptop	FX503VM	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL503VS	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoPC	Desktop	M80CJ	i5-7300HQ		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
	Desktop	G11CD	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoPC	Desktop	K31CD	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoPC	Desktop	M32CD	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
	Desktop	D520SF	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Mini PC	GR8II	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ROG	Mini PC	GR8II6G	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC66	i5-7400		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Zen AiO	AIO	ZN270IE	i5-7400T		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ASUSPRO	Desktop	E520	i5-7400T		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC66	i5-7500		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC68V	i5-7500		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX360CA	i5-7Y54		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP410UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP412UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP510UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	TP510UF	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX330UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX331UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX331UN	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX430UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX430UN	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX460UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX461UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX461UN	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX561UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X411UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X510UA	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X510UN	i5-8250U		14 nm	KABY LAKE	INTEL(R) CORE(TM) I5

ASUS						
ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
VivoBook	Laptop	X530UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X540UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X570UD	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
ASUSPRO	Laptop	P2540UB	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Vivo AiO	AIO	V2411C	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Vivo AiO	AIO	V272UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X420UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X540UB	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	X705UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Vivo AiO	AIO	V222UA	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Chromebox	Chrome Device	CN65	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
PN Series	Mini PC	PN60-B	i5-8250U	14 nm	KABY LAKE	INTEL(R) CORE(TM) I5
Transformer Book	Laptop	T304UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP410UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP501UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP501UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX330UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX360UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX370UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX390UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX410UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX430UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX430UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX490UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX510UX	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX560UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX560UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX560UX	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X541UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
X Series	Laptop	X541UJ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X541UV	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X542UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
X Series	Laptop	X556UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
X Series	Laptop	X556UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X705UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ASUSPRO	Laptop	B9440UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
ASUSPRO	Laptop	P2440UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ASUSPRO	Laptop	P2440UQ	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ASUSPRO	Laptop	P2540UA	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoMini	Mini PC	UN65U	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoMini	Mini PC	VM65N	i7-7500U	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Desktop	G11CD	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Desktop	G20CI	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Desktop	GD30CI	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoPC	Desktop	K31CD	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoPC	Desktop	M32CD	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Mini PC	GR8II	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Mini PC	GR8II6G	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoMini	Mini PC	VC66	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoMini	Mini PC	VC68V	i7-7700	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
FX/ZX Series	Laptop	FX502VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VS	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VM	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VS	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL503VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL503VM	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL553VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL553VE	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL702VI	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL702VM	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL702VS	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL703VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL703VM	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL753VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL753VE	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GX501VIK	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GX501VSK	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX550VE	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
X Series	Laptop	X550VX	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X580VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
TUF	Laptop	FX503VD	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
TUF	Laptop	FX503VM	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL503VS	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
Zen AiO	AIO	ZN242IF	i7-7700HQ	14 nm	KABY LAKE	INTEL (R) CORE (TM) I7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
ROG	Desktop	GT51CH	I7-7700K		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
Zen AiO	AIO	Z240IE	I7-7700T		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ASUSPRO	Desktop	E520	I7-7700T		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G701VI	I7-7820HK		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VS	I7-7820HK		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GX800VH	I7-7820HK		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G703VI	I7-7820HK		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP401CA	I7-7Y75		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP410UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP412UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP510UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	TP510UQ	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX331UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX370UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX391UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX410UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX430UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX430UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX461UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX461UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX490UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX561UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X542UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	UX561UD	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X411UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X411UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X411UQ	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UF	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X510UQ	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X530UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X540UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X542UA	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X570UD	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X705UD	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	X705UN	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
ASUSPRO	Laptop	P2540UB	I7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
ASUSPRO	Laptop	P5440UF	i7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
PN Series	Mini PC	PN60-B	i7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
Chromebox	Chrome Device	CN65	i7-8550U		14 nm	KABY LAKE	INTEL (R) CORE (TM) I7
	Laptop	X406UA	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X407UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X409UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X411UA/UF/JN	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X412UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X420UA	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	TP412UA	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X507UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X509UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X510UA/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X512UA/UB/UF	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X540UA/UB	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
	Laptop	X705UA/UB	i7-8550U/i5-8250U/i3-8130U/4417U		14 nm	KABY LAKE	:L (R) CORE (TM) I3, I5, I7, INTEL(R) PENTIUM
VivoBook	Laptop	TP401CA	m3-7Y30		14 nm	KABY LAKE	INTEL (R) CORE (TM) M
ZenBook	Laptop	UX330CA	m3-7Y30		14 nm	KABY LAKE	INTEL (R) CORE (TM) M
ZenBook	Laptop	UX360CA	m3-7Y30		14 nm	KABY LAKE	INTEL (R) CORE (TM) M
	Laptop	MJ401TA	M3-8100Y		14 nm	KABY LAKE	INTEL (R) CORE (TM) M
	Laptop	C434TA	M3-8100Y/4415Y/i5-8200Y/i7-8500Y		14 nm	KABY LAKE	TEL(R) PENTIUM®, INTEL® CORE™ M, I5,
Chromebook	Laptop	C302CA	4405Y		14 nm	SKYLAKE	INTEL(R) PENTIUM(R)
	Motherboard	H110I-CM-AA	G3900TE		14 nm	SKYLAKE	INTEL(R) CELERON(R)
VivoBook	Laptop	X540UA	i3-6006U		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	X541UA	i3-6006U		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
ASUSPRO	Laptop	P553UA	i3-6006U		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoPC	Desktop	K31CD	i3-6098P		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoPC	Desktop	M32CD	i3-6100		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
	Motherboard	H110I-CM-AA	i3-6100		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoMini	Mini PC	VC66	i3-6100		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoMini	Mini PC	VC65R	i3-6100T		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	TP501UA	i3-6100U		14 nm	SKYLAKE	INTEL (R) CORE (TM) I3
VivoBook	Laptop	X541UA	i3-6100U		14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UA	i3-6100U		14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X756UA	i3-6100U		14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoMini	Mini PC	VM65N	i3-6100U		14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	X541UA	i5-6198DU		14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X555UA	i5-6198DU		14 nm	SKYLAKE	INTEL(R) CORE(TM) I5

ASUS						
ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
X Series	Laptop	X556UQ	i5-6198DU	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X556UR	i5-6198DU	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
K Series	Laptop	K501UX	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
	Laptop	N543UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Transformer Book	Laptop	T303UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Transformer Book	Laptop	TP300UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Transformer Book	Laptop	TP301UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	TP501UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX303UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX305UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX310UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX360UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX560UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	X541UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X555UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X555UB	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UB	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UQ	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X756UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
	Laptop	X756UX	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ASUSPRO	Laptop	P453UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ASUSPRO	Laptop	P553UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Zen AiO	AIO	ZN240IC	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X456UA	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X555UF	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UF	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoMini	Mini PC	VM65N	i5-6200U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ROG	Laptop	GL502VM	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL552VW	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
ROG	Laptop	GL553VW	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	N551VW	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
VivoBook	Laptop	N552VX	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
X Series	Laptop	X550VQ	i5-6300HQ	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
	Desktop	G11CD	i5-6400	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
ROG	Desktop	G20CB	i5-6400	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
VivoPC	Desktop	K31CD	i5-6400	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
VivoPC	Desktop	M32CD	i5-6400	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
ROG	Mini PC	GR8II	i5-6400	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
Vivo AiO	AiO	V230IC	I5-6400T	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
Zen AiO	AiO	Z240IC	I5-6400T	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
VivoMini	Mini PC	VC65R	i5-6400T	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
K Series	Motherboard	H110I-CM-AA	i5-6500TE	14 nm	SKYLAKE	INTEL(R) CORE(TM) I5
K Series	Laptop	K501UW	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Transformer Book	Laptop	K501UX	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
Transformer Book	Laptop	T303UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	TP301UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	TP501UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	TP501UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	TP501UQ	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX303UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX303UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX305UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX310UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX390UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX510UW	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX510UX	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX560UQ	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX560UX	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	X541UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	X541UV	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X555UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X555UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UQ	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X556UR	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
ASUSPRO	Laptop	X756UX	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
K Series	Laptop	P453UA	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	K501UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	N592UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	N593UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X456UJ	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoBook	Laptop	X456UV	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
X Series	Laptop	X756UB	i7-6500U	14 nm	SKYLAKE	INTEL (R) PROCESSOR
	Desktop	G11CB	I7-6700	14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
	Desktop	G11CD	I7-6700	14 nm	SKYLAKE	INTEL (R) CORE (TM) I7

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
ROG	Desktop	G20CB	i7-6700		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
VivoPC	Desktop	M32CD	i7-6700		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Mini PC	GR8II	i7-6700		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VL	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VM	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VS	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VT	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VY	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VM	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VS	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VT	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL502VY	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL552VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL552VX	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL553VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL702VM	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GL752VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ZenBook	Laptop	N501VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	N551VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	N552VW	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
VivoBook	Laptop	N552VX	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
X Series	Laptop	X50VX	i7-6700HQ		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Desktop	GT51CA	i7-6700K		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
Zen AiO	AIO	Z240IC	i7-6700T		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
VivoMini	Mini PC	VC65R	i7-6700T		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G701VI	i7-6820HK		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G701VO	i7-6820HK		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VS	i7-6820HK		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	G752VY	i7-6820HK		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
ROG	Laptop	GX700VO	i7-6820HK		14 nm	SKYLAKE	INTEL (R) CORE (TM) I7
Chromebook	Laptop	C302CA	m3-6Y30		14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX305CA	m3-6Y30		14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX360CA	m3-6Y30		14 nm	SKYLAKE	INTEL (R) PROCESSOR
Chromebook	Laptop	C302CA	m5-6Y54		14 nm	SKYLAKE	INTEL (R) CORE (TM) M
Chromebook	Laptop	C302CA	m7-6Y75		14 nm	SKYLAKE	INTEL (R) PROCESSOR
ZenBook	Laptop	UX305CA	m7-6Y75		14 nm	SKYLAKE	INTEL (R) PROCESSOR
VivoMini	Mini PC	VC66	Pentium G4400		14 nm	SKYLAKE	INTEL(R) PENTIUM(R)
ASUSPRO	Desktop	E520	Pentium G4400T		14 nm	SKYLAKE	INTEL(R) PENTIUM(R)

ASUS

ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	PROCESS NODE	ARCHITECTURE	BRAND
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VivoMini	Mini PC	VC65R	Pentium G4400T	14 nm	SKYLAKE	INTEL(R) PENTIUM(R)
PE200U	Motherboard	PE200U	i3-8145U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I3
ZenBook	Laptop	UX331FN	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX333FA	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX433FA	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX431FA	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX533FN	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	X530FA	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
Vivo AiO	AIO	V241FA	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
PE200U	Motherboard	PE200U	i5-8265U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
ZenBook	Laptop	UX331FAL	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX362FA	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX433FA	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX433FN	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX461FA	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX461FN	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX533FD	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX562FD	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX391FA	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
ZenBook	Laptop	UX431FA	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
VivoBook	Laptop	X530FN	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
	Laptop	X705FD	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
	Laptop	X705FN	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
PE200U	Motherboard	PE200U	i7-8565U	14 nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
	Laptop	X330FA/FN	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X330FL	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X403FA	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X409FA/FB/FJ/FL	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X412FA/FJ	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X412FL	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X420FA	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X430FA/FN	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X432FA/FL	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	TP412FA	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	UX431FA/FN	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X509FA/FB/FJ/FL	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X512FA/FB	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple
	Laptop	X530FN/FA	i7-8565U/i5-8265U/i3-8145U/5405U	14 nm	WHISKEY LAKE	Multiple



ASUS PRODUCT NAME	PRODUCT TYPE	ASUS MODEL NAME	CPU	ASUS	PROCESS NODE	ARCHITECTURE	BRAND
	Laptop	X531FA/FL	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	X532FA/FL	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	X705FD/FN	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	X712FA/FB	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX391FA	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX392FA/FN	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX362FA	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX562FA	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX562FDX	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX334FA/FL	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX434FA/FL	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	UX534FA/FT	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	AIO	V241FA/FF	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	B9440FAV	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	L524FA/FB	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	P3540FA/FB	i7-8565U/i5-8265U/i3-8145U/5405U		14 nm	WHISKEY LAKE	Multiple
	Laptop	GL12CX	i9-9900K/i7-9700K/i5-9400/i5-9400F		14 nm	COFFEE LAKE	Multiple
	Laptop	GL10CS	i9-9900K/i7-9700K/i5-9400/i5-9400F		14 nm	COFFEE LAKE	Multiple
	Laptop	G21CN	i9-9900K/i7-9700K/i5-9400/i5-9400F		14 nm	COFFEE LAKE	Multiple
	Laptop	G21CX	i9-9900K/i7-9700K/i5-9400/i5-9400F		14 nm	COFFEE LAKE	Multiple

MATERIAL NUMBER		PRODUCT DESCRIPTION		LENOVO		PROCESSOR #		PROCESS CODE		PROCESS NODE		Architecture		Processor	
				PRODUCT TYPE		PROCESSOR #		PROCESS CODE		PROCESS NODE		Architecture		Processor	
80V4000GUS		Notebook YG 710-14IKB I5 8G 256 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80V40023US		Notebook YG 710-14IKB I7 8G 256 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80V4008FUS		Notebook YG 710-14IKB I7 8G 256 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WKCT01WW		ASSEMBLY Lenovo Y520-15IKBN		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK0165US		Notebook LN Y520-15IKBN I7 8G 2T 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00F9US		Notebook LN Y520-15IKBN I7 16 2T 256 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK001KUS		Notebook LN Y520-15IKBN I7 16 2T 256 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00FHUS		Notebook LN Y520-15IKBN I5 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00HTUS		Notebook LN Y520-15IKBN I5 16 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00CCUS		Notebook LN Y520-15IKBN I7 16 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK01HEUS		Notebook LN Y520-15IKBN I7 16G 1T128G10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK001LUS		Notebook LN Y520-15IKBN I5 8G 1T 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WK01F2US		Notebook LN Y520-15IKBN I5 8G 256G 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WK001JUS		Notebook LN Y520-15IKBN I7 8G 1T 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WK001MUS		Notebook LN Y520-15IKBN I7 16 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00G5US		Notebook LN Y520-15IKBN I7 16 1T 256 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00T2US		Notebook LN Y520-15IKBN I7 8G 1T 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00T3US		Notebook LN Y520-15IKBN I7 16 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00HSUS		Notebook LN Y520-15IKBN I7 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WKX005US		80WK00F9US S&D M/TM		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WK00MRFC		Notebook LN Y520-15IKBN I5 8G 1T 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WK00MTFC		Notebook LN Y520-15IKBN I7 16 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WKX003US		80WK00F9US REFURB M/TM		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WK00FCUS		Notebook LN Y520-15IKBN I7 8G 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WY0000US		Notebook LN Y520-15IKBA I5 8G 1T 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80WY0000US		Notebook LN Y520-15IKBA I7 8G 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WYCT01WW		ASSEMBLY Lenovo Y520-15IKBA		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WY0011CF		Notebook LN Y520-15IKBA I7 8G 1T 128 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80WY0015CF		Notebook LN Y520-15IKBA I5 8G 1T 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X4000WUS		Notebook IP 3205-14IKB I5 8G 256G 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X400EJUS		Notebook IP 3205-14IKB I3 4G 1T 10H		Notebook		13-7100U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I3	
80X400EHUS		Notebook IP 3205-14IKB I5 8G 1T 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X40094US		Notebook IP 3205-14IKB I3 4G 1T 10H		Notebook		13-7100U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I3	
80X40072US		Notebook IP 3205-14IKB I5 8G 256G 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X40093US		Notebook IP 3205-14IKB I5 8G 1T 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X5005DUS		Notebook IP 3205-15IKB I5 8G 1T 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X5005EUS		Notebook IP 3205-15IKB I7 8G 1T 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X50002US		Notebook IP 3205-15IKB I7 8G 1T 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X50003US		Notebook IP 3205-15IKB I5 8G 1T 10H		Notebook		15-7200U		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X50001US		Notebook IP 3205-15IKB I7 8G 512G 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X50041US		Notebook IP 3205-15IKB I7 8G 256G 10H		Notebook		17-7500U		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7008JUS		Notebook YG 720-15IKB I7 8G 1TB 10P		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7001WUS		Notebook YG 720-15IKB I7 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7003VUS		Notebook YG 720-15IKB I7 8G 1TB 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7008HUS		Notebook YG 720-15IKB I5 8G 256G 10H		Notebook		15-7300HQ		1272		14nm		KABY LAKE		INTEL(R) CORE(TM) I5	
80X7006KUS		Notebook YG 720-15IKB I7 8G 512G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7006NUS		Notebook YG 720-15IKB I7 8G 8G 512G 10P		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7001TUS		Notebook YG 720-15IKB I7 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7001SUS		Notebook YG 720-15IKB I7 8G 8G 512G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X700CAUS		Notebook YG 720-15IKB I7 8G 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7001LUS		Notebook YG 720-15IKB I7 8G 256G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7000CUS		Notebook YG 720-15IKB I7 8G 8G 512G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7008YCF		Notebook YG 720-15IKB I7 8G 1TB 10P		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7001VUS		Notebook YG 720-15IKB I7 8G 8G 512G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	
80X7005PCF		Notebook YG 720-15IKB I7 8G 8G 512G 10H		Notebook		17-7700HQ		1272		14nm		KABY LAKE		INTEL(R) CORE (TM) I7	

MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	LENOVO	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
80X7009XCF	Notebook YG 720-151KB I7 8G 8G 512G 10H	Notebook		17-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0001YUS	Notebook IP FLEX 5-1470 I5 8G 1T 10H	Notebook		15-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00015US	Notebook IP FLEX 5-1470 4415U 4G 1T 10H	Notebook		4415U	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)
80XA0002US	Notebook IP FLEX 5-1470 I3 4G 500 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XA00111US	Notebook IP FLEX 5-1470 I7 16G I1128G 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA00091US	Notebook IP FLEX 5-1470 I7 16G 1T 128G 1	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0009EUS	Notebook IP FLEX 5-1470 I5 16G 1T 256G 1	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00011US	Notebook IP FLEX 5-1470 I7 8G 256G 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0000AUS	Notebook IP FLEX 5-1470 I5 8G 128G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000TUS	Notebook IP FLEX 5-1470 I3 8G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00000US	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000VUS	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00006US	Notebook IP FLEX 5-1470 I7 8G 256G 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0000DUS	Notebook IP FLEX 5-1470 I7 16G 1T 512G 1	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA00011US	Notebook IP FLEX 5-1470 I5 8G 128G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000PIUS	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000KUS	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000CUS	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA0000QCF	Notebook IP FLEX 5-1470 I7 16G I1128G 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0000LFC	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00005CF	Notebook IP FLEX 5-1470 I7 8G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XA0010CF	Notebook IP FLEX 5-1470 I5 8G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XA00134US	Notebook IP FLEX 5-1470 4415U 4G 1T 10H	Notebook		4415U	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)
80XL033RKUS	Notebook IP 320-151KB I7 16G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL0355US	Notebook IP 320-151KB I3 4G 500 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XL035WUS	Notebook IP 320-151KB I7 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL0355US	Notebook IP 320-151KB I5 8G 4G 256G 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XL0039HUS	Notebook IP 320-151KB I3 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XL0006US	Notebook IP 320-151KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XL0000FUS	Notebook IP 320-151KB I7 16G 2T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL033HYUS	Notebook IP 320-151KB I7 4G 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL033CCUS	Notebook IP 320-151KB I3 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XL033CBUS	Notebook IP 320-151KB I5 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XL031BUS	Notebook IP 320-151KB I7 16G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL0311US	Notebook IP 320-151KB I7 16G 2T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL038QUUS	Notebook IP 320-151KB I7 8G 4G 256G 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL0005US	Notebook IP 320-151KB I3 2G 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XL02MRCF	Notebook IP 320-151KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XL039KCF	Notebook IP 320-151KB I7 4G 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XL039JCF	Notebook IP 320-151KB I3 4G 500 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XL0310US	Notebook IP 320-151KB I3 4G 500 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XM006EUS	Notebook IP 320-171KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XM000JUS	Notebook IP 320-171KB I3 4G 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XM000CAUS	Notebook IP 320-171KB I7 4G 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XM000IUS	Notebook IP 320-171KB I7 4G 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XM00000US	Notebook IP 320-171KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XM0002US	Notebook IP 320-171KB I7 16G 2T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XM0006US	Notebook IP 320-171KB I7 16G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
80XM000F0US	Notebook IP 320-171KB I3 4G 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XM000GRUS	Notebook IP 320-171KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XM00011US	Notebook IP 320-171KB I3 2G 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
80XM00008US	Notebook IP 320-171KB I5 4G 4G 1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
80XM000ECF	Notebook IP 320-171KB I7 4G 4G 1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7

MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	LENOVO	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
80XN0098CF	Notebook IP 320-17IKB I3 2G 4G 1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
80XN000AUS	Notebook IP 320-15IKB TOUCH I32G4G1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
80XN0002US	Notebook IP 320-15IKB TOUCH I7 16G2T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80XN0009US	Notebook IP 320-15IKB TOUCH I58G64G1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
80XN000MUS	Notebook IP 320-15IKB TOUCH I7 4G 4G 1T	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80XN0008US	Notebook IP 320-15IKB TOUCH I78G64G1T 10H	Notebook		I7-7500U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80XN0003US	Notebook IP 320-15IKB TOUCH I54G4G1T 10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
80XN0004US	Notebook IP 320-15IKB TOUCH I32G4G1T 10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
80XN000CCF	Notebook IP 320-15IKB TOUCH I5 4G4G1T10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
80XN000BCF	Notebook IP 320-15IKB TOUCH I3 2G4G1T10H	Notebook		I3-7100U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
80XN000DCF	Notebook IP 320-15IKB TOUCH I5 8G4G1T10H	Notebook		I5-7200U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
80XR017EUS	Notebook IP 320-15IAP N3450 4G 500 10H	Notebook		N3450	1273	14nm	APOLLO LAKE	INTEL(R) CELERON®
80XR00A7US	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR017DUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR00AGUS	Notebook IP 320-15IAP N3350 4G 1T 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
80XR017FUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR00AJUS	Notebook IP 320-15IAP N3350 4G 1T 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
80XR00AKUS	Notebook IP 320-15IAP N3350 4G 1T 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
80XR00AMUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR00AHUS	Notebook IP 320-15IAP N3350 4G 1T 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
80XR000WUS	Notebook IP 320-15IAP N3350 4G 1T 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
80XR000GUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR00ALUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80XR00ANUS	Notebook IP 320-15IAP N4200 4G 1T 10H	Notebook		N4200	1273	14nm	APOLLO LAKE	INTEL(R) PENTIUM(R)
80Y7CT01WW	ASSEMBLY Lenovo YOGA 920-13IKB	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70063US	Notebook YG 920-13IKB I5 8G 256G 10H	Notebook		I5-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
80Y70062US	Notebook YG 920-13IKB I7 16G 1TB 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70064US	Notebook YG 920-13IKB I7 8G 512G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70066US	Notebook YG 920-13IKB I7 16G 1TB 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70010US	Notebook YG 920-13IKB I7 16G 512G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y7000WUS	Notebook YG 920-13IKB I7 8G 256G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70074US	Notebook YG 920-13IKB I7 8G 256G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70025US	Notebook YG 920-13IKB I7 16G 512G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70012US	Notebook YG 920-13IKB I7 8G 256G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y700FNUS	Notebook YG 920-13IKB I7 16G 256G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y70061CF	Notebook YG 920-13IKB I7 8G 512G 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y8CT01WW	ASSEMBLY Lenovo YOGA 920-13IKB Glass	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y80000US	Notebook YG 920 Glass I7 16G 1TB 10H	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y8500000	Yoga 920 SW Glass-BBY	Notebook		I7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80YYCT01WW	ASSEMBLY Lenovo Y520-15IKBM	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y00060US	Notebook LN Y520-15IKBM I7 16 2T 256 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y0003PUS	Notebook LN Y520-15IKBM I7 8G 1T 128 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y0009PUS	Notebook LN Y520-15IKBM I7 16G 512G 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y0009NUS	Notebook LN Y520-15IKBM I7 8G 1T 128G10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y00074US	Notebook LN Y520-15IKBM I7 16G 256G 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y00090US	Notebook LN Y520-15IKBM I7 16 1T 128 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80Y0003TCF	Notebook LN Y520-15IKBM I7 8G 1T 10H	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80YYX005US	80Y0074US REFURB MTM	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
80YYX006US	80Y0074US S&D MTM	Notebook		I7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81A400BFUS	Notebook IP 120S-11IAP N3350 2G 64 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
81A400BGUS	Notebook IP 120S-11IAP N3350 2G 64 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
81A40025US	Notebook IP 120S-11IAP N3350 2G 32 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
81A50065US	Notebook IP 120S-14IAP N3350 4G 64 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)
81A50011US	Notebook IP 120S-14IAP N3350 2G 32 10H	Notebook		N3350	1273	14nm	APOLLO LAKE	INTEL(R) CELERON(R)

MATERIAL NUMBER			PRODUCT DESCRIPTION			LENOVO			PROCESSOR #			PROCESS CODE			PROCESS NODE			Architecture			Processor		
MATERIAL NUMBER			PRODUCT DESCRIPTION			PRODUCT TYPE			PROCESSOR #			PROCESS CODE			PROCESS NODE			Architecture			Processor		
81A70001US		Notebook IP FLEX 6-11IGM N5000 4G 128 10H	Notebook	N5000	1273	14mm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER															
81A70002US		Notebook IP FLEX 6-11IGM N5000 4G 64 10S	Notebook	N5000	1273	14mm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER															
81A70003US		Notebook IP FLEX 6-11IGM N4000 2G 64 10H	Notebook	N4000	1273	14mm	GEMINI LAKE	INTEL(R) CELERON(R)															
81A70004US		NB IP FLEX 6-11IGM N4000 4G 64 10S	Notebook	N4000	1273	14mm	GEMINI LAKE	INTEL(R) CELERON(R)															
81A70005US		Notebook IP FLEX 6-11IGM N5000 4G 64 10S	Notebook	N5000	1273	14mm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER															
81A70006US		NB IP FLEX 6-11IGM N5000 4G 64 10S	Notebook	N5000	1273	14mm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER															
81AC0007US		Notebook IP 7205-15IKB I7 8G 512G 10H	Notebook	17-7700HQ	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81AC0008US		Notebook IP 7205-15IKB I5 8G 256G 10H	Notebook	15-7300HQ	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81AC0009US		Notebook IP 7205-15IKB I5 8G 256G 10P	Notebook	17-7700HQ	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81AC0010US		Notebook IP 7205-15IKB I7 8G 512G 10P	Notebook	17-7700HQ	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81AC0011US		Notebook IP 7205-15IKB I5 8G 256G 10H	Notebook	15-7300HQ	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BD0012US		Notebook IP 7205-14IKB I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BD0013US		Notebook IP 7205-14IKB I7 8G 256G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BD0014US		Notebook IP 7205-14IKB I7 16G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BD0015US		Notebook IP 7205-14IKB I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BD0016US		Notebook IP 7205-14IKB I7 16G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BF0017US		Notebook IP 520-15IKB I5 4G 4G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BF0018US		Notebook IP 520-15IKB I7 16G 1T 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BF0019US		Notebook IP 520-15IKB I5 8G 4G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BG0020US		Notebook IP 320-15IKB I5 4G 4G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BG0021US		Notebook IP 320-15IKB I5 4G 4G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BH0002US		Notebook IP 320-15IKB Touch I584G4T10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BH0003US		Notebook IP 320-15IKB Touch I7 8G 4G 1T 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BH0004US		Notebook IP 320-15IKB Touch I54G4G1T10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BH0005US		Notebook IP 320-15IKB Touch I54G4G1T10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BH0006US		81BH0000US REFURB MTM	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BH0007US		81BH0000US S&D MTM	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BH0008US		81BH0001US REFURB MTM	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BU0009US		Notebook IP 320-17IKB I7 16G 1T 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BU0010US		Notebook IP 5205-14IKB I5 8G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BU0011US		Notebook IP 5205-14IKB I7 8G 1T 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BL0012US		Notebook IP 5205-14IKB I7 8G 1T 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BL0013US		Notebook IP 5205-14IKB I7 8G 1T 128G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BL0014US		Notebook IP 5205-14IKB I5 8G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BN0015US		Notebook IP 3205-15IKB I7 8G 256G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BQ0016US		Notebook IP 3205-15IKB I5 8G 1T 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BV0017US		Notebook IP 7205-13IKB I7 8G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BV0018US		Notebook IP 7205-13IKB I7 8G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BV0019US		Notebook IP 7205-13IKB I7 8G 1TB 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BV0020US		Notebook IP 7205-13IKB I7 8G 1TB 10P	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81BV0021US		Notebook IP 7205-13IKB I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81BV0022US		Notebook IP 7205-13IKB I7 8G 1TB 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81C30003US		Notebook YG 720-13IKB I7 8G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81C30004US		Notebook YG 720-13IKB I7 16G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81C30005US		Notebook YG 720-13IKB I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81C30006US		Notebook YG 720-13IKB I7 16G 256G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81C90007US		Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81C90008US		Notebook IP FLEX 5-1470 I7 8G 256G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															
81C90009US		Notebook IP FLEX 5-1470 I5 8G 128G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81C90010US		Notebook IP FLEX 5-1470 I5 8G 128G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81C90011US		Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook	15-8250U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I5															
81C90012US		Notebook IP FLEX 5-1470 I7 8G 512G 10H	Notebook	17-8550U	1272	14mm	KABY LAKE	INTEL(R) CORE(TM) I7															

LENOVO							
MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
81C9000GUS	Notebook IP FLEX 5-1470 I7 16G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81C9000DUS	Notebook IP FLEX 5-1470 I5 8G 256G 10H	Notebook	7-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81C9000KUS	Notebook IP FLEX 5-1470 I7 16G1T256G10H	Notebook	7-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
81C9X002US	81C9000EUS S&D MTM	Notebook	7-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81C9X001US	81C9000EUS REFURB MTM	Notebook	7-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000GUS	Notebook IP FLEX 5-1570 I7 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA000JUS	Notebook IP FLEX 5-1570 I5 8G 500 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA000HUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA001QUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000KUS	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000CUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000PUS	Notebook IP FLEX 5-1570 I58G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA0008US	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA000JUS	Notebook IP FLEX 5-1570 I7 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000BUS	Notebook IP FLEX 5-1570 I7 16G1T256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA001RUS	Notebook IP FLEX 5-1570 I3 8G 128G 10H	Notebook	I3-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
81CA001SUS	Notebook IP FLEX 5-1570 I7 8G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0013US	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5
81CA000RUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0017US	Notebook IP FLEX 5-1570 I7 16G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA001KUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA001TUS	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000DUS	Notebook IP FLEX 5-1570 I7 16G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0009US	Notebook IP FLEX 5-1570 I5 8G 1T128G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA000TUS	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA000AUS	Notebook IP FLEX 5-1570 I7 16G 512G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000VUS	Notebook IP FLEX 5-1570 I7 16G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0007US	Notebook IP FLEX 5-1570 I5 8G 1T 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0001US	Notebook IP FLEX 5-1570 I7 16G 1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000YUS	Notebook IP FLEX 5-1570 I7 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA0010US	Notebook IP FLEX 5-1570 I5 8G 1T 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA0000US	Notebook IP FLEX 5-1570 I5 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CAX018US	81CA000RUS REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX022US	81CA000RUS S&D MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA0016US	Notebook IP FLEX 5-1570 I7 16G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX006US	81CA000JUS REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CAX037US	81CA001KUS REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX039US	81CA001KUS S&D MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX032US	81CA000XUS REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX028US	81CA0017US REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX034US	81CA000XUS S&D MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CAX038US	81CA001TUS REFURB MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CAX040US	81CA001TUS S&D MTM	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81CA0011US	Notebook IP FLEX 5-1570 I7 16G1T256G10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CA000FUS	Notebook IP FLEX 5-1570 I7 8G 256G 10H	Notebook	7-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CR0005US	Notebook IP 720S T-15IKB I7 16G 1TB 10P	Notebook	7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CR0006US	Notebook IP 720S T-15IKB I7 16G 512G 10P	Notebook	7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CR0002US	Notebook IP 720S T-15IKB I7 16G 512G 10H	Notebook	7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CR0003US	Notebook IP 720S T-15IKB I7 16G 1TB 10H	Notebook	7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81CR0004US	Notebook IP 720S T-15IKB I7 16G 512G 10H	Notebook	7-7700HQ	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
81DE01M2US	Notebook IP 330-15IKB I5 4G 4G 1T 16G10H	Notebook	7-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81DE01KRUS	Notebook IP 330-15IKB I3 4G 1T 16G 10H	Notebook	I3-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3

MATERIAL NUMBER		PRODUCT DESCRIPTION		LENOVO		PROCESSOR #		PROCESS CODE		PROCESS NODE		Architecture		Processor	
				PRODUCT TYPE		PROCESSOR #		PROCESS CODE		PROCESS NODE		Architecture		Processor	
81DE0085U5	Notebook IP 330-151KB I3 4G 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE017BU5	Notebook IP 330-151KB I3 4G 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE0044U5	Notebook IP 330-151KB I3 2G 4G 1T 10H	Notebook					81-7020U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE0045U5	Notebook IP 330-151KB I5 4G 4G 1T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DE01P3U5	Notebook IP 330-151KB I3 2G 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE0026U5	Notebook IP 330-151KB I3 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE0025U5	Notebook IP 330-151KB I7 16G 1T 16G 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DE00L8U5	Notebook IP 330-151KB I3 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE00LAU5	Notebook IP 330-151KB I3 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE00T1U5	Notebook IP 330-151KB I3 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE00LBU5	Notebook IP 330-151KB I5 4G 4G 1T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DE00T0U5	Notebook IP 330-151KB I3 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE00L0U5	Notebook IP 330-151KB I5 4G 4G 256G 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DE00LCU5	Notebook IP 330-151KB I3 4G 4G 128G 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DE0043U5	Notebook IP 330-151KB I7 8G 4G 1T 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DE01THU5	Notebook IP 330-151KB I5 4G 4G 256G 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DE0029U5	Notebook IP 330-151KB I5 4G 4G 1T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DJ0007U5	Notebook IP 330-151KB Touch I3 2G4G1T10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DJ0006U5	Notebook IP 330-151KB Touch I5 8G4G1T10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DJ0002U5	Notebook IP 330-151KB Touch I5 8G4G1T10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DJ0004U5	Notebook IP 330-151KB Touch I7 8G4G1T10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DJ0000U5	Notebook IP 330-151KB Touch I7 16G 1T10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DJ0003U5	Notebook IP 330-151KB Touch I5 4G4G1T10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DJ0000AU5	Notebook IP 330-151KB Touch I3 4G4G2T10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DJ0009CF	Notebook IP 330-151KB Touch I5 8G4G1T10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DJ0008U5	Notebook IP 330-151KB Touch I716G1T16G10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DJX003U5	81DJ0002U5 S&D MTM	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DX009U5	81DJ0004U5 REFURB MTM	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DX001U5	81DJ0002U5 REFURB MTM	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DX010U5	81DJ0004U5 S&D MTM	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DJ0000CU5	Notebook IP 330-151KB Touch I716G1T16G10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DJ0000DU5	Notebook IP 330-151KB Touch I5 4G4G1T10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DK0030U5	Notebook IP 330-171KB I3 2G 4G 2T 10H	Notebook					81-7020U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DM0002U5	Notebook IP 330-171KB I3 2G 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DM0001U5	Notebook IP 330-171KB I5 4G 4G 1T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DM0000U5	Notebook IP 330-171KB I5 8G 4G 2T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DM0000MU5	Notebook IP 330-171KB I3 2G 4G 2T 10H	Notebook					81-7020U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DM0000PU5	Notebook IP 330-171KB I7 8G 4G 2T 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DM0000QU5	Notebook IP 330-171KB I3 2G 4G 2T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DM0000RU5	Notebook IP 330-171KB I5 8G 4G 1T 10H	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81DM0000SU5	Notebook IP 330-171KB I7 16G 1T 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DM0000TU5	Notebook IP 330-171KB I7 8G 4G 1T 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DM0004VCF	Notebook IP 330-171KB I3 2G 4G 1T 10H	Notebook					81-8130U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3				
81DM0000U5	Notebook IP 330-171KB I7 16G 1T 16G 10H	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DMX009U5	81DM0005U5 REFURB MTM	Notebook					81-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7				
81DMX007U5	81DM0004U5 REFURB MTM	Notebook					81-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I5				
81FK009U5	Notebook IP 330-151CH I7 8G 4G 1T 16G10H	Notebook					81-8550U	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7				
81FK0002U5	Notebook IP 330-151CH I5 4G 4G 1T 10H	Notebook					81-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I5				
81FK0008U5	Notebook IP 330-151CH I7 16G 1T 128G 10H	Notebook					81-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7				
81FK0007U5	Notebook IP 330-151CH I7 8G 4G 1T 10H	Notebook					81-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7				
81FK0000U5	Notebook IP 330-151CH I5 4G 4G 1T 10H	Notebook					81-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I5				
81FK0001U5	Notebook IP 330-151CH I7 16G 1T 10H	Notebook					81-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7				
81FK009VU5	Notebook IP 330-151CH I5 4G 4G 1T 16G10H	Notebook					81-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I5				
81FK009TU5	Notebook IP 330-151CH I7 16G 1T 16G 10H	Notebook					81-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7				
81FK00ECU5	Notebook IP 330-151CH I5 4G 4G 1T128G10H	Notebook					81-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I5				

LENOVO							
MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
81FK00DBUS	Notebook IP 330-151CH15 4G 4G 2T 10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81FL006FUS	Notebook IP 330-171CH17 8G 4G 1T 16G10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0003US	Notebook IP 330-171CH15 4G 4G 1T 10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81FL0004US	Notebook IP 330-171CH17 16G 1T 128G 10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0005US	Notebook IP 330-171CH17 8G 4G 1T 10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0066US	Notebook IP 330-171CH17 8G 4G 1T 16G10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0095US	Notebook IP 330-171CH17 8G 4G 1T 16G10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0000US	Notebook IP 330-171CH17 16G 1T 10H	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81FL0002US	Notebook IP 330-171CH15 4G 4G 1T 10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81FL0001US	Notebook IP 330-171CH15 4G 4G 1T 10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81FL0007US	81FL0066US REFURB MTM	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81G20086US	Notebook IP 330-141KB13 4G 4G 1T 10H	Notebook	13-7020U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I3
81G20085US	Notebook IP 330-141KB15 4G 4G 1T 10H	Notebook	15-8250U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I5
81G20084US	Notebook IP 330-141KB17 8G 4G 1T 10H	Notebook	17-8550U	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) I7
81HD0003US	Notebook LN LegionY730-151CH1716G1T12810	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HD000NUS	Notebook LN LegionY730-151CH158G1T16G10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81HD000PUS	Notebook LN LegionY730-151CH1716G2T25610	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HD0015US	ASSEMBLY Lenovo Legion Y730-151CH	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81HD001TUS	Notebook LN LegionY730-151CH158G1T16G10H	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81HG0004US	Notebook LN LegionY730-171CH1716G1T12810	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HGCT01VWV	ASSEMBLY Lenovo Legion Y730-171CH	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HG001TUS	Notebook LN LegionY730-171CH1716G1T25610	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HG001PUS	Notebook LN LegionY730-171CH1716G1T25610	Notebook	17-8750H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
81HG001HUS	Notebook LN LegionY730-171CH1516G1T12810	Notebook	15-8300H	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
81SQ0008US	NB IP FLEX-141WL 15 4G 4G 512G 10H	Notebook	15-8265U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
81SQ0001US	NB IP FLEX-141WL 15 4G 4G 512G 10H	Notebook	15-8265U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
81SQ0003US	Notebook IP FLEX-141WL 17 4G 4G 512G 10H	Notebook	17-8565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
81SQ0008US	Notebook IP FLEX-141WL 17 4G 4G 256G 10H	Notebook	17-8565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
81SQ0000US	NB IP FLEX-141WL 15 4G 4G 256G 10H	Notebook	15-8265U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
81SQ000MUS	Notebook IP FLEX-151WL 17 4G 4G 512G 10H	Notebook	17-8565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
81SR0008US	Notebook IP FLEX-151WL 17 16G1T8512G10H	Notebook	17-8565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
81SR000DIUS	Notebook IP FLEX-151WL 17 16G 512G 10H	Notebook	17-8565U	1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
4XG0G89074	CPU_BO LTS RD350 XEON E5-2630 V4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89078	CPU_BO LTS TD350 XEON E5-2620 V4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89079	CPU_BO LTS RD350 XEON E5-2620 V4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89080	CPU_BO LTS RD450 XEON E5-2620 V4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89090	CPU_BO LTS RD450 XEON E5-2603 V4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89093	CPU_BO LTS TD350 Xeon E5-2623 v4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
4XG0G89094	CPU_BO LTS RD350 Xeon E5-2623 v4	SERVER Option		1272	14nm	BROADWELL	INTEL(R) XEON(R)
70TT0025UX	SERVER TS TS460 E31240V6 RAID5201	Enterprise Product Group		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
70TE0011UX	Server TS RS160 E31240V6 12i1	SRV		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
70TG0015UX	Server TS RS160 E31230V6 12i1	SRV		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
70TT0020UX	Server TS TS460 E31230V6 12i1	Enterprise Product Group		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
70U8000AUX	Server TS TS150 E31225V6 12i1	Enterprise Product Group		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
7X02CT01WVW	ThinkSystem SR630 - 3yr Warranty	SRV		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
9532E0U	Flex System x240 M5 Compute Node	SRV		1272	14nm	SKYLAKE	INTEL(R) XEON(R) PLATINUM
3633KTU	LENOVO SYSTEM X3250 M6 E3-1270 M1215	SRV		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
3633KSU	LENOVO SYSTEM X3250 M6 E3-1240 M1215	SRV		1272	14nm	KABY LAKE	INTEL(R) XEON(R)
7Y46CT01WVW	ThinkSystem S7250 - 1Yr Warranty	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)
7X83XV1T00	Lenovo ThinkAgile HX3320 6148x2.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X06TD3800	ThinkSystem SR650 6140x2 32GBx24	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7Y94S0MR00	ThinkAgile VX 2U Node 6130x2 64GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X0254C400	ThinkSystem SR630 6130x2 32GBx24	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD

LENOVO							
MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
7X8350R800	Lenovo ThinkAgile HX3320 5120x2 16GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X0256F200	ThinkSystem SR630 51.20x2 32GBx8	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7XG7A05536	SR630 Xeon 5118 12C/105W/2.3GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X06A05XNA	ThinkSystem SR650 5118 32G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X10100QNA	ThinkSystem ST550 4110 32GB	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X37506K00	ThinkSystem SR670 5118x2 32GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X8450W000	Lenovo ThinkAgile HX7520 6150x2 64GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X37529S00	ThinkSystem SR670 6142x2.0 32GBx12.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X06XT7G00	ThinkSystem SR650 6136x2 16GBx24	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X8351G000	Lenovo ThinkAgile HX3320 6136x2 32GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7XG7A05590	SR650 Xeon 6126 12C/125W/2.6GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X8450C000	Lenovo ThinkAgile HX5520 6126x2 16GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X06U1EB00	ThinkSystem SR650 6126x2 16GBx8	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X06A040NA	ThinkSystem SR650 6134 32GB	SRV		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X067X5100	ThinkSystem SR650 6134x2 32GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7XG7A05605	SR650 Xeon 6134 8C/130W/3.2GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X02A01LNA	ThinkSystem SR630 5115x1 16Gx1	SRV		1272	14nm	SKYLAKE	INTEL(R) XEON(R) GOLD
7X02A04JNA	ThinkSystem SR630 4116x1 32Gx1	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7XG7A05551	ThinkSystem SR630 4116 32GB	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X10A02PNA	ThinkSystem ST550 4116 32GB	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
4XG7A07212	ST550 Xeon Silver 4116 12C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
4XG7A07227	SR570 Xeon 4116 12C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X09CTO1WW	Server SP: ThinkSystem ST550 - 1yr Warra	DCG SERVER OPTIONS HIGH VOLUME		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y8950TTM00	ThinkAgile HX1321 Node 4114 16GBx12	Enterprise Product Group		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X8351G000	Lenovo ThinkAgile HX3320 4114x2 16GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y8950UN000	ThinkAgile HX1321 Node 4114 32GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X060UT8900	ThinkSystem SR650 4114x2 32GBx24	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X02T6H0A00	ThinkSystem SR650 4114x2 16GBx4	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7XG7A05575	SR650 Xeon 4110 8C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X10A028NA	ThinkSystem ST550 4110 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X03A02BNA	THINKSYSTEM SR570 SERVER 4110 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X02A03UNA	ThinkSystem SR630 4110x1 16Gx1	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
4XG7A07215	ST550 Xeon Silver 4110 8C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X10100NNA	ThinkSystem ST550 4110 16GB	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X04W9TE00	ThinkSystem SR590 Server 4110 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X99A03DNA	ThinkSystem SR550 4110x2.0 16GBx4.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X02T6BT00	ThinkSystem SR630 4110x2.0 16GBx4.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
4XG7A07263	SR590 Xeon 4110 8C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
4XG7A07195	SR550 Xeon 4110 8C/85W/2.1GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X04A04YNA	ThinkSystem SR550 4110 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y8950RT00	HX2321 Node 3YR 4110x2 32GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X8350D200	Lenovo ThinkAgile HX1320 4110 8GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X04A057NA	ThinkSystem SR550 4110 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y0350CT00	ThinkSystem SR570 4110x2.0 16GBx2.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X085GTE00	ThinkSystem SR530 4110 16GBx4	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X83524T00	Lenovo ThinkAgile HX3320 4110x2 16GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y99T99U00	ThinkSystem SR590 4110 16GB	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X06T7M7R00	ThinkSystem SR650 4110 16GBx12	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7X02532N00	ThinkSystem SR630 4110x2 16GBx6	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) SILVER
7Y03A02JNA	ThinkSystem SR570 Server 3106 16G	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE
4XG7A07218	ST550 Xeon Bronze 3106 8C/85W/1.7GHZ	SERVER Option		1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE
7X0853Y000	ThinkSystem SR530 3104x1.0 16GBx4.0	ThinkSystem		1272	14nm	SKYLAKE	INTEL(R) XEON(R) BRONZE
7Y46A002NA	ThinkSystem ST250 E-2174G 8GB	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)
7Y49A01CNA	ThinkSystem ST550 Server E-2144G 8GB	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R) XEON(R)



MATERIAL NUMBER	PRODUCT DESCRIPTION	PRODUCT TYPE	PROCESSOR #	PROCESS CODE	PROCESS NODE	Architecture	Processor
7Y46A019NA	THINKSYSTEM ST250 E-2136 8GB	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
7Y51S0HB00	ThinkSystem SR250 E-2136 16GBx4	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
7Y51S0PJ00	ThinkSystem SR250 E-2136 16GBx2	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
7Y51S0SE00	ThinkSystem SR250 E-2136 16GB	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
7Y49A013NA	ThinkSystem ST50 Server E-2124G 8GB	ThinkSystem		1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
MSI									
A0E-N305015-106		942602	DUAL CORE N3050	911-7890-001	MB	1273	14nm	BRASWELL	INTEL(R) CELERON(R)
A0F-N315015-106		942600	QUAD CORE N3150	911-7890-103	MB	1273	14nm	BRASWELL	INTEL(R) CELERON(R)
A0F-N316015-106		947023	QUAD CORE N3160	911-7890-104	MB	1273	14nm	BRASWELL	INTEL(R) CELERON®
A0E-N370015-106		942599	QUAD CORE N3700	956-AC1611-025	AIO	1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)
A0E-N371015-106		947020	QUAD CORE N3710	956-AC1611-029	AIO	1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)
A0E-N371015-106		947020	QUAD CORE N3710	956-B12011-056	DT	1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)
A0E-N371015-106		947020	QUAD CORE N3710	956-AE9211-018	AIO	1273	14nm	BRASWELL	INTEL(R) PENTIUM(R)
A0F-N316015-106		947023	QUAD CORE N3160	956-AC1611-024	AIO	1273	14nm	BRASWELL	INTEL(R) CELERON(R)
A0F-N316015-106		947023	QUAD CORE N3160	956-AA8811-048	AIO	1273	14nm	BRASWELL	INTEL(R) CELERON(R)
A0B-5010U15-106		939363	DUAL CORE i3-5010U	939-9A69-002	Server BB	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i3
A0E-G456000-106		952994	DUAL CORE G4560	956-AAC111-021	AIO	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)
A0B-5005U35-106		940707	DUAL CORE i3-5005U	936-B09611-062	DT BB	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i3
A0B-5005U35-106		940707	DUAL CORE i3-5005U	936-B09612-004	DT BB	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i3
A0D-5950H15-106		943431	QUAD CORE i7-5950HQ	957-181212-263	NB	1272	14nm	BROADWELL	INTEL (R) CORE (TM) i7
A0D-5500U15-106		939360	DUAL CORE i7-5500U	956-B09611-251	DT	1272	14nm	BROADWELL	INTEL (R) CORE (TM) i7
A13-2220125-106		939362	DUAL CORE i5-5200U	956-B09611-225	DT	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i5
A13-2220125-106		939362	DUAL CORE i5-5200U	959-9A75-004	Server	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i5
A13-2220125-106		939362	DUAL CORE i5-5200U	939-9A75-003	Server BB	1272	14nm	BROADWELL	INTEL(R) CORE(TM) i5
A0D-5700H15-106		943450	QUAD CORE i7-5700HQ	957-161212-453	NB	1272	14nm	BROADWELL	INTEL (R) CORE (TM) i7
A0D-5700H15-106		943450	QUAD CORE i7-5700HQ	957-16H512-606	NB	1272	14nm	BROADWELL	INTEL (R) CORE (TM) i7
A0H-2176G00-106		963450	6 CORE E-2176G	957-17A512-018	NB	1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
A0H-2176M05-106		963717	6 CORE E-2176M	957-17C532-293	NB	1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
A0H-2176M05-106		963717	6 CORE E-2176M	957-17C532-294	NB	1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
A0H-2176M05-106		963717	6 CORE E-2176M	957-17C632-200	NB	1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
A0H-2176M05-106		963717	6 CORE E-2176M	957-16P632-280	NB	1272	14nm	COFFEE LAKE	INTEL(R)XEON(R)
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B92621-002	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B91641-270	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B92631-054	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B92631-251	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B92631-253	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0K-9900K00-106		983354	8 CORE i9-9900K	956-B92631-062	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i9
A0C-8400000-106		960619	6 CORE i5-8400	957-1T3111-023	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8400000-106		960619	6 CORE i5-8400	956-B91531-459	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8400000-106		960619	6 CORE i5-8400	956-B92011-005	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8400000-106		960619	6 CORE i5-8400	956-B92011-225	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8400000-106		960619	6 CORE i5-8400	956-B92011-236	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8600K00-106		960620	6 CORE i5-8600K	956-B91314-067	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0C-8600K00-106		960620	6 CORE i5-8600K	956-B91314-234	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5
A0D-8700000-106		960618	6 CORE i7-8700	957-1T3111-022	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) i7
A0D-8700000-106		960618	6 CORE i7-8700	957-1T3131-060	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) i7
A0D-8700000-106		960618	6 CORE i7-8700	957-1T3131-061	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) i7
A0D-8700000-106		960618	6 CORE i7-8700	957-1T3131-059	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) i7
A0D-8700000-106		960618	6 CORE i7-8700	957-1T3131-080	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) i7

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-8700000-106	960618	6 CORE I7-8700	957-1T3111-215	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-1T3131-208	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B90721-230	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-003	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-208	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-204	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91531-242	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	936-B92011-012	DT BB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	936-B92011-009	DT BB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-238	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-201	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B90721-223	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92012-002	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91531-457	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-004	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-040	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B90721-224	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-097	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B90721-232	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-202	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-237	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91531-458	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-17A512-005	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-17A512-008	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-17A512-007	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-17A512-006	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-030	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-091	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91621-095	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91611-007	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91621-093	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-027	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-069	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-084	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-086	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91621-094	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-074	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-068	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91611-006	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-085	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-028	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-065	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-233	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-062	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-036	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-073	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-001	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700000-106	960618	6 CORE I7-8700	956-B91314-204	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700000-106	960618	6 CORE I7-8700	936-B92011-010	DT BB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700000-106	960618	6 CORE I7-8700	956-B91621-039	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700000-106	960618	6 CORE I7-8700	956-B90721-233	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8850H05-106	963719	6 CORE I7-8850H	957-16Q211-278	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8850H05-106	963719	6 CORE I7-8850H	957-16Q211-287	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92621-021	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92621-003	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91611-008	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91711-029	DT		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-135	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-125	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-095	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-145	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I7
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-17A311-267	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-17A311-269	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16Q211-276	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16Q211-274	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16JF42-200	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16R112-409	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16R112-249	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-17C612-239	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-16Q211-279	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-16Q211-286	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-085	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-17C612-201	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-075	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-446	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-664	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-077	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16JE32-016	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16JE32-057	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16JE32-061	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-499	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-444	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-069	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-627	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16P612-657	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5
A0C-8300H05-106	963720	QUAD CORE I5-8300H	957-16R112-223	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16P612-221	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16P732-209	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-17C722-028	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16JF42-042	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16JF42-260	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16JF42-275	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16R112-065	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16P612-071	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8300H05-106	963720	QUAD CORE i5-8300H	957-16R312-030	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8400H05-106	963721	QUAD CORE i5-8400H	957-16Q211-275	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8400H05-106	963721	QUAD CORE i5-8400H	957-17A311-268	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8400H05-106	963721	QUAD CORE i5-8400H	957-17A311-266	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0C-8400H05-106	963721	QUAD CORE i5-8400H	957-16Q211-273	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) i5	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17E112-055	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C612-418	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C612-412	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C612-282	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C612-031	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C612-421	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C512-012	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C512-676	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C512-456	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-17C512-641	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-803	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-077	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-439	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-602	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-609	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K722-017	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K722-024	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K722-030	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K722-056	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K722-055	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16K622-018	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-448	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-456	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-663	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-012	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-011	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P512-605	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-013	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16P522-438	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	
A0D-8750H05-106	963718	6 CORE i7-8750H	957-16L411-047	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) i7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16L411-048	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q312-020	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-067	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-809	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-447	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-066	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-210	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-448	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-805	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C612-413	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C612-032	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C612-425	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16L411-046	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16L411-052	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K622-019	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K622-046	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K622-045	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-179E33-007	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B512-045	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B512-012	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-626	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-033	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-485	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-041	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-807	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-053	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-405	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-068	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-054	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-037	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-406	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-283	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-268	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-245	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-259	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q213-450	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q213-441	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q312-073	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q312-021	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JE32-015	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JE32-056	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P512-603	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P512-493	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
					Product Type					
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16P512-672	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16P512-447	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16P512-025	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16P512-010	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C522-626	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C522-609	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C522-014	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-179F43-011	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q213-442	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-16L411-061	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-181612-014	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-181612-027	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-181612-016	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-17A311-057	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-17A311-056	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-17A311-275	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-17A311-273	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-16K731-040	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-16K631-034	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106		963719	6 CORE I7-8850H	957-16K731-039	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16P522-428	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16JF42-035	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C632-077	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C632-281	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C632-078	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-243	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-291	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-045	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-244	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-051	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-270	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C532-606	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C532-258	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C532-292	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C532-605	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16JF42-034	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16JF31-037	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16JF42-205	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C632-076	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-17C632-273	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-277	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-047	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106		963718	6 CORE I7-8750H	957-16Q211-050	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-007	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-222	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-088	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-066	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-248	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-264	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-410	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C622-001	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C622-403	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-445	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-076	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-625	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-238	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-239	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-624	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-052	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-064	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-051	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-010	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-040	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-046	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-047	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-009	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-235	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-621	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-623	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-233	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-234	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-620	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q221-431	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P532-639	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P532-673	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P532-629	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-064	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-063	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-059	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C512-672	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C512-013	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-016	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-014	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-055	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-058	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-274	NB		1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-276	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JE22-058	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-615	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-209	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-636	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-443	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-806	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-015	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-016	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-442	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-065	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P612-068	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-16Q221-615	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-16Q221-476	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-071	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-272	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-277	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-093	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A311-094	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P722-052	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q411-004	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q411-007	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P732-054	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-049	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q411-005	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P722-053	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-050	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A611-015	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A611-013	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q411-006	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P722-051	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C722-010	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-091	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-089	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-089	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C612-436	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16L511-032	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16L511-033	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A611-011	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-204	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-042	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-203	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91641-273	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91641-272	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-040	DT	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-202	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P522-201	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K722-021	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P522-202	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C612-408	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K622-022	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-048	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-073	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-074	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q213-449	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-060	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-291	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-290	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P632-292	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P722-012	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-021	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-824	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P732-013	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-064	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-048	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-17A611-012	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-251	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-248	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8850H05-106	963719	6 CORE I7-8850H	957-181612-035	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-249	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700K00-106	960617	6 CORE I7-8700K	956-B91314-243	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C622-434	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91641-271	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-267	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91641-274	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A611-014	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JF42-276	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-041	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P512-805	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-252	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-093	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q412-253	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-022	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-250	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91911-051	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-080	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JE32-018	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JF42-041	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P732-014	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16K512-033	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91314-252	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17E212-023	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	957-17A522-069	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-411	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R112-252	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17B712-026	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C512-077	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B92631-055	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16R312-029	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P512-226	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B92011-406	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q411-002	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91318-278	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-9700K00-106	983355	8 CORE I7-9700K	956-B91318-279	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16P622-823	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C622-437	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C512-078	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-079	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8850H05-106	963719	6 CORE I7-8850H	957-17A311-039	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-059	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C622-041	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0K-8950H05-106	975241	6 CORE I9-8950HK	957-16Q221-622	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I9	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C522-081	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17A311-040	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	607-17B71-025	NB-MB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0C-8400000-106	960619	6 CORE I5-8400	957-17C622-040	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE(TM) I5	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16JF42-259	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17G111-205	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-17C632-209	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8750H05-106	963718	6 CORE I7-8750H	957-16Q211-271	NB	1272	14nm	COFFEE LAKE	INTEL(R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	957-17A512-026	NB	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0D-8700000-106	960618	6 CORE I7-8700	956-B91314-230	DT	1272	14nm	COFFEE LAKE	INTEL (R) CORE (TM) I7	
A0F-N400005-106	961640	DUAL CORE N4000	956-AAC211-005	AIO	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	
A0F-N400005-106	961640	DUAL CORE N4000	956-AAC211-007	AIO	1273	14nm	GEMINI LAKE	INTEL(R) CELERON(R)	
A0E-N500005-106	961638	QUAD CORE N5000	956-AAC211-025	AIO	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	
A0E-N500005-106	961638	QUAD CORE N5000	956-AAC211-008	AIO	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	
A0E-N500005-106	961638	QUAD CORE N5000	956-AAC211-006	AIO	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	
A0E-N500005-106	961638	QUAD CORE N5000	956-B17111-010	DT	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	
A0E-N500005-106	961638	QUAD CORE N5000	956-B17111-011	DT	1273	14nm	GEMINI LAKE	INTEL(R) PENTIUM(R) SILVER	

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AC1711-212	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AAC111-028	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AAC111-029	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AAC111-002	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AC1711-087	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AAC111-053	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AAC111-052	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0B-7100000-106	954033	DUAL CORE i3-7100	956-AC1711-083	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0C-7200025-106	953353	DUAL CORE i5-7200U	956-AEC113-009	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200025-106	953353	DUAL CORE i5-7200U	936-B15921-020	DT BB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200025-106	953353	DUAL CORE i5-7200U	936-B15921-033	DT BB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200005-106	951957	DUAL CORE i5-7200U	957-16J712-058	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200005-106	951957	DUAL CORE i5-7200U	957-179773-026	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200005-106	951957	DUAL CORE i5-7200U	936-B14211-006	DT BB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7200025-106	953353	DUAL CORE i5-7200U	939-9A95-005	IPS-BB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0H-E315025-106	952951	QUAD CORE E3-1505MV6	957-16H812-675	NB	1272	14nm	KABY LAKE	INTEL(R) XEON(R)
A0H-E315025-106	952951	QUAD CORE E3-1505MV6	957-17A131-687	NB	1272	14nm	KABY LAKE	INTEL(R) XEON(R)
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J962-265	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J962-1407	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J962-2011	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16P112-228	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J962-407	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J962-624	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16M312-010	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16J942-285	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16JD21-093	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7300H05-106	952959	QUAD CORE i5-7300HQ	957-16JD21-280	NB	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-020	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-258	DT	1273	14nm	KABY LAKE	INTEL(R) CORE(TM) i6
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-242	DT	1274	10nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-274	DT	1275	10nm	KABY LAKE	INTEL(R) CORE(TM) i8
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-053	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i9
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-268	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i10
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-091	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i11
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-028	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i12
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B09031-264	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i13
A0C-7400010-106	952986	QUAD CORE i5-7400	956-AE9311-069	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i14
A0C-7400010-106	952986	QUAD CORE i5-7400	956-AE9311-054	AIO	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i15
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90111-224	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i16
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-047	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i17
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B91011-020	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i18
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-261	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i19
A0C-7400010-106	952986	QUAD CORE i5-7400	956-B90611-086	DT	1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i20

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0C-8250U05-106	959160	QUAD CORE i5-8250U	957-14B121-060	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0C-8250U05-106	959160	QUAD CORE i5-8250U	957-14B141-064	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0E-G456000-106	952994	DUAL CORE G4560	956-AAC111-026	AIO		1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)
A0C-8250U05-106	959160	QUAD CORE i5-8250U	957-14B141-269	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i5
A0F-G393000-106	954043	DUAL CORE G3930	956-AAC111-023	AIO		1272	14nm	KABY LAKE	INTEL(R) CELERON(R)
A0F-G393000-106	954043	DUAL CORE G3930	956-AAC111-027	AIO		1272	14nm	KABY LAKE	INTEL(R) CELERON(R)
A0B-7100U05-106	951959	DUAL CORE i3-7100U	936-B14211-007	DT BB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i3
A0D-7500U05-106	951958	DUAL CORE i7-7500U	936-B14211-005	DT BB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7500U05-106	951958	DUAL CORE i7-7500U	957-16JA11-013	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7500U05-106	951958	DUAL CORE i7-7500U	957-16JA11-002	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7500U05-106	951958	DUAL CORE i7-7500U	957-16JA21-017	NB		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-077	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90111-217	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-037	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B09031-281	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91511-008	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-073	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91521-071	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91521-088	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B9031-267	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-089	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91511-021	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-271	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-405	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-063	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91511-007	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90111-215	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-062	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90612-096	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-202	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-018	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90111-216	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-058	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91521-252	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-217	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-267	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90612-070	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91521-036	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91521-070	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B91511-006	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-013	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90711-057	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7
A0D-7700010-106	953004	QUAD CORE i7-7700	956-B90611-090	DT		1272	14nm	KABY LAKE	INTEL(R) CORE(TM) i7

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0D-7700H05-106	953004	QUAD CORE I7-7700	956-B90711-078	DT		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	953004	QUAD CORE I7-7700	956-B90612-272	DT		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	953004	QUAD CORE I7-7700	956-B90711-036	DT		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	953004	QUAD CORE I7-7700	956-B09031-246	DT		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K222-105	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179993-402	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1067	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-053	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-001	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-062	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-079	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-068	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B412-009	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J911-059	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1083	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1082	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1091	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1032	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1093	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179577-1210	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179C11-080	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1896	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBC2-1029	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBC2-1038	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17A121-1006	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17A121-1226	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17A121-693	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-178541-448	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-178554-638	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-178554-639	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-1097	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-1440	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-1463	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-863	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-1227	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-1218	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799E5-699	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBA1-837	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBA1-1061	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBA1-836	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBB2-1008	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBC2-873	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16IB92-1264	NB		1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBC2-877	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBE2-1044	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JBE2-1048	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J932-264	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179941-030	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB12-466	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B93-281	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16L231-239	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16L231-240	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16L231-238	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179BCC-677	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179983-622	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179983-615	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-250	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-298	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-402	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-066	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-045	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-249	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-256	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-003	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C312-008	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C312-023	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17A211-215	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B93-284	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179BCC-651	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179BCC-848	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179BCC-668	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179BCC-650	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J962-625	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J962-056	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-223	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-224	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-441	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-466	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-444	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B112-225	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17A211-214	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-14A332-069	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-14A332-210	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J962-620	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J962-2027	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J962-2013	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-2631	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1645	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-2089	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1273	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1408	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1427	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1646	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-2070	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I962-1096	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB12-822	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB12-659	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JD21-001	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JD21-279	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16M312-008	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179947-027	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB92-661	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB92-653	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799C9-666	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-001	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-202	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-212	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-096	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-213	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-075	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB82-644	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB12-694	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179983-621	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179983-667	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I9C2-1045	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799D3-1250	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799D3-1214	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I572-1862	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I572-1861	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-1799D3-1213	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B11-416	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B11-418	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B11-665	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0F-3865U05-106	953360	DUAL CORE 3865U	936-B15921-019	DT BB	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	
A0F-3865U05-106	953360	DUAL CORE 3865U	956-AEC113-025	AIO	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	
A0F-3865U05-106	953360	DUAL CORE 3865U	956-AEC113-026	AIO	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B11-865	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I572-1833	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I572-1828	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16I572-1832	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-021	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-002	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K332-024	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K322-066	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K332-023	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K412-016	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179941-658	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179941-096	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179B11-471	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K232-280	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K412-060	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K222-610	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K222-467	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K232-290	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16P112-215	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-002	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K412-060	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K412-061	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0E-4415U05-106	953359	DUAL CORE 4415U	956-B15921-019	DT	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	
A0E-4415U05-106	953359	DUAL CORE 4415U	956-AEC113-023	AIO	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	
A0E-4415U05-106	953359	DUAL CORE 4415U	956-AEC113-024	AIO	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K412-062	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B312-089	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B312-001	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B312-033	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17B312-060	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J912-1452	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J912-2096	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J912-2025	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J912-2088	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-067	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-17C112-252	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB42-463	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-179985-028	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J9C2-1046	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J9F1-1095	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16J9B2-2223	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16JB42-408	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K212-228	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K222-294	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K212-275	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K212-674	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	
A0D-7700H05-106	952957	QUAD CORE I7-7700HQ	957-16K222-293	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K212-230	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K212-252	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K212-229	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K222-401	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-17A121-1005	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-17A121-1039	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-17A121-865	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-17A121-887	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16P312-008	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16J982-2076	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K312-001	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K322-206	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K312-034	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K312-078	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K322-063	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16JC12-034	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16JC12-003	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-181542-253	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-181542-252	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-181542-213	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-181542-212	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-16K222-407	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16JC12-041	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-179883-473	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16J932-055	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-179BC3-670	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7920H05-106		952952	QUAD CORE I7-7920HQ	957-16K322-040	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-1799A8-444	NB-BB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K232-297	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K332-067	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16J982-1428	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16J962-1227	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-178541-450	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-16K412-253	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700H05-106		952957	QUAD CORE I7-7700HQ	957-14A332-072	NB	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91211-014	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-013	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-016	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91211-052	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-052	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-012	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-015	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7
A0D-7700K10-106		953006	QUAD CORE I7-7700K	956-B91312-028	DT	1272	14nm	KABY LAKE	INTEL (R) CORE (TM) I7

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
A0D-7700K10-106	953006	QUAD CORE I7-7700K	956-B91211-022	DT	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7700K10-106	953006	QUAD CORE I7-7700K	956-B91211-024	DT	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7700K10-106	953006	QUAD CORE I7-7700K	957-1T1122-243	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0F-3865U05-106	953360	DUAL CORE 3865U	956-AEC113-056	AIO	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A211-205	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A211-028	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A211-082	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A211-083	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A211-202	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-480	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-423	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0E-4415U05-106	953359	DUAL CORE 4415U	956-AEC113-055	AIO	1272	14nm	KABY LAKE	INTEL(R) PENTIUM(R)
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-479	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-1T2111-067	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-1T2111-088	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-823	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1038	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1024	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-872	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1095	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0B-7100U25-106	953354	DUAL CORE I3-7100U	936-B15921-030	DT-BB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I3
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1216	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1084	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-858	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-867	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-1097	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-866	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A131-648	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A131-1205	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A131-1211	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-425	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-181542-266	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-17A121-426	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-1T2111-239	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-7820H05-106	952955	QUAD CORE I7-7820HK	957-1T2111-251	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-8550U05-106	959163	QUAD CORE I7-8550U	957-14B121-270	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-8550U05-106	959163	QUAD CORE I7-8550U	957-14B121-059	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0D-8550U05-106	959163	QUAD CORE I7-8550U	957-14B212-074	NB	1272	14nm	KABY LAKE	INTEL(R) CORE (TM) I7
A0F-3865U05-106	953360	DUAL CORE 3865U	956-A61611-036	AIO	1272	14nm	KABY LAKE	INTEL(R) CELERON(R)
A0B-6100010-106	945208	DUAL CORE I3-6100	956-AC1711-035	AIO	1272	14nm	SKYLAKE	INTEL(R) CORE (TM) I3
A0H-E315015-106	944366	QUAD CORE E3-1505MV5	957-16H812-258	NB	1272	14nm	SKYLAKE	INTEL(R) XEON(R)
A0H-E315015-106	944366	QUAD CORE E3-1505MV5	957-178212-400	NB	1272	14nm	SKYLAKE	INTEL(R) XEON(R)
A0H-E315015-106	944366	QUAD CORE E3-1505MV5	957-178212-423	NB	1272	14nm	SKYLAKE	INTEL(R) XEON(R)

COMPONENT NAME		MMID	CPU TYPE	MSI ITEM #	Product Type	PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
MSI									
A0C-6300H15-106	944367	QUAD CORE I5-6300HQ	957-179675-001	NB	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6300H15-106	944367	QUAD CORE I5-6300HQ	956-AEA111-041	AIO	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6300H15-106	944367	QUAD CORE I5-6300HQ	956-AEA111-049	AIO	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6300H15-106	944367	QUAD CORE I5-6300HQ	957-161622-047	NB	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6300H15-106	944367	QUAD CORE I5-6300HQ	957-179586-696	NB	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-B90611-009	DT	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-B90611-008	DT	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-B90111-070	DT	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-AF1C11-026	AIO	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-AE9311-022	AIO	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0C-6400020-106	947207	QUAD CORE I5-6400	956-B90111-050	DT	1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I5	
A0E-G440010-106	943908	DUAL CORE G4400	956-AA7811-058	AIO	1272	14nm	SKYLAKE	INTEL(R) PENTIUM(R)	
A0D-6700010-106	943465	QUAD CORE I7-6700	956-B90111-093	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700010-106	943465	QUAD CORE I7-6700	956-B90111-208	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700010-106	943465	QUAD CORE I7-6700	956-B90111-209	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700010-106	943465	QUAD CORE I7-6700	956-B90111-061	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700020-106	947202	QUAD CORE I7-6700	957-1T1111-028	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-67000K10-106	943463	QUAD CORE I7-6700K	956-B90311-018	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K20-106	947200	QUAD CORE I7-6700K	957-1T1111-091	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K20-106	947200	QUAD CORE I7-6700K	957-1T1111-096	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K20-106	947200	QUAD CORE I7-6700K	957-1T1111-002	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K10-106	943463	QUAD CORE I7-6700K	956-B90511-032	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K10-106	943463	QUAD CORE I7-6700K	956-B90511-033	DT	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700K20-106	947200	QUAD CORE I7-6700K	957-1T1111-029	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178211-219	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-181412-012	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178312-245	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-177514-202	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-175B12-003	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-161B42-218	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-161B42-248	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	956-AEA211-014	AIO	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16H712-002	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
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A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-161B12-001	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
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A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-161221-078	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
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A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178312-219	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178312-258	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-181512-023	NB	1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7	

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-181512-055	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-058	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-202	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-226	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-060	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-200	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-017	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-181412-002	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-181412-274	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-1T2111-007	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178344-030	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178211-408	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-1T2111-02S	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-178233-805	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-1T2111-006	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6820H25-106	944356	QUAD CORE I7-6820HK	957-17A111-201	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6920H15-106	944371	QUAD CORE I7-6920HQ	957-178311-041	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J562-1446	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J12-650	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J12-086	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
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A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-179441-070	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-422	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-001	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-034	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-021	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-469	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-179541-003	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-179B11-009	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-179B11-010	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6920H15-106	944371	QUAD CORE I7-6920HQ	957-178312-218	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6920H15-106	944371	QUAD CORE I7-6920HQ	957-178312-260	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6920H15-106	944371	QUAD CORE I7-6920HQ	957-181412-257	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-178211-034	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-178211-831	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J412-233	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-14A312-006	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-178511-063	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16K212-041	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J512-203	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-178511-033	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-16J12-021	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7
A0D-6700H15-106	944368	QUAD CORE I7-6700HQ	957-178511-032	NB		1272	14nm	SKYLAKE	INTEL (R) CORE (TM) I7

COMPONENT NAME	MMID	CPU TYPE	MSI ITEM #	MSI		PROCESS CODE	PROCESS NODE	ARCHITECTURE	BRAND
				Product Type	Brand				
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-178533-031	NB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-178511-015	NB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-16H712-053	NB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-178211-1252	NB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-178511-076	NB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0D-6700H15-106	944368	QUAD CORE i7-6700HQ	957-179441-033	NB-BB		1272	14nm	SKYLAKE	INTEL(R) CORE(TM) I7
A0C-8265U15-106	982921	QUAD CORE i5-8265U	957-14B321-200	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
A0C-8265U15-106	982921	QUAD CORE i5-8265U	957-16S111-099	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
A0C-8265U15-106	982921	QUAD CORE i5-8265U	957-16S111-200	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I5
A0D-8565U05-106	982918	QUAD CORE i7-8565U	957-16S111-008	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
A0D-8565U05-106	982918	QUAD CORE i7-8565U	957-16S111-085	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
A0D-8565U05-106	982918	QUAD CORE i7-8565U	957-16S111-091	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7
A0D-8565U05-106	982918	QUAD CORE i7-8565U	957-16S211-018	NB		1272	14nm	WHISKEY LAKE	INTEL(R) CORE(TM) I7

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **INITIAL DETERMINATION** has been served via EDIS upon the Commission Investigative Attorney, **John Shin, Esq.**, and the following parties as indicated, on 6/16/2020.



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UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN INTEGRATED CIRCUITS AND
PRODUCTS CONTAINING THE SAME**

Inv. No. 337-TA-1148

ORDER NO. 34: CONSTRUING TERMS OF THE ASSERTED CLAIMS

(October 2, 2019)

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I. INTRODUCTION

This investigation was instituted by the Commission on March 15, 2019 to determine whether certain tri-gate integrated circuits and products which contain such circuits infringe U.S. Patent Nos. 7,943,966 (“the ’966 patent”), 7,948,012 (“the ’012 patent”), 10,141,334 (“the ’334 patent”), 10,141,335 (“the ’335 patent”), and 10,186,523 (“the ’523 patent”) (altogether, “the Asserted Patents”). See 84 Fed. Reg. 9558-9 (Mar. 15, 2019). On October 2, 2019, however, the ’966 and ’012 patents were terminated from the investigation. (Order No. 33.) The complainant is Tela Innovations, Inc. (“Tela” or “Complainant”). The respondents are Acer, Inc., Acer America Corporation, AsusTek Computer Inc., Asus Computer International, Intel Corporation, Lenovo Group Ltd., Lenovo (United States) Inc., Micro-Star International Co., Ltd., and MSI Computer Corp. (together, “Respondents”). The Commission Investigative Staff (“Staff”) is also a participant (all collectively, “the Parties”).

Pursuant to Ground Rule 8, a *Markman* hearing was held July 17, 2019, regarding the interpretation of certain terms of the patent at issue. Prior to the hearing, the Parties filed a joint claim construction chart setting forth a limited set of terms to be construed, with an updated joint chart after the hearing (EDIS Doc. ID 683388; see Order No. 24). Tela and Respondents filed initial and rebuttal claim construction briefs,¹ wherein each party offered its construction for the claim

¹ The briefs and amended chart submitted by the Parties are referred to hereafter as:

CIMB	Complainant’s Corrected Initial <i>Markman</i> Brief
CRMB	Complainant’s Rebuttal <i>Markman</i> Brief
RIMB	Respondents’ Initial <i>Markman</i> Brief
RRMB	Respondents’ Rebuttal <i>Markman</i> Brief
SMB	Staff’s <i>Markman</i> Brief
JC	Updated Joint Claim Construction Chart
Hr’g Tr.	<i>Markman</i> hearing transcript
Tutorial	Joint Technology Tutorial
Comp. Tutorial	Complainant’s Technology Tutorial
Resp. Tutorial	Respondents’ Technology Tutorial

terms in dispute, along with support for its proposed interpretation. The Staff filed a single brief. Further, per my request, the Parties prepared and filed a joint tutorial on the technology at issue (EDIS Doc. ID 680838), as well as their own individualized tutorials (EDIS Doc. IDs 682967, 682993).

II. RELEVANT LAW

“An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a “matter of law exclusively for the court.” *Id.* at 970-71. “The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.” *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the “ordinary and customary meaning of a claim term” as understood by a person of ordinary skill in the art at the time of the invention. 415 F.3d at 1313. “Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.” *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). “Quite apart

from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms.” *Id.* at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) (“In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to ‘particularly point [] out and distinctly claim [] the subject matter which the patentee regards as his invention.’”). The context in which a term is used in an asserted claim can be “highly instructive.” *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.* “Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee.” *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999).

The specification “is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term.” *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptoronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). “[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor’s lexicography governs.” *Id.* at 1316. “In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor.” *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, “[t]he construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be ... the correct construction.” *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Phillips* at 1317; *see Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can “often inform the meaning of the claim language by

demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips*, 415 F.3d at 1317; *see Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (“The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.”).

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* “The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence.” *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, “if the only claim construction that is consistent with the claim’s language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid.” *Id.*

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) “the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention”; or

(2) “the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009); *see also GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (“the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal.”); *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) (“[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.”); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) (“The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution.”). Nevertheless, there is a “heavy presumption that a claim term carries its ordinary and customary meaning.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is “exacting” and requires “a clear and unmistakable disclaimer.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012); *see Epistar Corp. v. Int’l Trade Comm’n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring “expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope” to deviate from the ordinary meaning) (citation omitted). As the Federal Circuit has explained, “[w]e do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that.” *Thorner*, 669 F.3d at 1366.

A claim must also be definite. Pursuant to 35 U.S.C. § 112, second paragraph: “The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.” 35 U.S.C. § 112, ¶ 2. In *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014), the Supreme Court held that § 112, ¶ 2 requires “that a patent’s claims, viewed in light of the specification and prosecution history

inform those skilled in the art about the scope of the invention with reasonable certainty.” A claim is required to “provide objective boundaries for those of skill in the art,” and a claim term is indefinite if it “might mean several different things and no informed and confident choice is among the contending definitions.” *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). A patent claim that is indefinite is invalid. 35 U.S.C. § 282(b)(3)(A).

Courts are not required to construe every claim limitation of an asserted patent. *See O2 Micro Intern. Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (citations omitted); *Vanderlande Indus. Nederland BV v. Int’l Trade Comm’n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms). Rather, “claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims.” *Id.* at 1362 (quoting *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997)); *see also Embrex*, 216 F.3d at 1347 (“The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.”) (citation omitted).

In addition, “[a] determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.” *O2 Micro*, 521 F.3d at 1361. Claim construction, however, is not an “obligatory exercise in redundancy.” *U.S. Surgical Corp.*, 103 F.3d at 1568. “[M]erely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction.” *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004).

III. LEVEL OF ORDINARY SKILL

Respondents' opening brief offers no description of the person of ordinary skill in this art.

(See generally RIMB.) An expert declaration attached to the brief, however, offers the following:

In my opinion, with respect to the Asserted Patents, a person of ordinary skill in the art would have had the equivalent of a bachelor's degree in electrical engineering, physics, or materials science and at least three years of experience in semiconductor integrated circuit design, layout, and/or fabrication. Additional graduate education could substitute for professional experience, while significant experience in the field might substitute for formal education.

(RIMB, Ex. 6 at ¶ 29.)

The Staff offers the following definition:

The Staff submits that one of ordinary skill in the field of semiconductor design and manufacturing, as related to the Asserted Patents, would have at least a Bachelor of Science degree in electrical or computer engineering or a related field *and* two to three years of practical experience, such as with semi-conductor design and/or manufacturing, or in lieu of practical experience at least a Master's degree in electrical or computer engineering or a related field. All of the Asserted Patents relate back to the same provisional application, No. 60/781,288, which was filed on March 9, 2006. The time period for the state of the art is, therefore, around 2006.

(SMB at 5.)

These proposed levels of skill are substantially similar. Tela initially proposed a level of skill in the art which was not pertinent, and later submitted a corrected brief with a more helpful proposal, although Tela never moved for leave to file it. In any event, Tela's corrected proposed definition is substantially similar to the other parties'. (CIMB at 13.)

Based on the technology and industry behind semiconductor integrated circuits at the 45-193 nm scale, at least three years of experience, as opposed to two, is an appropriate minimum for a person with only a bachelor's degree. The expected undergraduate majors for one of ordinary skill working in hardware, as opposed to software or more theoretical fields, would be electrical

engineering and computer engineering. Physics and materials science might be appropriate, but those disciplines provide less practical experience in design, layout work, and fabrication. And although experience can substitute for education, and education for experience, at least some practical experience would normally be required in a field focused on design and fabrication, even for a person with a master's degree.

On balance, a person having ordinary skill in the art at the time of invention would have: (1) a bachelor's degree in electrical engineering or computer engineering with at least three years of experience in the field of semiconductor layout technology and integrated circuit design; (2) a master's degree in electrical engineering or computer engineering with at least two years of experience in the same field; (3) a bachelor's degree in physics or materials science with at least five years of experience in the same field; or (4) a comparable combination of education and experience.

IV. THE ASSERTED PATENTS

The '334 patent, entitled "Semiconductor Chip Including Region Having Rectangular-Shaped Gate Structures and First-Metal Structures," was issued on November 27, 2018 to Scott T. Becker and Michael C. Smayling. The '334 patent reports an assignment on its face to Tela Innovations, Inc.

The '335 patent, entitled "Semiconductor Cip [sic] Including Region Having Rectangular-Shaped Gate Structures and First Metal Structures," was issued on November 27, 2018 to Scott T. Becker and Michael C. Smayling. The '335 patent reports an assignment on its face to Tela Innovations, Inc.

The '523 patent, entitled "Semiconductor Chip Having Region Including Gate Electrode Features Formed in Part from Rectangular Layout Shapes on Gate Horizontal Grid and First-Metal Structures Formed in part from Rectangular Layout Shapes on at least Eight First-Metal Gridlines

of First-Metal Vertical Grid,” was issued on January 22, 2019 to Scott T. Becker and Michael C. Smayling. The ’523 patent reports an assignment on its face to Tela Innovations, Inc.

All three of the Asserted Patents issued from continuation applications, which claim priority to a series of previous continuation applications, with an ultimate claim of priority to Provisional Application No. 60/781,288, filed on March 9, 2006. All Asserted Patents therefore essentially share a common specification. (CIMB at 10 n.1; RIMB at 4 n.2.)

A. Technical Background

A semiconductor is a material that has electrical conductivity properties falling between that of a conductor and an insulator. (Tutorial at 2.) These conductive properties may be changed with the addition of impurities. (*Id.* at 6.) The addition of different types of impurities results in two different types of semiconductor, known as p-type and n-type. (*Id.*)

P-type and n-type semiconductors can be used with other materials to construct transistors. (Tutorial at 10-13.) The relevant transistor here is a complementary metal oxide semiconductor, or CMOS. (*Id.* at 11, 14.) A CMOS transistor is made of four basic components: (1) a body made of one type of semiconductor; (2) a source region made of the other type of semiconductor; (3) a drain region also made of the other type of semiconductor; (4) a gate made of metal and an oxide, where the gate oxide functions as an insulator by separating the gate metal from the other components. (*Id.* at 10-14.) The source region and the drain region together constitute the diffusion region.² (’523 patent at 9:35-42 (“diffusion regions 203 represent selected regions of the base substrate 201 within which impurities are introduced” and “diffusion contacts 205 are defined to enable connection between source and drain diffusion regions 203”).)

² Although this term is construed below with regard to positioning and the nature of the substrate, the Parties do not dispute that the source and drain regions together form the diffusion region. (SMB at 36.)

When a voltage is applied to the gate an electric field is formed under it, causing a conductive channel connecting the source and drain to either appear or disappear, depending on the voltage and the type of semiconductor used to form the source and drain. (Tutorial at 10-16.) As a result, current can be made to either flow or not flow from source to drain, and the transistor in effect acts as an on/off switch. (*Id.* at 10, 13.) Logic circuits using this switching effect may be formed by connecting many transistors together. (Tutorial at 10; Resp. Tutorial at 3-6.) A set of such circuits disposed on a semiconductor substrate is called an integrated circuit, or chip. (Tutorial at 2.) A silicon wafer is the substrate material for a CMOS chip. (*Id.* at 17.)

The circuitry on a CMOS chip is formed through a multi-stage process, including layout, in which the size, shape, and spacing of the chip's features are specified, followed by photolithography. (Tutorial at 17, 19; *see* RIMB, Ex. 6 at 6 (“A layout represents the size, shape, and spacing guidelines for a given layer in a transistor”); Comp. Tutorial at 2 (describing “Layout & Simulation” as occurring before “Fabrication & Verification”).) In photolithography, a material called photoresist is deposited on the wafer. (*Id.* at 17.) Photoresist undergoes chemical changes when exposed to light. (*Id.* at 19.) In one embodiment of the photolithography process, a pattern of opaque chrome material is placed on transparent quartz glass to form a photomask corresponding to at least a portion of the layout. (*Id.* at 18.) The photomask is placed over the wafer, ultraviolet light is shined through it, and the underlying photoresist chemically changes to match the photomask's pattern. (*Id.*) Application of a solvent then removes some of the photoresist, leaving the remaining photoresist in either a positive or negative pattern (depending on the photoresist) matching that of the photomask. (*Id.* at 18-19.)

Further processing can then be used to build features on the wafer; for example, in areas where photoresist has been removed, material may be added by deposition or removed by etching. (Tutorial at 19; Comp. Tutorial at 15-28.) Repeated application of photolithography and additional

processing results in a “stack of layers” on the wafer. (’523 patent at 9:14-15; *see generally* ’523 patent at Fig. 2.) Within these layers, the various features forming the integrated circuit include gates, gate electrodes, source and drain contacts, and other elements, all of which “enable . . . the desired circuit connectivity.” (*Id.* at 9:56-57; *see generally id.* at 9:30-49.)

The density of circuitry can be increased by reducing feature size. (Tutorial at 20.) Historically, feature size has been shrinking, and in many cases features are smaller than the wavelength of the light used for photolithography. (*Id.*) Because of the small feature size, interference patterns are generated during fabrication as shapes on the photomask interact with the light. (’523 patent at 4:16-17.) These interference patterns cause the fabricated feature shape to deviate from the designed feature shape, so much so that failure may result. (*Id.* at 4:22-24.)

In particular, when “two-dimensionally varying features are located in neighboring proximity to each other, the light used to expose the features will interact in a complex and generally unpredictable manner,” and may result in, for instance, “layout feature shape distortion.” (’523 patent at 7:41-44, 8:25.) Although “[c]orrection methodologies” exist to solve this problem, “semiconductor product yield is reduced as a result of . . . two-dimensionally varying features disposed in proximity to each other.” (*Id.* at 4:24, 8:17-21.) The patents in suit claim a new such methodology focused on “topology,” or feature shape. (*Id.* at 7:36-37.) Specifically, the patents in suit assert that “layout feature shape enhancement can be realized if the layout feature shapes are rectangular, near the same size, and are oriented in the same direction.” (*Id.* at 9:8-9.)

B. The Asserted Claims

The ’334 patent has 30 claims. As of the date of this order, claims 1, 2, 5, 6, 9, 11, 15, 20, 24, 29, and 30 are asserted in this investigation, either as infringed or under the domestic industry

technical prong.³ The asserted claims read as follows (with the first instance of the agreed-upon terms in italics and the first instance of the disputed terms highlighted in bold):

1. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a **gate horizontal grid** that includes at least seven **gate gridlines**, wherein adjacent gate gridlines are separated from each other by a **gate pitch** of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon, wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers, wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

³ Claims 7, 10, 22, and 23 are not listed as asserted in the Notice of Investigation, 84 Fed. Reg. 9559, but they are implicated by dependent claims 9, 11, and 24, which are asserted.

a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material, wherein the first-metal layer includes first-metal structures positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline, **each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers**, wherein each pair of first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers; and

at least six **contact structures** formed within the region of the semiconductor chip, wherein at least six gate structures within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six contact structures, each of the at least six contact structures having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in the x-direction, each of the at least six contact structures positioned and sized to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein the logic circuit includes electrical connections that collectively include first-metal structures positioned on at least five of the at least eight first-metal gridlines.

2. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures positioned in accordance with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, each second-metal structure in the region having at least one adjacent second-metal structure positioned next to each of its sides in accordance with an x-coordinate spacing of less than or equal to 193 nanometers, each second-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure positioned thereon, wherein each pair of second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the **gate structures**.

5. The semiconductor chip as recited in claim 2, wherein the at least six **contact structures** are positioned in accordance with a **contact vertical grid**, the contact vertical grid including **contact gridlines** extending in the x-direction, each of the at least six contact structures positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six contact

structures positioned to also extend lengthwise in the x-direction in a substantially centered manner along a corresponding first-metal gridline.

6. The semiconductor chip as recited in claim 2, **wherein each second-metal structure in the region is positioned next to at least one other second-metal structure on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure on a second side in accordance with the second-metal pitch,** wherein the second-metal pitch is measured in the x-direction and is equal to the **gate pitch**.

7. The semiconductor chip as recited in claim 6, wherein each second-metal structure in the region has a substantially equal width as measured in the x-direction.

9. The semiconductor chip as recited in claim 7, wherein the region has a size of 1930 nanometers as measured in the x-direction and a size of 1930 nanometers as measured in the y-direction.

10. The semiconductor chip as recited in claim 7, wherein the region includes a third-metal layer including third-metal structures positioned in accordance with a **third-metal vertical grid**, the third-metal vertical grid including at least eight **third-metal gridlines**, **each third-metal structure in the region having at least one adjacent third-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers**, each third-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure positioned thereon, wherein each pair of third-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the third-metal layer is

positioned third in the stack of metal layers counting upward from the top surfaces of the **gate structures**.

11. The semiconductor chip as recited in claim 10, **wherein each second-metal structure in the region is positioned next to at least one other second-metal structure on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure on a second side in accordance with the second-metal pitch**, wherein the second-metal pitch is measured in the x-direction and is equal to the **gate pitch**.

15. The semiconductor chip as recited in claim 1, wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein each diffusion region that forms part of at least one transistor within the region of the semiconductor chip has a substantially rectangular shape.

20. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures positioned in accordance with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, each second-metal structure in the region having at least one adjacent second-metal structure positioned next to each of its sides in accordance with an x-coordinate spacing of less than or equal to 193 nanometers, each second-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure positioned thereon, wherein each pair of second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the

second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the **gate structures**,

wherein the region includes a third-metal layer including third-metal structures positioned in accordance with a third-metal vertical grid, the third-metal vertical grid including at least eight third-metal gridlines, **each third-metal structure in the region having at least one adjacent third-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers**, each third-metal structure in the third-metal layer having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure positioned thereon, wherein each pair of third-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the third-metal layer is positioned third in the stack of metal layers upward from the top surfaces of the gate structures.

22. The semiconductor chip as recited in claim 20, wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a **gate structure** forming a **gate electrode** of the first transistor of the first transistor type is positioned on a given **gate gridline**, wherein a gate structure forming a gate electrode of the first transistor of the second transistor type is also positioned on the given gate gridline, wherein no other transistor is positioned on the given gate gridline between the gate structures that form the gate electrodes of the first transistor of the first transistor type and the first transistor of the second transistor type,

wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein a diffusion region of the first transistor of the first transistor type is electrically connected to a diffusion region of the first transistor of the second transistor type,

wherein the at least six **contact structures** include a contact structure substantially centered in the x-direction on the given gate gridline at a location between the diffusion regions of the first transistor of the first transistor type and the first transistor of the second transistor type.

23. The semiconductor chip as recited in claim 22, wherein an electrical connection between the **diffusion region** of the first transistor of the first transistor type and the diffusion region of the first transistor of the second transistor type includes at least one first-metal structure and at least one second-metal structure.

24. The semiconductor chip as recited in claim 23, wherein the **gate electrode** of the first transistor of the first transistor type is electrically connected to the gate electrode of the first transistor of the second transistor type.

29. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a **gate horizontal grid** that includes at least seven **gate gridlines**, wherein adjacent gate gridlines are separated from each other by a **gate pitch** of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon, wherein each pair of gate

structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers, wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

a number of **contact structures** formed within the region of the semiconductor chip, wherein each gate structure that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding contact structure having a substantially rectangular shape, wherein each contact structure that contacts a given gate structure that forms any transistor gate electrode does not contact another gate structure, wherein each contact structure having a corresponding length greater than or equal to a corresponding width is oriented to have its corresponding length extend in an x-direction, wherein each contact structure that contacts a corresponding gate structure is positioned to overlap at least one edge of the corresponding gate structure,

wherein each transistor within the region is formed in part by a corresponding **diffusion region**, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a first gate structure forms both a gate electrode of the first transistor of the first transistor type and a gate electrode of the first transistor of the second transistor type.

30. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures positioned in accordance with a **gate horizontal grid** that includes a number of **gate gridlines**, wherein adjacent gate gridlines are separated from each other by a **gate pitch** of less than or equal to about 193 nanometers, each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate structure positioned thereon, wherein each pair of gate structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers, wherein at least one gate structure within the region is a first-transistor-type-only gate

structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region;

a number of **contact structures** formed within the region of the semiconductor chip, wherein each of at least six gate structures within the region has a respective top surface in physical and electrical contact with a corresponding contact structure having a substantially rectangular shape, wherein each contact structure is centered in an x-direction on the gate structure with which it physical contacts, wherein each contact structure that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in an x-direction, wherein each corresponding contact structure is in physical contact with only one gate structure, wherein each corresponding contact structure is positioned to overlap at least one edge of the gate structure contacted by the corresponding contact structure,

wherein each transistor within the region is formed in part by a corresponding **diffusion region**, wherein each diffusion region that forms part of any transistor within the region has a substantially rectangular shape,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a

portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch,

wherein both a gate electrode of a transistor of a first transistor type and a gate electrode of a transistor of a second transistor type are formed by a same gate structure within the region.

The '335 patent has 30 claims. As of the date of this order, claims 1, 2, 5, 6, 9, 11, 15, 20, 24, 29, and 30 are asserted in this investigation, either as infringed or under the domestic industry technical prong.⁴ The asserted claims read as follows (with the first instance of the agreed-upon terms in italics and the first instance of the disputed terms highlighted in bold):

1. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures formed in part based on corresponding gate structure layout shapes used as an input to a *lithography process*, the gate structure layout shapes positioned in accordance with a **gate horizontal grid**, the gate horizontal grid including at least seven **gate gridlines**, each gate structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, each gate gridline having at least one gate structure layout shape positioned thereon, wherein adjacently positioned ones of the gate structures are separated from each other by a **gate pitch**

⁴ Claims 7, 10, 22, and 23 are not listed as asserted in the Notice of Investigation, 84 Fed. Reg. 9559, but they are implicated by dependent claims 9, 11, and 24, which are asserted.

of less than or equal to about 193 nanometers, each of the gate structures having a width of less than or equal to about 45 nanometers, wherein each pair of the gate structures that are positioned in an end-to-end manner are separated from each other by a line end-to-line end gap of less than or equal to about 193 nanometers;

a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material, wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the first-metal structure layout shapes positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline, each of the first-metal structures having at least one adjacent first-metal structure positioned next to each of its sides at a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers;

at least six **contact structures** formed within the region of the semiconductor chip, the at least six contact structures formed in part utilizing corresponding at least six contact structure layout shapes as an input to a lithography process, the at least

six contact structures formed in physical and electrical contact with corresponding ones of at least six of the gate structures, each of the at least six contact structure layout shapes having a substantially rectangular shape and a corresponding length greater than a corresponding width and with the corresponding length oriented in the x-direction, each of the at least six contact structure layout shapes positioned and sized to form its corresponding contact structure to overlap both edges of the top surface of the gate structure to which it is in physical and electrical contact,

wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region, wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit.

2. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to *a lithography process*, the second-metal structure layout shapes positioned in accordance with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, each second-metal structure layout shape in the region having a substantially rectangular shape

and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, wherein each of the second-metal structures has at least one adjacent second-metal structure positioned next to each of its sides at an x-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the **gate structures**.

5. The semiconductor chip as recited in claim 2, wherein the at least six **contact structure** layout shapes are positioned in accordance with a **contact vertical grid**, the contact vertical grid including **contact gridlines** extending in the x-direction, each of the at least six contact structure layout shapes positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six contact structure layout shapes positioned to also extend lengthwise in the x-direction in a substantially centered manner along an associated first-metal gridline.

6. The semiconductor chip as recited in claim 2, wherein each second-metal structure layout shape in the region is positioned next to at least one other second-metal structure layout shape on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure layout shape on a second side in accordance with the second-metal pitch, wherein the second-metal pitch is measured in the x-direction and is equal to the **gate pitch**.

7. The semiconductor chip as recited in claim 6, wherein each second-metal structure layout shape in the region has a substantially equal width as measured in the x-direction.

9. The semiconductor chip as recited in claim 7, wherein the region has a size of 1930 nanometers as measured in the x-direction and a size of 1930 nanometers as measured in the y-direction.

10. The semiconductor chip as recited in claim 7, wherein the region includes a third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a *lithography process*, the third-metal structure layout shapes positioned in accordance with a **third-metal vertical grid**, the third-metal vertical grid including at least eight **third-metal gridlines**, each third-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, wherein each third-metal structure in the region has at least one adjacent third-metal structure positioned next to each of its sides at a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the third-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the third-metal layer is positioned third in the stack of metal layers counting upward from the top surfaces of the **gate structures**.

11. The semiconductor chip as recited in claim 10, wherein each second-metal structure layout shape in the region is positioned next to at least one other second-metal structure layout shape on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure layout shape on a second side in accordance with the second-metal pitch, wherein the second-metal pitch is measured in the x-direction and is equal to the **gate pitch**.

15. The semiconductor chip as recited in claim 1, wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein each diffusion region that forms part of at least one transistor within the region of the semiconductor chip has a substantially rectangular shape.

20. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to a *lithography process*, the second-metal structure layout shapes positioned in accordance with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, each second-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, wherein each second-metal structure in the region has at least one adjacent second-metal structure positioned next to each of its sides at an x-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the second-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the second-metal layer is positioned second in the stack of metal layers counting upward from the top surfaces of the **gate structures**,

wherein the region includes a third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a lithography process, the third-metal structure layout shapes positioned in accordance with a third-metal vertical grid, the third-metal vertical grid including at least eight third-metal gridlines, each third-metal structure layout shape

in the third-metal layer having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, wherein each third-metal structure in the region has at least one adjacent third-metal structure positioned next to each of its sides at a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of the third-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap, wherein the third-metal layer is positioned third in the stack of metal layers counting upward from the top surfaces of the gate structures.

22. The semiconductor chip as recited in claim 20, wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a **gate structure** that forms a **gate electrode** of the first transistor of the first transistor type and a gate structure that forms a gate electrode of the first transistor of the second transistor type are formed to extend lengthwise along a same line, wherein no other transistor is positioned on the same line between the gate structures that form the gate electrodes of the first transistor of the first transistor type and the first transistor of the second transistor type,

wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein a diffusion region of the first transistor of the first transistor type is electrically connected to a diffusion region of the first transistor of the second transistor type,

wherein the at least six **contact structures** include a contact structure substantially centered in the x-direction on the same line at a location between the diffusion regions of the first transistor of the first transistor type and the first transistor of the second transistor type.

23. The semiconductor chip as recited in claim 22, wherein an electrical connection between the **diffusion region** of the first transistor of the first transistor type and the diffusion region of the first transistor of the second transistor type includes at least one first-metal structure and at least one second-metal structure.

24. The semiconductor chip as recited in claim 23, wherein the **gate electrode** of the first transistor of the first transistor type is electrically connected to the gate electrode of the first transistor of the second transistor type.

29. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures formed in part based on corresponding gate structure layout shapes used as an input to a *lithography process*, the gate structure layout shapes positioned in accordance with a **gate horizontal grid** that includes at least seven **gate gridlines**, each gate structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, each gate gridline having at least one gate structure layout shape positioned thereon, wherein adjacently positioned ones of the gate structures are separated from each other by a **gate pitch** of less than or equal to about 193 nanometers, each of the gate structures having a width of less than or equal to about 45 nanometers, wherein each pair of the gate structures that are positioned in an end-to-end manner are separated from each other by a line end-to-line end gap of less than or equal to about 193 nanometers, wherein at least one gate structure within

the region is a first-transistor-type-only gate structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region,

wherein each gate structure that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding **contact structure** formed in part based on a corresponding contact structure layout shape having a substantially rectangular shape, wherein each contact structure that contacts a given gate structure that forms any transistor gate electrode does not contact another gate structure, wherein each contact structure layout shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in an x-direction, wherein each contact structure that contacts a corresponding gate structure has its corresponding contact structure layout shape positioned to overlap at least one edge of the gate structure layout shape of the corresponding gate structure,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-

only gate structure within the region is included within the portion of the multiplexer or the portion of the latch.

30. A semiconductor chip, comprising:

gate structures formed within a region of the semiconductor chip, the gate structures formed in part based on corresponding gate structure layout shapes used as an input to a *lithography process*, the gate structure layout shapes positioned in accordance with a **gate horizontal grid** that includes a number of **gate gridlines**, each gate structure layout shape having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, each gate gridline having at least one gate structure layout shape positioned thereon, wherein adjacently positioned ones of the gate structures are separated from each other by a **gate pitch** of less than or equal to about 193 nanometers, each of the gate structures having a width of less than or equal to about 45 nanometers, wherein each pair of the gate structures that are positioned in an end-to-end manner are separated from each other by a line end-to-line end gap of less than or equal to about 193 nanometers, wherein at least one gate structure within the region is a first-transistor-type-only gate structure that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate structure within the region is a second-transistor-type-only gate structure that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type, wherein a total number of first-transistor-type-only gate structures within the region is equal to a total number of second-transistor-type-only gate structures within the region,

wherein each of at least six gate structures within the region has a respective top surface in physical and electrical contact with a corresponding at least six **contact structures** that are formed in part based on corresponding contact structure layout shapes having a substantially rectangular shape, wherein each of the at least six contact structures is in physical contact with only one corresponding gate structure, wherein each contact structure layout shape of the at least six contact structures is centered in an x-direction on the gate structure layout shape of the gate structure with which it physical contacts, wherein each contact structure layout shape of the at least six contact structures has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in an x-direction, wherein each contact structure of the at least six contact structures has its contact structure layout shape positioned to overlap at least one edge of the gate structure layout shape of the gate structure that is contacted by the contact structure,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least one first-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch, wherein at least one second-transistor-type-only gate structure within the region is included within the portion of the multiplexer or the portion of the latch.

The '523 patent has 28 claims. As of the date of this order, claims 1-12, 14-20, 22-24, and 26-28 are asserted in this investigation, either as infringed or under the domestic industry technical

prong.⁵ The asserted claims read as follows (with the first instance of the agreed-upon terms in italics and the first instance of the disputed terms highlighted in bold):

1. A semiconductor chip, comprising:

gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to *a lithography process*, the gate electrode feature layout shapes positioned in accordance with a **gate horizontal grid** that includes at least seven **gate gridlines**, wherein all gate gridlines extend in a y-direction, wherein adjacent gate gridlines are separated from each other by a **gate pitch**, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

at least six **gate contact structures** formed within the region of the semiconductor chip, the at least six gate contact structures formed in part utilizing

⁵ Claim 25 is not listed as asserted in the Notice of Investigation, 84 Fed. Reg. 9559, but it is implicated by dependent claim 26, which is asserted.

corresponding at least six gate contact structure layout shapes as an input to a lithography process, wherein at least six gate electrode features within the region have a respective top surface in physical and electrical contact with a corresponding one of the at least six gate contact structures, each of the at least six gate contact structure layout shapes having a substantially rectangular shape with a corresponding length greater than a corresponding width and with the corresponding length oriented in an x-direction, each of the at least six gate contact structure layout shapes positioned and sized to overlap both edges of the gate electrode feature layout shape corresponding to the gate electrode feature to which it is in physical and electrical contact; and

a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material, wherein the first-metal layer includes first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, wherein the first-metal structure layout shapes are positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, wherein all first-metal gridlines extend in the x-direction, wherein at least eight of the at least eight first-metal gridlines have at least one first-metal structure layout shape positioned thereon, each first-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner on an associated first-metal gridline,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form part of a logic circuit, wherein electrical connections within the logic circuit collectively include at least five first-metal structures corresponding to at least five first-metal structure layout shapes respectively positioned on at least five different first-metal gridlines,

wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein some diffusion regions within the region of the semiconductor chip are physically and electrically contacted by at least one diffusion contact structure, the at least one diffusion contact structure formed in part utilizing corresponding at least one diffusion contact structure layout shape as an input to a lithography process, each diffusion contact structure layout shape within the region positioned in a substantially centered manner along an associated diffusion contact gridline of a diffusion contact grid, the diffusion contact grid having a diffusion contact gridline-to-diffusion contact gridline spacing measured in the x-direction equal to the gate pitch.

2. The semiconductor chip as recited in claim 1, further comprising:

a second-metal layer formed above the first-metal layer within the region of the semiconductor chip, the second-metal layer positioned second in the stack of metal layers counting upward from top surfaces of the **gate electrode features**, the second-metal layer separated from the first-metal layer by at least one insulator material, the second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to a *lithography process*, the second-metal layer layout shapes positioned in accordance

with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, wherein all second-metal gridlines extend in the y-direction, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, each second-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline,

wherein some second-metal structures within the region are electrically connected to at least one first-metal structure within the region through at least one first-metal-to-second-metal via structure, each first-metal-to-second-metal via structure within the region formed in part based on corresponding first-metal-to-second-metal via structure layout shape used as an input to a lithography process, each first-metal-to-second-metal via structure layout shape within the region positioned in a substantially centered manner along an associated second-metal gridline.

3. The semiconductor chip as recited in claim 2, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is either a first width or a second width, the second width different than the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal layout shape that has the second width.

4. The semiconductor chip as recited in claim 3, wherein at least one **gate electrode feature** within the region that forms at least one gate electrode of at least one transistor of the first transistor type and does not form a gate electrode of a transistor of the second

transistor type is electrically connected to at least one gate electrode feature within the region that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type through an electrical connection that includes at least one first-metal structure and at least one second-metal structure.

5. The semiconductor chip as recited in claim 2, wherein the at least six **gate contact structure** layout shapes are positioned in accordance with a **contact vertical grid**, the contact vertical grid including **contact gridlines** extending in the x-direction, each of the at least six gate contact structure layout shapes positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated contact gridline, and at least two of the at least six gate contact structure layout shapes positioned to also extend lengthwise in the x-direction in a substantially centered manner along a corresponding first-metal gridline.

6. The semiconductor chip as recited in claim 2, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is one of a plurality of widths, the plurality of widths including a first width and a second width, the first width smaller than the second width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the second width, wherein each first-metal-to-second-metal via structure that contacts a first-metal structure formed in part by a first-metal structure layout shape having the first width is formed at least in part by a first-metal-to-second-metal via structure layout shape that is intersected by a corresponding **first-metal gridline**.

7. The semiconductor chip as recited in claim 6, wherein each first-metal-to-second-metal via structure layout shape is intersected by a corresponding **first-metal gridline**.
8. The semiconductor chip as recited in claim 2, wherein adjacent **second-metal gridlines** are separated from each other by a second-metal pitch, the second-metal pitch equal to the **gate pitch**, the **second-metal horizontal grid** aligned with the diffusion contact grid.
9. The semiconductor chip as recited in claim 8, wherein all second-metal structure layout shapes in the region of the semiconductor chip have a same width as measured in the x-direction.
10. The semiconductor chip as recited in claim 9, further comprising:
 - a third-metal layer formed above the second-metal layer within the region of the semiconductor chip, the third-metal layer positioned third in the stack of metal layers counting upward from top surfaces of the **gate electrode features**, the third-metal layer separated from the second-metal layer by at least one insulator material, the third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a *lithography process*, the third-metal layer layout shapes positioned in accordance with a **third-metal vertical grid**, the third-metal vertical grid including at least eight **third-metal gridlines**, wherein all third-metal gridlines extend in the x-direction, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, each third-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline,

wherein some third-metal structures within the region are electrically connected to at least one second-metal structure within the region through at least one second-metal-to-third-metal via structure, each second-metal-to-third-metal via structure within the region formed in part based on corresponding second-metal-to-third-metal via structure layout shape used as an input to a lithography process, wherein at least one second-metal-to-third-metal via structure layout shape within the region is positioned in a substantially centered manner along an associated third-metal gridline.

11. The semiconductor chip as recited in claim 10, wherein each second-metal-to-third-metal via structure layout shape is intersected by a corresponding **second-metal gridline**.

12. The semiconductor chip as recited in claim 10, wherein each second-metal structure layout shape in the region is positioned next to at least one other second-metal structure layout shape on a first side at a second-metal pitch and is positioned next to at least one other second-metal structure layout shape on a second side at the second-metal pitch, wherein the second-metal pitch is measured in the x-direction and is equal to the **gate pitch**.

14. The semiconductor chip as recited in claim 1, wherein at least one of the at least six **gate contact structures** is in physical and electrical contact with, and is substantially centered in the x-direction on, a **gate electrode feature** within the region that forms at least one gate electrode of at least one transistor of the first transistor type and that does not form a gate electrode of a transistor of the second transistor type.

15. The semiconductor chip as recited in claim 1, wherein each of the at least six **gate contact structure** layout shapes is intersected by a corresponding **gate gridline**.

16. The semiconductor chip as recited in claim 1, wherein the first-metal layer includes at least eight first-metal structure layout shapes positioned on four **first-metal layer**

gridlines such that a different two of the at least eight first-metal structure layout shapes is positioned on each of the four first-metal layer gridlines, wherein each of the at least eight first-metal structure layout shapes is positioned next to and spaced apart from at least one other first-metal structure layout shape at a first-metal pitch.

17. The semiconductor chip as recited in claim 1, wherein the at least eight of the at least eight **first-metal gridlines** that have at least one first-metal structure layout shape positioned thereon are spaced at a first-metal pitch.

18. The semiconductor chip as recited in claim 1, further comprising:

a second-metal layer formed above the first-metal layer within the region of the semiconductor chip, the second-metal layer positioned second in the stack of metal layers counting upward from top surfaces of the **gate electrode features**, the second-metal layer separated from the first-metal layer by at least one insulator material, the second-metal layer including second-metal structures formed in part based on corresponding second-metal structure layout shapes used as an input to a *lithography process*, the second-metal structure layout shapes positioned in accordance with a **second-metal horizontal grid**, the second-metal horizontal grid including at least eight **second-metal gridlines**, wherein all second-metal gridlines extend in the y-direction, wherein at least eight of the at least eight second-metal gridlines have at least one second-metal structure layout shape positioned thereon, each second-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the y-direction in a substantially centered manner along an associated second-metal gridline; and

a third-metal layer formed above the second-metal layer within the region of the semiconductor chip, the third-metal layer positioned third in the stack of metal

layers counting upward from top surfaces of the gate electrode features, the third-metal layer separated from the second-metal layer by at least one insulator material, the third-metal layer including third-metal structures formed in part based on corresponding third-metal structure layout shapes used as an input to a lithography process, the third-metal structure layout shapes positioned in accordance with a third-metal vertical grid, the third-metal vertical grid including at least eight third-metal gridlines, wherein all third-metal gridlines extend in the x-direction, wherein at least eight of the at least eight third-metal gridlines have at least one third-metal structure layout shape positioned thereon, each third-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in the x-direction in a substantially centered manner along an associated third-metal gridline.

19. The semiconductor chip as recited in claim 18, wherein each first-metal structure layout shape in the region has a width measured in the y-direction that is one of a plurality of widths, the plurality of widths including a first width and a second width, the first width smaller than the second width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the first width, the first-metal layer including at least one first-metal structure formed in part by a first-metal structure layout shape that has the second width, wherein each first-metal-to-second-metal via structure that contacts a first-metal structure formed in part by a first-metal structure layout shape having the first width is formed at least in part by a first-metal-to-second-metal via structure layout shape that is intersected by a corresponding **first-metal gridline**.

20. The semiconductor chip as recited in claim 18, wherein some third-metal structures within the region are electrically connected to at least one second-metal structure within the

region through at least one second-metal-to-third-metal via structure, each second-metal-to-third-metal via structure formed at least in part by a second-metal-to-third-metal via structure layout shape that is intersected by a corresponding **second-metal gridline**.

22. The semiconductor chip as recited in claim 18, wherein the at least four transistors of the first transistor type include a first transistor of the first transistor type, wherein the at least four transistors of the second transistor type include a first transistor of the second transistor type, wherein a **gate electrode feature** layout shape used to form a gate electrode feature that forms a gate electrode of the first transistor of the first transistor type and a gate electrode feature layout shape used to form a gate electrode feature that forms a gate electrode of the first transistor of the second transistor type are positioned to extend lengthwise along a same **gate gridline**, wherein no other transistor is positioned on the same gate gridline between the gate electrode feature layout shapes used to form the gate electrode features that form the gate electrodes of the first transistor of the first transistor type and the first transistor of the second transistor type,

wherein each transistor within the region of the semiconductor chip is formed in part by a corresponding **diffusion region**, wherein a diffusion region of the first transistor of the first transistor type is electrically connected to a diffusion region of the first transistor of the second transistor type,

wherein the at least six **gate contact structure** layout shapes include a gate contact structure layout shape substantially centered in the x-direction on the same gate gridline at a location between the diffusion regions of the first transistor of the first transistor type and the first transistor of the second transistor type,

wherein an electrical connection between the diffusion region of the first transistor of the first transistor type and the diffusion region of the first transistor of

the second transistor type includes at least one first-metal structure and at least one second-metal structure,

wherein the at least four transistors of the first transistor type and the at least four transistors of the second transistor type within the region collectively form part of an inverting two-to-one multiplexer.

23. The semiconductor chip as recited in claim 22, wherein adjacent **second-metal gridlines** are separated from each other by a second-metal pitch, the second-metal pitch equal to the **gate pitch**, the **second-metal horizontal grid** aligned with the diffusion contact grid.

24. The semiconductor chip as recited in claim 23, wherein all second-metal structure layout shapes in the region of the semiconductor chip have a same width as measured in the x-direction.

25. The semiconductor chip as recited in claim 1, wherein the at least four transistors of the first transistor type are collectively separated from the at least four transistors of the second transistor type by an inner region that does not include another transistor.

26. The semiconductor chip as recited in claim 25, wherein at least one of the at least six **gate contact structure** layout shapes is positioned over the inner region and forms a gate contact structure that is in physical and electrical contact with, and is substantially centered in the x-direction on, a **gate electrode feature** within the region that forms at least one gate electrode of at least one transistor.

27. A semiconductor chip, comprising:

gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to a *lithography process*, the gate electrode

feature layout shapes positioned in accordance with a **gate horizontal grid** that includes at least seven **gate gridlines**, wherein adjacent gate gridlines are separated from each other by a **gate pitch**, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

a number of **gate contact structures** formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each gate electrode feature that forms any transistor gate electrode within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape, wherein each gate contact structure that contacts a given gate electrode feature that forms any transistor gate electrode does not contact another gate electrode feature, wherein any gate contact structure layout shape that has a corresponding length greater than or equal

to a corresponding width is oriented to have its corresponding length extend in an x-direction; and

a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material, the first-metal layer including first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process,

wherein each transistor within the region is formed in part by a corresponding **diffusion region**, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape,

wherein the region includes at least four transistors of the first transistor type and at least four transistors of the second transistor type that collectively form a portion of a multiplexer or a portion of a latch, wherein at least two first-metal structures form portions of one or more electrical connections within the multiplexer or the latch.

28. A semiconductor chip, comprising:

gate electrode features formed within a region of the semiconductor chip, the gate electrode features formed in part based on corresponding gate electrode feature layout shapes used as an input to *a lithography process*, the gate electrode

feature layout shapes positioned in accordance with a **gate horizontal grid** that includes a number of **gate gridlines**, wherein adjacent gate gridlines are separated from each other by a **gate pitch**, each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise in a y-direction in a substantially centered manner along an associated gate gridline, wherein each gate gridline has at least one gate electrode feature layout shape positioned thereon, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one **gate electrode** of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type, wherein at least one gate electrode feature layout shape within the region corresponds to a gate electrode feature that forms at least one gate electrode of at least one transistor of the second transistor type and does not form a gate electrode of a transistor of the first transistor type;

a number of **gate contact structures** formed within the region of the semiconductor chip, the gate contact structures formed in part utilizing corresponding gate contact structure layout shapes as an input to a lithography process, wherein each of at least six gate electrode features within the region has a respective top surface in physical and electrical contact with a corresponding gate contact structure formed at least in part from a gate contact structure layout shape having a substantially rectangular shape, wherein each gate contact structure is centered in an x-direction on the gate electrode feature with which it physical contacts, wherein each gate contact structure layout shape that has the substantially rectangular shape has a corresponding length greater than or equal to a corresponding width and is oriented to have its corresponding length extend in the x-direction,

wherein each of the number of gate contact structures is in physical contact with only one of any of the gate electrode features; and

a first-metal layer formed above top surfaces of the gate electrode features within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate electrode features, the first-metal layer separated from the top surfaces of the gate electrode features by at least one insulator material, the first-metal layer including at least two first-metal structures formed in part based on corresponding first-metal structure layout shapes used as an input to a lithography process, the at least two first-metal structures forming portions of one or more electrical connections within the region of the semiconductor chip,

wherein each transistor within the region is formed in part by a corresponding **diffusion region**, each diffusion region formed in part utilizing a corresponding diffusion region layout shape as an input to a lithography process, wherein each diffusion region that forms part of any transistor within the region is formed at least in part by a corresponding diffusion region layout shape that has a substantially rectangular shape.

V. CLAIM CONSTRUCTION

A. Construction of the Agreed-Upon Claim Term

Prior to the *Markman* hearing, the Parties reached agreement regarding the construction of one term in the asserted claims:

Claim Term	Present in Asserted Claims	Agreed Construction
“a lithography process”	’335 Patent at claims 1, 2, 10, 20, 29, 30	Plain and ordinary meaning; <i>i.e.</i> , “a process by which a pattern is imprinted on a resist

	'523 Patent at claims 1, 2, 10, 18, 27, 28	or semiconductor wafer using light as a mask”
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(JC, App’x A at 1.)

B. Construction of the Disputed Claim Terms

1. “linear [conductive segment(s) / conductive structure(s)]”

As shown in the chart below, this term is found in the claim language of the now terminated ’966 and ’012 patents; however, it is not found in the claim language of the remaining Asserted Patents. In its motion to terminate, Tela contends that this term no longer needs to be construed. (EDIS Doc. ID 688619.) Respondents and the Staff, however, contend that the claim language still needs to be construed because the term applies even to the claims of the remaining Asserted Patents. (EDIS Doc. IDs 689665, 689247; see RRMB at 14-15; SMB at 19-22.) The Parties proposed the following constructions:

Relevant Claims	'966 patent at claims 2, 3, 6, 7, 9-12, 21-23, 25-27, 29-30, 32-33 '012 patent at claims 2-4, 6-8, 11-16, 18-21, 23-28, 31-35		
Tela	Respondents	Staff	
<u>linear</u> : “a 3D conductive structure having a rectangular shape of a given width defined in a plane parallel to a top surface of the substrate and defined to have a length that extends in one direction” <u>linear conductive segment / linear conductive structure</u> : No further construction required beyond the construction of “linear.” Plain and ordinary meaning.	<u>linear</u> : “having a consistent vertical cross-section shape and extending in a single direction over the substrate” <u>linear conductive segment(s) / linear conductive structures</u> : no additional construction needed beyond “linear”	“linear-shaped feature(s), in a given layer, that is a 3-D conductive structure characterized as having a consistent vertical cross-section shape and extending straight without bends in a single lengthwise direction over the substrate, and having a 2-D rectangular shape of a given width defined in a plane parallel to a top surface of the substrate”	

(JC, App’x A at 2-4.)

Respondents and the Staff advance five basic arguments for why this term should be read into claims that do not explicitly contain it. First, Respondents and the Staff point out that Tela initially proposed a construction of another claim term (“gate pitch”) which seemingly incorporated this term, but later “renewed from its own construction.” (RIMB at 23; *see* SMB at 20.) This point would be more persuasive had Tela changed its position after the completion of, or in the midst of, briefing on claim construction. Instead, Tela changed its position before it had to commit to a position, and the argument is essentially beside the point.

Second, the Staff correctly observes that the specification emphasizes the importance of all chip features above the diffusion region possessing “linear” shapes. (SMB at 19 (quoting ’523 patent at 10:4-5 (“in each layer other than the diffusion region layer 203, only linear-shaped features are allowed”) (emphasis omitted)).) But there is generally no language in the claims corresponding to “linear,” so it is improper to import that limitation from the specification. Even a large number of references to the importance of linearity—the Staff counts over 50 such references—are not alone enough to justify limiting the claims as the Staff proposes. (SMB at 19-20.) And even assuming that the patentees acted as their own lexicographers, as the Staff contends, that lexicography at most defines the term “linear,” which, again, is not found in the remaining claims in suit. (SMB at 14.)

Third, Respondents argue for the term’s general applicability based on the prosecution history of the ’523 patent, which includes the following statement: “[t]he gate structures are defined as rectangular-shaped, *i.e.*, linear shaped, features extending in a parallel relationship across the dynamic array in the second reference direction (y).” (RIMB at 22 (quoting RIMB, Ex. 18 at 17 (emphasis omitted)).) This argument has two defects. First, even though the ’523 patent shares a specification with the ’334 and ’335 patents, that the patentee’s representation applies to the former patent does not necessarily mean that it also applies to the latter two patents, which both issued

before the '523 patent. Second, the representation appears to be gratuitous; nothing in the prosecution history suggests that it was necessary for allowance, or intended as a disclaimer.

Fourth, Respondents contend that where the remaining claims in suit use the term “rectangular,” that term should be read as “linear.” (RRMB at 14.) Certainly the term “rectangular” is found throughout the claims of the '334, '335, and '523 patents, and applies to various claimed features. (*E.g.*, '523 patent at 24:61 (“gate electrode feature”), 31:15 (“gate contact structure”), 32:56 (“diffusion region layout shape”).) But there is no evidence the patentees acted as their own lexicographers in connection with the term “rectangular,” and as explained above, the prosecution history does not mandate any deviation from the term’s plain and ordinary meaning. Most importantly, even assuming that the term “linear” is defined by the specification—namely, “having a consistent vertical cross-section shape and extending in a single direction over the substrate”—the plain and ordinary meaning of “rectangular” is unquestionably different and simpler. ('523 patent at 10:7-8.)

Fifth, Respondents argue that in a parallel litigation before the United States District Court for the Northern District of California, the court’s tentative claim construction “illustrate[s] that construing ‘linear’ is required to define the scope” of other claim terms. (EDIS Doc. ID 689665 at 2.) But again, there is generally no language in the claims of the remaining Asserted Patents corresponding to “linear,” and in any event the District Court’s claim construction is not binding in this investigation.

Accordingly, “linear [conductive segment(s) / conductive structure(s)]” is not an element of any claim of the remaining Asserted Patents, and is therefore not construed.

2. “gate electrode”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claims 1, 22, 24, 29, 30 '335 patent at claims 1, 22, 24, 29, 30 '523 patent at claims 1, 2, 4, 10, 14, 18-22, 26-28	
Tela	Respondents	Staff
“portion of linear conductive segment ('966 and '012 Patents) /gate structure ('334 and '335 Patents) / gate electrode feature ('523 Patent) used to control the flow of electrical current between the source and drain regions of a transistor”	“a portion of a conductive shape in the gate layer that extends over and parallel with a diffusion region to form a transistor gate”	“portion of a linear-shaped feature in the gate electrode layer that is used to control the flow of electrical current between the source and drain diffusion regions of a transistor”

(JC, App'x A at 5-6.)

References to gates, components of gates, and the structure of gates varies between the Asserted Patents. In the '334 and '335 patents, the claims use the term “gate structure” in reference to an element that, in some instances, forms a “gate electrode.” (*E.g.*, '334 patent at 30:18-19; '335 patent at 31:4.) In the '523 patent, by contrast, the claims use the term “gate electrode feature,” seemingly in reference to the same element, because it “forms at least one gate electrode.” (*E.g.*, '523 patent at 24:67-25:1.) The specification uses the terms “gate electrode” and “gate electrode feature,” as well as “gate electrode track,” but not “gate structure.” (*E.g.*, '523 patent at 9:43-45 (“gate electrode features 207 are defined above the diffusion regions 203 to form transistor gates”); 15:9-12 (“the gate electrode tracks extend over the substrate . . . the gate electrodes may extend through the boundaries at the top and bottom of the cells”).)

The Parties apparently agree, at least implicitly, that “gate structure” and “gate electrode feature” are synonymous, and this is supported by the intrinsic evidence. (CIMB at 24; RIMB at 21; SMB at 22 & n.11.) Although a gate is made of two parts, a metal and an oxide, and the oxide necessarily is not itself an electrode (because it does not conduct electricity), both the metal part of

the gate alone and the metal/oxide combination could be considered electrodes. (*See* Tutorial at 11-13.) So I find that the terms “gate electrode feature,” “gate structure,” and “gate electrode track” all refer to the same structure, which for present purposes I call the “gate electrode feature.”

So understood, the parties further agree that for a “gate electrode feature” to carry out its principal function, that is, to form a transistor gate, at least a portion of it must extend over a diffusion region and control the current flowing between the source and drain. (CIMB at 28-29; RIMB at 26; SMB at 27.) This is supported by the specification. (’523 patent at 9:43-45 (“gate electrode features 207 are defined above the diffusion regions 203 to form transistor gates).) So a “gate electrode” is simply that portion of a “gate electrode feature” which actually forms a transistor gate; it is redundant to add limitations concerning source, drain, and diffusion region.

Respondents and the Staff urge a construction limiting the “gate electrode” to a particular shape—for Respondents, a conductive shape, and for the Staff, a linear shape. Respondents also argue for a construction limiting the “gate electrode” to a “gate layer” parallel with the diffusion region. And the Staff advances a construction limiting the “gate electrode” to a gate electrode layer.

These requirements are inappropriate because they are not even arguably within the plain and ordinary meaning of a “gate electrode.” Although the specification refers to a “gate electrode layer,” nothing in the claim language suggests that the “gate electrode” is limited to such a layer. (’523 patent at 14:20.) The term “gate layer” is mentioned nowhere in the intrinsic evidence, and the term is therefore ambiguous. And the term “linear” does not apply to “gate electrode,” nor does the claim language suggest that a “gate electrode” must be some other shape.

Accordingly, “gate electrode” is construed as “that portion of a gate electrode feature that forms a transistor gate.”

3. “gate electrode feature(s) / gate structure(s)”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claims 1, 2, 4, 10, 20, 22, 29, 30	
	'335 patent at claims 1, 2, 4, 10, 20, 22, 29, 30	
	'523 patent at claims 1, 2, 4, 10, 14, 18, 22, 26-28	
Tela	Respondents	Staff
“feature that can form a gate(s) of a transistor(s) defined below the gate contact”	“linear-shaped feature comprising a gate(s) of a transistor(s) or a dummy gate”	“linear-shaped feature that can form a gate(s) of a transistor(s) defined below the gate contact layer”

(JC, App’x A at 4-5.)

As reflected in the table above, and as stated by Tela, the principal interpretive dispute “appears to be whether the claimed ‘gate electrode feature’ and ‘gate structure’ require a ‘linear-shaped feature’ as interpreted by Respondents and Staff.” (CIMB at 24.) As explained above, the term is inapplicable.

Tela and the Staff further contend that the “gate electrode features” and “gate structures” must be below the “gate contact” or “gate contact layer.” Tela justifies this limitation in light of claim language requiring it. (See CIMB at 25-26 (citing ’523 patent at cl. 1; ’334 patent at cl.1; ’335 patent at cl. 1)) and Figure 2 of the ’334, ’335, and ’523 patents (*see id.* at 26 (citing ’334 patent at Fig. 2).) The Staff justifies the limitation by reference to Figure 2 of the specification. (SMB at 23.) I disagree that these details should be part of the construction primarily because, as Tela acknowledges, the presence of electrode contacts positioned above the “gate electrode features” or “gate structures” is already recited in the claims. (See CIMB at 25-26.) To place it within the construction of “gate electrode features” or “gate structures” is therefore redundant. Moreover, it is improper to import a limitation from the specification (such as that shown in Figure 2) into the

claims without better support for that importation. *Kara Tech. Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009) (“The patentee is entitled to the full scope of his claims, and we will not limit him to his preferred embodiment or import a limitation from the specification into the claims.”).

Lastly, the Parties dispute the proper method for capturing the fact that a “gate electrode feature” or “gate structure” does not necessarily have to act as a transistor gate at every, or even any, point along its length. For example, “Respondents’ construction recites that the claimed feature comprises a gate or a dummy gate; Tela and Staff appear to attempt to capture the same concept using the language ‘can form a gate.’” (RIMB at 21.) The construction of “gate electrode” is helpful here. As noted, a “gate electrode” is “that portion of a gate electrode feature that forms a transistor gate.” It follows that a “gate electrode feature” that does not form a transistor gate at any point along its length is a dummy gate, that is, one that is designed to form a gate but does not.

It further follows that a feature or structure that forms a transistor gate over some but not all of its length is a feature that “can form” a transistor gate, and does, as Tela and the Staff contend. Respondents’ proposed construction, by using the term of art “comprising,” succinctly characterizes this aspect of the element. (RIMB at 24.) Specifically, a feature that “comprises a transistor gate” is a feature that forms a transistor gate over at least some of its length.

However, in light of the withdrawal of the ’966 and ’012 patents, the definition of a dummy gate is otherwise moot. The ’966 and ’012 patents include claims covering dummy gates, that is, gate electrode features that do not form a transistor gate any point along their lengths. (’966 patent at 27:66-67; ’012 patent at 33:19-20.) The ’334, ’335, and ’523 patents do not, however; every claim of these patents reciting the limitation “gate electrode feature that . . . does not form a gate electrode” is accompanied by the limitation “forms at least one gate electrode” of the other transistor type. For instance, claim 1 of the ’523 patent recites: “a gate electrode feature that forms at least

one gate electrode of at least one transistor of a first transistor type and does not form a gate electrode of a transistor of a second transistor type.” (’523 patent at 24:67-25:3.) Therefore, every claimed “gate electrode feature” in suit that can form a transistor gate actually does, and the dispute over how to precisely define a “gate electrode feature” that does not form a transistor gate at all need not be resolved.

Accordingly, a “gate electrode feature” or “gate structure” is construed as a “feature comprising a transistor gate.”

4. “diffusion region(s)”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	’334 patent at claims 15, 22, 23, 29, 30 ’335 patent at claims 15, 22, 23 ’523 patent at claims 1, 22, 27, 28		
Tela	Respondents	Staff	
“selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor”	“selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor”	“selected portion(s) defined in the base substrate located below the gate electrode layer within which impurities are introduced in order to form the source and/or drain of a transistor”	

(JC, App’x A at 10-12.)

As shown in the above table, Tela and the Respondents agree on this term, with the Staff offering a modified construction that adds two requirements: (1) the referenced substrate is the “base” substrate; and (2) such substrate is below the gate electrode layer. The Staff supports adding these details because the specification states that “[d]iffusion regions 203 are defined in the base substrate 201,” and “gate electrode features 207 are defined above the diffusion regions 203 to form

transistor gates.” (’523 patent at 9:33-45.) But calling the substrate “base” is redundant; there is only one substrate, so it is necessarily the “base substrate.” And the term “diffusion region” by itself is not accompanied in the claims by any particular layer requirement, so there is no reason to import such a requirement from the specification into the claims. The remaining proposed construction is otherwise supported by the specification and sufficiently tied to the plain and ordinary meanings of “diffusion” and “region.” (’523 patent at 9:35-42 (“diffusion regions 203 represent selected regions of the base substrate 201 within which impurities are introduced” and “diffusion contacts 205 are defined to enable connection between source and drain diffusion regions 203”).)

Accordingly, “diffusion region(s)” is construed as “selected portions of the substrate within which impurities have been introduced to form the source or drain of a transistor.”

5. “[gate horizontal / first-metal vertical grid]; [second-metal horizontal] grid; [contact vertical] grid; [third-metal vertical] grid; [diffusion contact] grid”

The Parties disagree on the proper claim construction and have proposed the following constructions:

<p>Relevant Claims</p>	<p>’334 patent at claims 1, 2, 5, 10, 20, 22, 29, 30</p> <p>’335 patent at claims 1, 2, 5, 10, 20, 29, 30</p> <p>’523 patent at claims 1, 2, 5-8, 10, 11, 15-20, 22, 23, 27, 28</p>	
<p>Tela</p> <p><i>grid</i>: “virtual projected gridlines along which [gate / metal / contact] features are defined”</p>	<p>Respondents</p> <p>“projected grid used during fabrication of a given layer along which [gate / metal / contact] linear-shaped features are formed”</p>	<p>Staff</p> <p>“projected grid used during fabrication of a given layer along which [gate / metal / contact] linear-shaped features are formed”</p>

(JC, App’x A at 12-13.)

As reflected in the table above, one of the Parties' disputes over the term "grid," with its various modifiers, again concerns the requirement of "linear-shaped features." And again, the limitation is inapplicable.

A second dispute is over how the grid must be "projected," although the Parties agree that such a projection is required. The Staff argues that the grid is "an actual projection of a grid," while Tela argues that the grid projection is virtual. (SMB at 37 (emphasis omitted); CIMB at 40; CRMB at 20.) The Staff cites one passage of the specification: "the base grid is projected in a substantially consistent manner with respect to position on each layer of the dynamic array, thus facilitating accurate feature stacking and alignment." (*Id.* at 37-38 (citing '334 patent at 13:9-13).) But in the preceding sentence the specification makes clear that the grid is "not physically defined as part of the dynamic array," and instead "can be considered as a projection on each layer of the dynamic array." ('334 patent at 13:7-9.) It may be true that, just as a "movie projected on a screen is not physically a part of the screen," an actual projection of a grid during fabrication is also not physically part of the dynamic array, but this observation from Respondents sheds no light on whether the specification requires an actual projection. (RRMB at 23.)

More to the point, it is what the claims require that controls here, but the claims do not even require a projection, actual or virtual. And in the '335 and '523 patents, where "grid" is used, the claims typically refer to "layout," and in many instances to "layout shapes used as an input to a lithography process." (*E.g.*, '335 patent at 30:5-6; '523 patent at 24:54-56.) The term "layout" by itself, and especially combined with "input to a lithography process," suggests that if the grid is "projected" if at all, it is not actually projected onto a wafer. (*See* '523 patent at 8:8-9 ("addition of margin in the set of design rules assists with the layout portions").) The claims of the '334 patent are even less specific, because they typically refer to "gate structures positioned in accordance with a . . . grid," with no limitation on how that is achieved. (*E.g.*, '334 patent at 30:4-5.)

In short, the claims (as opposed to the specification) do not require projection of a “grid” and do not require such projection to be either virtual or actual. Nonetheless, because the Parties agree that the “grid” is projected, and this requirement is supported by the specification, it will be incorporated into the term’s construction. (’523 patent at 11:18-19 (“the base grid can be considered as a projection on each layer of the dynamic array”).)

The third dispute between the Parties pertains to when the grid is used, specifically, whether during design or fabrication; this dispute overlaps with the Parties’ dispute over the construction of “gridline(s).” (RIMB at 41 (“[t]he first dispute (formed vs. defined) is addressed below in the context of the ‘gridlines’ term”); CRMB at 22.) Nothing in the claim language explicitly addresses this issue, but again, in the ’335 and ’523 patents, where “grid” is used the claims typically refer to “layout,” and in many instances to “layout shapes used as an input to a lithography process,” where the “layout shapes are positioned in accordance with a . . . grid.” (*E.g.*, ’335 patent at 30:5-8; ’523 patent at 24:54-56.) The various features are then “formed in part based on [the] layout shapes.” (*E.g.*, ’335 patent at 30:4-5; ’523 patent at 24:52-54.) That the claims require positioning the shapes, as opposed to the features, and then forming the features based on the shapes, implies that the “grid” is used during the layout process, that is, before fabrication. This is consistent with the layout stage of integrated circuit manufacturing described by Respondents’ expert. (*See* RIMB, Ex. 6 at 6 (“A layout represents the size, shape, and spacing guidelines for a given layer in a transistor”); *see also* Comp. Tutorial at 2 (describing “Layout & Simulation” as occurring before “Fabrication & Verification”).) Nothing in the claim language, however, bars the grid from also being used during fabrication or any other stage in the manufacturing process.

In the ’334 patent, by contrast, the claims do not include the word “layout” at all. Instead, the various claimed “structures” must be “positioned,” either “in accordance with a . . . grid,” or “on . . . gridlines,” or “along a . . . gridline.” (*E.g.*, ’334 patent at 30:4-5, 31:4-5, 31:43-48.) As

Respondents point out, the prosecution history is to similar effect. (RIMB at 43-44 (quoting RIMB, Ex. 20 at 24).) In response, Tela argues that formation of a structure is not the same as placement, or positioning of shapes. (CRMB at 21-22.) I disagree. “Positioning” a “structure,” as opposed to a shape, is most naturally understood as building or forming a structure in a particular location. Therefore, in the ’334 patent the “grid” is used, that is, projected, during fabrication. Nothing in the claim language bars the grid from also being used during layout or any other stage of the manufacturing process, however.

Lastly, the parties do not dispute the meaning of “grid” beyond these three disagreements, so the term will not otherwise be construed.

Accordingly, for the ’335 and ’523 patents, “grid” is construed as “projected gridlines used at least during the layout stage of integrated circuit manufacturing,” and for the ’334 patent, “grid” is construed as “projected gridlines used at least during the fabrication stage of integrated circuit manufacturing.”

6. “[gate / metal / contact] gridline(s)”

The Parties disagree on the proper claim construction and have proposed the following constructions:

<p>Relevant Claims</p>	<p>’334 patent at claims 1, 2, 5, 10, 20, 22, 29, 30</p> <p>’335 patent at claims 1, 2, 5, 10, 20, 29, 30</p> <p>’523 patent at claims 1, 2, 5-8, 10, 11, 15-20, 22, 23, 27, 28</p>	
<p>Tela</p> <p>“virtual projected lines along which [gate/metal/contact] features are defined”</p>	<p>Respondents</p> <p>“gridline(s) along which [gate / metal / contact] structures are formed”</p>	<p>Staff</p> <p>“projected lines on a corresponding grid used during fabrication along which [gate / metal / contact] linear-shaped features are formed”</p>

(JC, App'x A at 13-14.)

All of the Parties' disputes over this term are addressed above, in construing the term "grid." The plain and ordinary meaning of "gridline" is otherwise simply one of the lines making up a "grid."

Accordingly, "gridline" is construed as "one of the lines making up a grid."

7. "contact structure(s) / gate contact structure(s)"

The Parties disagree on the proper claim construction and have proposed the following constructions:

<p>Relevant Claims</p>	<p>'334 patent at claims 1, 5, 22, 29, 30</p> <p>'335 patent at claims 1, 5, 22, 29, 30</p> <p>'523 patent at claims 1, 5, 14, 15, 22, 26-28</p>	
<p>Tela</p> <p>"a structure that passes through an insulator to enable connection of the gate electrode feature to the overlying metal conduction lines"</p>	<p>Respondents</p> <p>"linear conductive structure(s) in a gate contact layer above and separate from the gate layer and below and separate from interconnect layers"</p>	<p>Staff</p> <p>"linear-shaped feature, separate from a gate electrode feature, that enables connection of the gate electrode feature to the overlying metal conduction lines, where the linear-shaped feature is oversized in the direction perpendicular to the gate electrode feature and is located above the gate electrode layer"</p>

(JC, App'x A at 7-9.)

As with the other disputed claim terms, to the extent a "contact structure" or "gate contact structure" must be linear, the limitation is inapplicable. In any event, these features are less likely to possess the "linear-shaped" limitation because the claim language defines their shapes.

(*E.g.*, '334 patent at 30:59-64 (“a substantially rectangular shape . . . positioned and sized to overlap both edges” of the associated gate structure); '532 patent at 25:19-24 (same).)

Indeed, the claim language is generally inconsistent with all three proposed constructions. For example, nothing in the claim language requires passage through an insulator, as Tela proposes. The only insulator-related limitation in the claims relevant to these claim terms is that the first-metal layer must be “separated from the top surfaces of the gate electrode features by at least one insulator material.” ('523 patent at 25:31-33; *see* '335 patent at 30:27-29.) And the function of a “contact structure” is to connect a gate and the overlying metal conduction lines, as both Tela and the Staff indicate in their proposed constructions, but neither that function nor a structure that would perform that function is recited in the claim language. The Staff’s proposed limitation that the “contact structure” be “oversized” is already captured by the “overlap both edges” language, and therefore redundant. ('335 patent at 30:61; '532 patent at 25:23-24.) The limitation proposed by Respondents and the Staff, that the “contact structure” be “in a gate contact layer” or “located above the gate electrode layer” is already captured by the requirement that the “top surface” of the “gate electrode features” be “in physical and electrical contact” with the “contact structures,” and is also redundant. ('532 patent at 25:14-18; *see* '335 patent at 30:60-63 (the “contact structure” must “overlap both edges of the top surface”).)

Accordingly, because none of the Parties’ proposed constructions are supported by the claim language, I decline to construe the term “contact structure” or “gate contact structure” at present.

8. “gate pitch”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claims 1, 6, 11, 29, 30 '335 patent at claims 1, 6, 11, 29, 30
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	'523 patent at claims 1, 8, 12, 23, 27, 28	
Tela	Respondents	Staff
“center-to-center separation distance between adjacent gate features”	“center-to-center separation distance between adjacent linear-shaped gate features”	“center-to-center separation distance between adjacent linear-shaped gate features”

(JC, App’x A at 15-16.)

The Parties’ proposed constructions are identical, except that Respondents and the Staff add the requirement that the “adjacent . . . gate features” be “linear-shaped.” As noted, this limitation is inapplicable. The proposed construction is otherwise supported by the specification and sufficiently reflects the term’s plain and ordinary meaning. (’523 patent at 8:61 (“pitch” refers to “layout feature spacing”); 17:52 (“pitch (center-to-center spacing)”)).

Accordingly, “gate pitch” is construed as “center-to-center separation distance between adjacent gate features.”

9. “each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers”

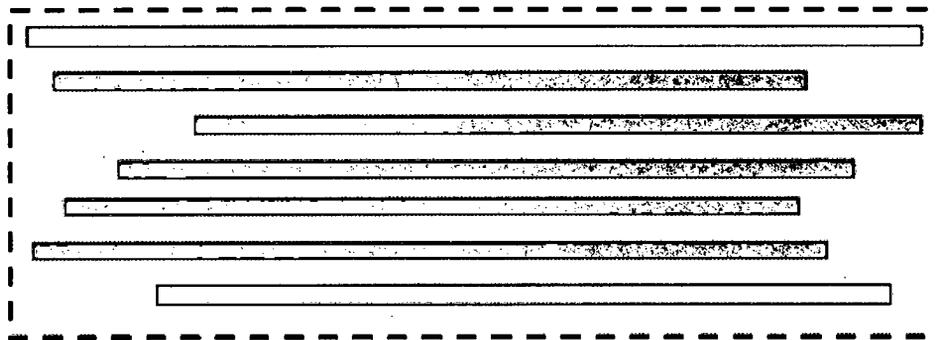
The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claim 1 '335 patent at claim 1	
Tela	Respondents	Staff
Plain and ordinary meaning.	Indefinite.	Indefinite.

(JC, App’x A at 16-17.)

Unlike the previous terms, here, Respondents and the Staff contend the limitation “each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers” is

indefinite because one of ordinary skill in the art would not be able to ascertain its scope with reasonable certainty. (RIMB at 49 (citing *Nautilus*, 572 U.S. at 910); SIMB at 42-43.) Central to this claim are two premises: (1) that “*all* of the first-metal structures in the region have adjacent first-metal structures on *both* of their sides”; but (2) “there are necessarily two first-metal structures—at the edges of the region—that only have another first-metal structure adjacent to *one* of their sides.” (RIMB at 49 (emphasis in original); *see* SMB at 44-45.) Respondents reason, “each first-metal structure in the region has at least one adjacent first-metal structure positioned next to each of its sides’ is thus seemingly impossible to satisfy.” (Id. at 49-50; *see* SMB at 44-45.) Respondents use the following demonstrative to show this point, explaining “blue shapes have shapes next to both of their sides; but the yellow highlighted shapes at the edge of the region cannot”:



(RIMB at 49-50.)

Respondents’ logic actually require a third, unspoken premise—that the “adjacent first-metal structure(s)” recited in the limitation (shown in yellow above) must also be in the “region.” Importantly, this premise distinguishes claim 1 of the ’335 patent from claim 1 of the ’334 patent.

The introduction of the “region” claim term, and “first-metal layer” term, along with the full limitation at issue here reads:

1. A semiconductor chip, comprising:
gate structures formed within *a region* of the semiconductor chip

.....

a first-metal layer formed above top surfaces of the gate structures within the region of the semiconductor chip, the first-metal layer positioned first in a stack of metal layers counting upward from top surfaces of the gate structures, the first-metal layer separated from the top surfaces of the gate structures by at least one insulator material, adjacent metal layers in the stack of metal layers separated by at least one insulator material, wherein the first-metal layer includes first-metal structures positioned in accordance with a first-metal vertical grid, the first-metal vertical grid including at least eight first-metal gridlines, each first-metal structure in the region having a substantially rectangular shape and positioned to extend lengthwise in an x-direction in a substantially centered manner on an associated first-metal gridline, each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers, wherein each pair of first-metal structures that are positioned in an end-to-end manner are separated by a line end-to-line end gap of less than or equal to about 193 nanometers; and

(’334 patent at cl. 1 (emphasis added); see ’335 patent at cl. 1.) As recited in this excerpt, the term “region” is not itself specified as beginning or ending at any point. It merely denotes some subsection or portion of the overall “semiconductor chip.” As additionally recited, there are “gate structures” within this region, but the “first-metal layer” is not recited as existing entirely within the region—all that is stated is that the layer is “formed above the top surfaces” of those gate structures (which happen to exist within the unspecified “region”).

Thus, when claim 1 of the ’334 patent and claim 1 of the ’335 patent later introduce “wherein the first-metal layer includes first-metal structures,” there is no reason to understand these first-metal structures as necessarily being within the “region.” They are simply part of the “first-metal layer” which itself is so far only defined as existing “above the top surfaces” of the gate electrodes within the region. Therefore, at this point in the claim language, the recited “first metal structures” may be inside or outside the “region.” Contrary to the contentions of Respondents and the Staff, there is no further language requiring all “first-metal structures” to be within the “region.” Rather,

the claim only recites “*each* first-metal structure in the region.” (’334 patent at cl. 1 (emphasis added).) I understand this language to simply mean that at least one first-metal structure must be in the region.

The challenged limitation—“each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides”—actually only exists in claim 1 of the ’334 patent. The similar phrasing in claim 1 of the ’335 patent importantly leaves out “in the region”:

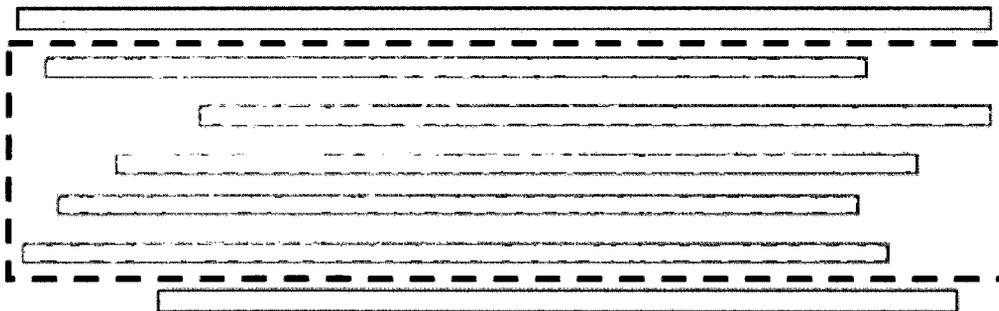
each first-metal structure *in the region* having at least one adjacent first-metal structure positioned next to each of its sides

(’334 patent at cl. 1);

each of the first-metal structures having at least one adjacent first-metal structure positioned next to each of its sides

(’335 patent at cl. 1). Thus, these limitations must be evaluated separately.

The most natural reading of “in the region” is that only those first-metal structures “in the region” must have additional first-metal structures on either side. Additional structures may themselves be outside of the region, and need not have adjacent structures next to both sides. This point can be illustrated with a modified version of Respondents’ demonstrative, again using blue for first-metal structures in the “region” and yellow for first-metal structures which are not in the “region”:



There is nothing incompatible with this reading and the intrinsic evidence, nor with *Apple Inc. v. Samsung Elecs. Co.*, 695 F.3d 1370, 1378 (Fed. Cir. 2012) cited by Respondents and the Staff (*see* RIMB at 49; SMB at 44), as the “each” in “each first-metal structure in the region having at least one adjacent . . .” is fully honored. Respondents and the Staff have pointed to no intrinsic evidence to show otherwise. (*See* RIMB at 49-50; RRMB at 25-26; SMB at 42-47.)

Accordingly, for the limitation as found in claim 1 of the ’334 patent, I find “each first-metal structure in the region having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers” is not indefinite. And because there is otherwise no dispute over the limitation, I further find that it possesses its plain and ordinary meaning.

However, the challenged limitation as it appears in the ’335 patent does not use the “in the region” modifier. All first-metal structures, regardless of their location as inside or outside the “region,” must necessarily have additional first-metal structures on either side. For the exact reasons explained by Respondents and the Staff, I find this requirement cannot possibly be met, that is, the outermost first-metal structures cannot have an additional first-metal structure on both sides.

Tela’s argument to the contrary is not persuasive. That argument is rooted in the idea that “the person [of] ordinary skill in the art would understand that this spacing requirement ends at the bounds of the region as illustrated, for example, in Figure 8A.” (CIMB at 48-49 (citing CIMB, Ex. 7 at ¶¶ 92-93).) But Tela’s cited support is limited to its expert’s declaration, which is wholly conclusory on this point:

92. [Reciting challenged limitations]

93. I disagree that a person of ordinary skill in the art would not be able to understand with reasonable certainty, the bounds of these claim elements. It is well understood in the art that any region of an integrated circuit is finite in size, and as such it will have a boundary. A person of ordinary skill in the art, reading the specification would

understand that the claim elements are directed to placing a metal structures on each metal gridline in the region. As described in the Asserted Patents, placing the features on each metal gridline in the region helps with manufacturability of the features.

(CIMB, Ex. 7 at ¶¶ 92-93.) Certainly “any region . . . will have a boundary,” but there is no reason to think a person of ordinary skill would have understood this limitation to be limited in the way Tela contends, because the “in the region” language is omitted from the ’335 patent. *In re Skvorec*, 580 F.3d 1262, 1267 (Fed. Cir. 2009) (“The Board erred in holding that some wire legs . . . need not have an offset, when the claims state that each wire leg has an offset.”); *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379 (Fed. Cir. 2000) (“[W]hat the patentee subjectively intended his claims to mean is largely irrelevant to the claim's objective meaning and scope.”).

Accordingly, for the limitation as found in claim 1 of the ’335 patent, I find “each first-metal structure having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers” is clearly, convincingly, and necessarily indefinite.

10. “wherein each second-metal structure in the region is positioned next to at least one other second-metal structure on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure on a second side in accordance with the second-metal pitch”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claims 6, 11 '335 patent at claims 6, 11 '523 patent at claim 12	
Tela	Respondents	Staff
Plain and ordinary meaning.	Indefinite.	Indefinite.

(JC, App’x A at 17-18.)

The Parties brief the indefiniteness of this term along with, and on the same grounds as, “each first-metal structure [in the region] having at least one adjacent first-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers” discussed above. Unlike those limitations, all three of the ’334 patent, ’335 patent, and ’523 patent are the same in that they all use the “in the region” language to describe which “second-metal structure(s)” must have additional second-metal structures on either side. (’334 patent at cls. 6, 11; ’335 patent at cls. 6, 11; ’523 patent at cl. 12.)⁶

Despite this “in the region” language, however, I find the limitation indefinite for the same logical reason as claim 1 of the ’335 patent. As noted above, each of the ’334 patent, ’335 patent, and ’523 patent introduce the “second-metal layer” which the “second-metal structure(s)” are a part of, as being included “within” the “region”:

2. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures

(’334 patent at cl. 2);

2. The semiconductor chip as recited in claim 1, wherein the region includes a second-metal layer including second-metal structures

(’335 patent at cl. 2);

2. The semiconductor chip as recited in claim 1, further comprising: a second-metal layer formed above the first-metal layer within the region of the semiconductor chip

(’523 patent at cl. 2).

Given that the “second-metal layer” is defined as being within the “region,” it logically follows that all of the “second-metal structure(s)” are also within the “region.” Thus, although these

⁶ The ’335 patent and ’523 patent’s use of “second-metal structure layout shape” (’335 patent at cls. 6, 11; ’523 patent at cl. 12) instead of “second-metal structure” as in the ’334 patent (’334 patent at cls. 6, 11) does not affect the indefiniteness analysis.

challenged limitations include “in the region,” as in claim 1 of the ’334 patent, the language is to the same effect as claim 1 of the ’335 patent: all “second-metal structure(s)” must be within the “region” and have additional second-metal structures on either side, and those additional second-metal structures must be within the “region” and have additional second-metal structures on either side, ad infinitum. This is, of course, an impossibility.

Accordingly, I find “wherein each second-metal structure in the region is positioned next to at least one other second-metal structure on a first side in accordance with a second-metal pitch and is positioned next to at least one other second-metal structure on a second side in accordance with the second-metal pitch” is clearly, convincingly, and necessarily indefinite.

11. “each third-metal structure in the region having at least one adjacent third-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers”

The Parties disagree on the proper claim construction and have proposed the following constructions:

Relevant Claims	'334 patent at claims 10, 20 '335 patent at claims 10, 20	
Tela	Respondents	Staff
Plain and ordinary meaning.	Indefinite.	Indefinite.

(JC, App’x A at 18-19.)

The Parties brief the indefiniteness of this term along with, and on the same grounds as, the previous two limitations.⁷ As with the limitation concerning “second-metal structure(s)” within a “second-metal layer,” the ’334 and ’335 patents introduce “third-metal structure(s)” as within a “third-metal layer” which is itself introduced as included “within” the “region”:

⁷ The ’335 patent’s use of “third-metal structure layout shape” (’335 patent at cls. 10, 20) instead of “third-metal structure” as in the ’334 patent (’334 patent at cls. 10, 20) does not affect the indefiniteness analysis.

10. The semiconductor chip as recited in claim 7, wherein the region includes a third-metal layer including third-metal structures

('334 patent at cl. 10);

20. The semiconductor chip as recited in claim 1 wherein the region includes a third-metal layer including third-metal structures

('334 patent at cl. 20);

10. The semiconductor chip as recited in claim 7, wherein the region includes a third-metal layer including third-metal structures

('335 patent at cl. 10);

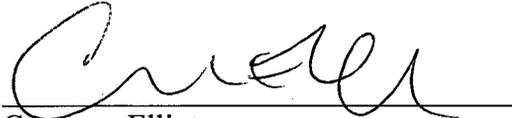
20. The semiconductor chip as recited in claim 1 wherein the region includes a third-metal layer including third-metal structures

('335 patent at cl. 20).

Like the “second-metal structure(s)” limitation, the '334 patent and '335 patent each use the “in the region” language to describe which “third-metal structure(s)” must have additional second-metal structures on either side. ('334 patent at cls. 10, 20; '335 patent at cls. 10, 20.) Despite this “in the region” language, the limitation is indefinite for the same reasons as above: given that the “third-metal layer” is defined as being within the “region,” it follows that all of the “third-metal structure(s)” are also within the “region.” Thus, the same impossible effect is required—all “third-metal structure(s)” must have additional third-metal structures on either side and within the “region.”

Accordingly, I find “each third-metal structure in the region having at least one adjacent third-metal structure positioned next to each of its sides in accordance with a y-coordinate spacing of less than or equal to 193 nanometers” is clearly, convincingly, and necessarily indefinite.

SO ORDERED.

A handwritten signature in black ink, appearing to read "C. Elliot", written over a horizontal line.

Cameron Elliot
Administrative Law Judge

**CERTAIN INTEGRATED CIRCUITS AND PRODUCTS
CONTAINING THE SAME**

INV. NO. 337-TA-1148

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **Order No. 34** has been served by hand upon the Commission Investigative Attorney John Shin, Esq., and the following parties as indicated, on OCT 02 2019.



Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT TELA INNOVATIONS, INC.	
William Bélanger, Esq. PEPPER HAMILTON, LLP Hamilton Square 19 th Floor, High Street Tower Boston, MA 02110	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____
FOR RESPONDENT ACER, INC., ACER AMERICA CORPORATION, ASUSTEK COMPUTER INC., ASUS COMPUTER INTERNATIONAL, INTEL CORPORATION, LENOVO GROUP LTD., LENOVO (UNITED STATES) INC., MICRO-STAR INTERNATIONAL CO., LTD. & MSI COMPUTER CORP.	
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