

In the Matter of

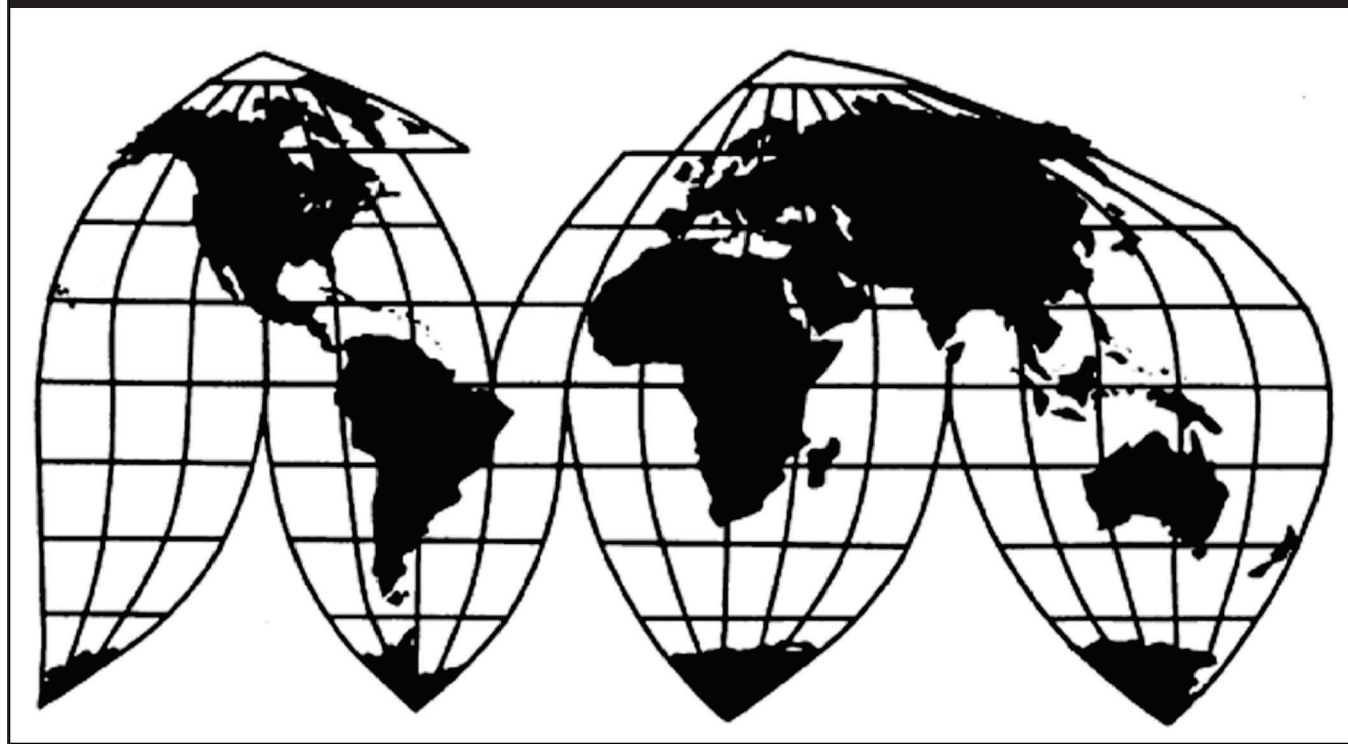
**CERTAIN SEMICONDUCTOR DEVICES
AND CONSUMER AUDIOVISUAL
PRODUCTS CONTAINING THE SAME**

Investigation No. 337-TA-1047

Publication 4966

September 2019

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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U.S. International Trade Commission

Washington, DC 20436
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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

**CERTAIN SEMICONDUCTOR
DEVICES AND CONSUMER
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CONTAINING THE SAME**

Investigation No. 337-TA-1047

**NOTICE OF THE COMMISSION'S FINAL DETERMINATION OF NO
VIOLATION OF SECTION 337; TERMINATION OF THE INVESTIGATION**

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has found no violation of section 337 of the Tariff Act of 1930, as amended, by respondents Sigma Designs, Inc. and Vizio, Inc. The investigation is terminated.

FOR FURTHER INFORMATION CONTACT: Robert Needham, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW, Washington, D.C. 20436, telephone (202) 708-5468. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, SW, Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (<https://www.usitc.gov>). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at <https://edis.usitc.gov>. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on April 12, 2017, based on a complaint filed by Broadcom Corporation ("Broadcom") of Irvine, California. 82 FR 17688. The complaint alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337 ("section 337"), in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products containing the same that infringe U.S. Patent Nos. 7,310,104 ("the '104 patent"); 7,342,967 ("the '967 patent"); 7,590,059 ("the '059 patent"); 8,068,171 ("the '171 patent"); and 8,284,844 ("the '844 patent"). *Id.* The Commission's notice of investigation named as respondents MediaTek Inc. of Hsinchu City, Taiwan, MediaTek

USA Inc. of San Jose, California, and MStar Semiconductor Inc. of ChuPei Hsinchu Hsien, Taiwan (together, “MediaTek”); Sigma Designs, Inc. of Fremont, California (“Sigma”); LG Electronics Inc. of Seoul, Republic of Korea and LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey (together, “LG”); Funai Electric Company, Ltd., of Osaka, Japan, Funai Corporation, Inc. of Rutherford, New Jersey, and P&F USA, Inc. of Alpharetta, Georgia (together, “Funai”); and Vizio, Inc., of Irvine, California (“Vizio”). *Id.* The Office of Unfair Import Investigations is not participating in this investigation. *Id.*

Several parties were terminated from the investigation based on settlement. Specifically, the Commission terminated the investigation with respect to Funai, Order No. 31 (Nov. 7, 2017), *not reviewed* Notice (Dec. 12, 2017); MediaTek, Order No. 35 (Nov. 29, 2017), *not reviewed* Notice (Dec. 19, 2017); and LG, Order No. 42 (Apr. 9, 2018), *not reviewed* Notice (May 4, 2018). Accordingly, only respondents Sigma and Vizio (together, “Respondents”) remained in the investigation at the time of the final ID.

The Commission also terminated two patents and several claims of the remaining patents based on Broadcom’s partial withdrawal of the complaint. Specifically, the Commission terminated the investigation with respect to the ’967 patent, the ’171 patent, claims 21-30 of the ’059 patent, and claim 14 of the ’844 patent. Order No. 24 (Oct. 10, 2017), *not reviewed* Notice (Oct. 24, 2017). Broadcom also elected to withdraw claims 5 and 11-13 of the ’844 patent in its post-hearing brief. ID at 7. Accordingly, at the time of the final ID, the only remaining claims were claims 1, 10, 11, 16, 17, and 22 of the ’104 patent; claims 1-4, 6-10, of the ’844 patent; and claims 11-20 of the ’059 patent.

On May 11, 2018, the ALJ issued a final ID finding no violation of section 337. Specifically, he found that Respondents did not infringe any claim, that the asserted claims of the ’844 patent are invalid, and that Broadcom did not satisfy the technical prong of the domestic industry requirement for the ’104 patent. On May 29, 2018, Broadcom and Respondents each petitioned for review of the ID. On June 6, 2018, the parties opposed each other’s petitions.

On July 17, 2018, the Commission determined to review the following issues: (1) the construction of “a processor adapted to control a decoding process” in claim 1 of the ’844 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (2) the finding that the prior art reference Fandrianto anticipates the limitation “adapted to perform a decoding function on a digital media stream” of claim 1 of the ’844 patent; (3) the construction of “the blended graphics image” in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (4) the construction of “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” limitation in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; and (5) the finding that claims 1 and 10 of the ’104 patent are invalid as obvious if certain claim constructions are modified. The

Commission determined not to review the ID's finding of no violation with respect to the '059 patent.

Having examined the record of this investigation, including the ALJ's final ID, the petitions, responses, and other submissions from the parties and the public, the Commission has determined that Broadcom has not proven a violation of section 337 by Sigma and Vizio. Specifically, the Commission has determined to modify the ID's construction of "a processor adapted to control a decoding process," and, under the modified construction, finds that the limitation is satisfied for the technical prong of the domestic industry requirement and invalidity, but is not satisfied for infringement. The Commission also has determined to affirm under modified reasoning that Pandrianto satisfies the limitation "adapted to perform a decoding function on a digital media stream." The Commission has additionally determined to modify the ID's construction of "the blended graphics image," and, under the modified construction, finds that the limitation is satisfied for infringement and the technical prong. The Commission has further determined to affirm under modified reasoning the ID's construction of "blend the blended graphic image with the video image using the alpha values and/or at least one value derived from the alpha values," and affirms the ID's findings on infringement, invalidity, and the technical prong with respect to the limitation. Finally, the Commission has determined to take no position on the ID's finding that claims 1 and 10 of the '104 patent are obvious.

Accordingly, the Commission has determined that Broadcom has failed to show a violation of section 337 with respect to both the '844 and '104 patents. For the '844 patent, the Commission finds that Broadcom failed to establish infringement, but did satisfy the technical prong of the domestic industry requirement. The Commission further finds that the Respondents showed by clear and convincing evidence that claims 1-10 are invalid as anticipated. For the '104 patent, the Commission finds that Broadcom failed to show both infringement and the satisfaction of the technical prong of the domestic industry requirement. The Commission's determinations are explained more fully in the accompanying Opinion. All other findings in the ID under review that are consistent with the Commission's determinations are affirmed.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. 1337), and in part 210 of the Commission's Rules of Practice and Procedure (19 CFR part 210).

By order of the Commission.

A handwritten signature in black ink, appearing to read "Lisa R. Barton", with a stylized flourish at the end.

Lisa R. Barton
Secretary to the Commission

Issued: September 19, 2018

**CERTAIN SEMICONDUCTOR DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS CONTAINING THE SAME**

Inv. No. 337-TA-1047

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served upon the following parties as indicated, on September 19, 2018.



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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

CERTAIN SEMICONDUCTOR
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Investigation No. 337-TA-1047

COMMISSION OPINION

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I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on April 12, 2017, based on a complaint filed by Broadcom Corporation ("Broadcom") of Irvine, California. 82 Fed. Reg. 17688. The

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complaint alleged violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337 (“section 337”), in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products containing the same that infringe U.S. Patent Nos. 7,310,104 (“the ’104 patent”); 7,342,967 (“the ’967 patent”); 7,590,059 (“the ’059 patent”); 8,068,171 (“the ’171 patent”); and 8,284,844 (“the ’844 patent”). *Id.* The Commission’s notice of investigation named as respondents MediaTek Inc. of Hsinchu City, Taiwan, MediaTek USA Inc. of San Jose, California, and MStar Semiconductor Inc. of Chupei Hsinchu Hsien, Taiwan (together, “MediaTek”); Sigma Designs, Inc. of Fremont, California (“Sigma”); LG Electronics Inc. of Seoul, Republic of Korea and LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey (together, “LG”); Funai Electric Company, Ltd., of Osaka, Japan, Funai Corporation, Inc. of Rutherford, New Jersey, and P&F USA, Inc. of Alpharetta, Georgia (together, “Funai”); and Vizio, Inc., of Irvine, California (“Vizio”). *Id.* The Office of Unfair Import Investigations is not participating in this investigation. *Id.*

The Commission terminated the investigation by reason of settlement with respect to Funai, Order No. 31 (Nov. 7, 2017), *not reviewed* Notice (Dec. 12, 2017); MediaTek, Order No. 35 (Nov. 29, 2017), *not reviewed* Notice (Dec. 19, 2017); and LG, Order No. 42 (Apr. 9, 2018), *not reviewed* Notice (May 4, 2018). The Commission also terminated the investigation by reason of partial withdrawal of the complaint with respect to the entire ’967 patent, the entire ’171 patent, and certain claims of the ’059 and ’844 patents. Order No. 24 (Oct. 10, 2017), *not reviewed* Notice (Oct. 24, 2017). Accordingly, at the time of the final initial determination, the only remaining respondents were Sigma and Vizio (together, “Respondents”) and the only remaining asserted claims were claims 1, 10, 11, 16, 17, and 22 of the ’104 patent; claims 1-4, 6-

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10, of the '844 patent; and claims 11-20 of the '059 patent.

The presiding administrative law judge ("ALJ") conducted a hearing on December 6-8 and 11, 2017.¹ On May 11, 2018, the ALJ issued a final initial determination ("ID") finding no violation of section 337.² Specifically, the ID concluded that: (1) Broadcom had not shown infringement or the technical prong of the domestic industry requirement for the '104 patent; (2) Broadcom had not shown infringement for the '844 patent, and Respondents had shown that claims 1-10 of the '844 patent are invalid as anticipated; and (3) Broadcom had not shown infringement for the '059 patent. ID at 444-45. On May 23, 2018, the ALJ issued a Recommended Determination on Remedy and Bonding.

On May 29, 2018, Broadcom filed a petition for Commission review of the ID,³ and Respondents filed a contingent petition for Commission review of the ID.⁴ On September 29, 2015, ARM and Respondents filed replies to each other's petitions.⁵

On July 17, 2018, the Commission determined to review the ID in part. 83 Fed. Reg. 34870-71 (Jul. 23, 2018). The scope of Commission review encompassed: (1) the construction

¹ Following the hearing, the parties filed opening and reply post-hearing briefs before the ALJ. Complainant Broadcom Corporation's Post-Hearing Brief (Jan. 8, 2018) ("Broadcom IPHB"); Respondents' Post-Hearing Brief (Jan. 8, 2018) ("Respondents IPHB"); Complainant Broadcom Corporation's Reply Post-Hearing Brief (Jan. 19, 2018) ("Broadcom RPHB"); Respondents' Post-Hearing Reply Brief (Jan. 19, 2018) ("Respondents RPHB").

² Final Initial Determination (May 11, 2018).

³ Complainant Broadcom Corporation's Petition for Commission Review (May 29, 2018) ("Broadcom Pet.").

⁴ Respondents' Contingent Petition to Review the Final Initial Determination (May 29, 2018).

⁵ Complainant Broadcom Corporation's Reply to Respondents' Contingent Petition for Commission Review (Jun. 6, 2018) ("Broadcom Pet. Reply"); Response of Respondents Vizio Inc. and Sigma Designs, Inc. to Complainant Broadcom Corporation's Petition for Commission Review (Jun. 6, 2018) ("Respondents Pet. Reply").

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of “a processor adapted to control a decoding process” in claim 1 of the ’844 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (2) the finding that the prior art reference Fandrianto anticipates the limitation “adapted to perform a decoding function on a digital media stream” of claim 1 of the ’844 patent; (3) the construction of “the blended graphics image” in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (4) the construction of “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” limitation in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; and (5) the finding that claims 1 and 10 of the ’104 patent are invalid as obvious if certain claim constructions are modified. *Id.* The Commission determined not to review the ID’s finding of no violation with respect to the ’059 patent. The Commission also solicited briefing from the parties on certain issues under review, and solicited briefing on remedy, bonding, and the public interest from the parties and the public. *Id.*

On July 27, 2018, Broadcom and Respondents filed written submissions in response to the Commission’s notice of review,⁶ and filed reply written submissions on August 3, 2018.⁷

⁶ Complainant Broadcom Corporation’s Written Submission on the Issues Identified in the Notice of a Commission Determination to Review in Part a Final Initial Determination Finding No Violation of Section 337 (Jul. 27, 2018) (“Broadcom Sub.”); Respondents’ Response to the Commission’s July 17, 2018 Notice and Request for Written Submissions (“Respondents Sub.”).

⁷ Complainant Broadcom Corporation’s Reply Submission to Respondents’ Response to the Commission’s July 17, 2018 Notice and Request for Written Submissions (Aug. 3, 2018) (“Broadcom Reply Sub.”); Respondents’ Reply to Complainant’s Response to the Commission’s July 17, 2018 Notice and Request for Written Submissions (Aug. 3, 2018), as corrected on August 7, 2018 (“Respondents Reply Sub.”).

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The Commission also received a submission on the public interest from the American Consumer Institute.

B. The Asserted Patents

The '844 patent is entitled "Video Decoding System Supporting Multiple Standards," and claims priority to April 1, 2002. JX-0001. The patent generally relates to a system of arranging hardware accelerators into a decoding pipeline, where the hardware accelerators are configurable to support decoding a variety of formats. *Id.* at Abstract. In response to Broadcom's petition, the Commission determined to review two issues with respect to claim 1, which reads as follows:

1. A digital media decoding system comprising:
 - a processor adapted to control a decoding process; and
 - a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream, wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.

Id. at 20:17-23.

The '104 patent is entitled "Graphics Display System with Anti-flutter Filtering and Vertical Scaling Feature," and claims priority to a provisional application filed on November 9, 1998. JX-0003. The patent generally relates to a chip used in a set-top box for providing anti-flutter filtering and scaling of graphics, although the independent claims are generally directed to devices that blend graphics together, then blend the blended graphics with video according to a certain alpha value technique. *Id.* at Abstract and 60:45-62:52. In response to Broadcom's petition, the Commission determined to review three issues with respect to claim 1, which reads as follows:

1. One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:

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at least one interface operable to receive one or both of video and audio; and

at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:

blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,

process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

Id. at 60:44-63.

C. The Accused Products

Broadcom accuses Sigma of infringing the '844 and '104 patents through the importation and sale of its [] system-on-a-chip ("SoC") products. *Id.* at 8. The parties agreed that the [] SoC is representative of all four of these SoC products. *Id.* These SoC products perform multimedia data processing for televisions and other audiovisual products. Respondents IPHB at 11.

Broadcom accuses Vizio of infringing the '844 and '104 patents through the importation and sale of televisions and other consumer audiovisual products containing an accused Sigma SoC. *Id.* at 8. The parties agreed that the [] SoC is representative in relevant part of the accused Vizio products containing Sigma SoCs. *Id.*

D. The Alleged Domestic Industry Products

Broadcom alleges that the domestic industry products are the [] models of Broadcom products listed on pages 9 and 10 of the ID. The ID found that Broadcom showed that the [] SoC is representative of all [] alleged domestic industry products. *Id.*

II. ANALYSIS

The Commission determines to make the findings, conclusions, and supporting analysis set forth below. Any findings, conclusions, and supporting analysis by the ALJ that are under review and are not inconsistent with our analysis and conclusions below are affirmed.

A. The '844 Patent

The Commission finds no violation of section 337 with respect to the '844 patent because Broadcom failed to show that the [] product satisfies the limitation “a processor adapted to control a decoding process” required for infringement and because Respondents showed that claims 1-10 are invalid as anticipated by clear and convincing evidence.

1. Claim Construction

The first step of a patent infringement analysis is “determining the meaning and scope of the patent claims asserted to be infringed.” *Markman v. Westview Instrs., Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995). Claim 1 of the '844 patent includes the limitation “a processor adapted to control a decoding process.” JX-0001. The ID construed the limitation to mean “a core decoder processor designed to orchestrate decoding for each pipeline stage.” ID at 187. Broadcom contends that the ID’s construction is erroneous because it improperly imports limitations from the specification into the claims, and argues that the term should be given its plain and ordinary meaning. Broadcom Pet. at 31, 34. Respondents contend the ID correctly construed the term in light of the specification. Respondents Resp. at 35-41.

The Commission finds that the ID’s construction of “a core decoder processor designed

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to orchestrate decoding for each pipeline stage” lacks sufficient legal and factual support. The ID relies primarily upon a portion of the specification stating “[t]he software control typically consists of a simple pipeline that orchestrates decoding by issuing commands to each hardware accelerator module for each pipeline stage” JX-0001 at 5:30-32 (emphasis added), but the Commission finds no basis to limit the claims based on a description as to how the invention “typically” works. The ID also relies upon portions of the specification in which the core processor controls a pipeline, ID at 189, but none of these citations recite a processor designed to “orchestrate decoding for each pipeline stage.”

The Commission also rejects Broadcom’s proposed construction of plain and ordinary meaning. The plain and ordinary meaning of “a processor adapted to control a decoding process” would encompass any processor that controls a decoding process in any manner, but the ’844 patent specification disclaims such scope. The specification disclaims several types of prior art processor control, JX-0001 at 1:59-2:31, and specifically disclaims a processor controlling decoding through “fine-granularity acceleration,” *id.* at 5:12-19. But under the plain and ordinary meaning, claim 1 would cover a processor performing fine-granularity acceleration, as long as it also controls a configurable hardware accelerator. Thus, construing the term in the manner proposed by Broadcom would cause the limitation to read on disclaimed prior art.

For the reasons that follow, the Commission has determined to modify the construction of “a processor adapted to control a decoding process” to mean “a core processor adapted to control a decoding process according to a processing pipeline.” A basic tenet of claim construction is that “[w]hen a patent thus describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.” *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007). Here, the specification describes the “present invention”

as “high-level granularity acceleration,” in which a core processor controls a decoding process by instructing hardware accelerators to run according to a processing pipeline:

The decoding system of **the present invention** employs high-level granularity acceleration with internal programmability or configurability to achieve the requirements above by implementation of very fundamental processing structures that can be configured dynamically by the **core decoder processor** In the high-level granularity system of **the present invention**, the firmware configures each hardware accelerator, which in turn represent high-level functions (such as motion compensation) that run (using a well defined specification of input data) without intervention from the main **core processor**. Therefore, each hardware accelerator runs in parallel **according to a processing pipeline dictated by the firmware in the core processor**. Upon completion of the high-level functions, each accelerator notifies the main **core processor, which in turn decides what the next processing pipeline step should be**.

JX-0001 at 5:7-29 (emphasis added). This passage thus makes clear that “the present invention” involves a “core processor” that controls a decoding process “according to a processing pipeline.” Later, the specification emphasizes the critical nature of the pipeline to the disclosed invention by referring to “the pipeline architecture of the present invention”:

Due to the selection of hardware elements that comprise the pipeline, **the pipeline architecture of the present invention** can accommodate, at least, substantially any existing or future compression algorithms that fall into the general class of block-oriented algorithms.

JX-0001 at 15:38-40 (emphasis added). These statements show that the patentee viewed the “present invention” as a “high-level granularity acceleration” decoding system in which a core processor controls configurable hardware accelerators according to a processing pipeline.

Claim terms must also be read in view of the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed.Cir.2005) (*en banc*). Here, the remainder of the specification shows that the term “a processor adapted to control a decoding process” means “a core processor adapted to control a decoding process according to a processing pipeline.” Every embodiment of the

specification recites a “core processor” that controls a decoding process according to a processing pipeline. *See, e.g.*, JX-0001 at 5:41-44 (“The core processor 302 is the central control unit of the decoding system 300 The core processor 302 also orchestrates the macroblock (MB) processing pipeline for all modules”); *id.* at 8:15-30 (“the core processor 302 interprets the decoded bits for the appropriate headers and decides and coordinates the actions of hardware blocks 306, 308, 309, 310, 312, and 314 The core processor keeps track of certain information in order to maintain the correct pipeline”); *id.* at 16:13-15 (“The core processor 302 controls the pipeline, initiates the decoding of each macroblock, and controls the operation of each of the hardware accelerators.”); *id.* at 17:39-41 (same); *id.* at 18:4-7 (“the core processor starts all the hardware modules for which input criteria is available. The criteria for starting all modules depends on an exemplary pipeline control mechanism illustrated in FIG. 6.”). Indeed, the specification is inextricably intertwined with both “core processors” and “pipelines,” reciting “core processor” more than one hundred times and “pipeline” more than fifty times.

Accordingly, when viewed in light of the specification, the term “a processor adapted to control a decoding process” does not encompass any processor that exhibits any form of control, but rather requires a “core processor” that controls a decoding process “according to a processing pipeline.”

The '844 patent explains that “decoding according to a pipeline” means that a first decoding function is performed on a first data block of a data stream, then a second decoding function is performed on the first block while the first decoding function is performed on a second block, and so on until all necessary decoding functions are performed on each block. *See* JX-0001 at Abstract (“The hardware accelerators function in a decoding pipeline wherein at any given stage in the pipeline, while a given function is being performed on a given macroblock, the

next macroblock in the data stream is being worked on by the previous function in the pipeline.”); *see also id.* at 2:47-63 (describing performing a first decoding function on the data element i of a data stream, then performing a second decoding function on the data element i while also performing the first decoding function on data element $i+1$); *id.* at FIG. 6 and 15:52-58, 16:27-63 (same). Accordingly, under the Commission’s construction of “a processor adapted to control a decoding process,” the core processor controls a decoding process according to a pipeline in which a series of decoding functions are performed on each data block, arranged so that multiple decoding functions decode different data blocks simultaneously.

Broadcom argues that it is erroneous to limit the term “a processor adapted to control a decoding process” to a specific processor, because the claim language itself does not require a specific type of processor. Broadcom Pet. at 31-32. Patent claims, however, are not read in isolation, but must instead be read in the context of the specification. *UltimatePointer, L.L.C. v. Nintendo Co., Ltd.*, 816 F.3d 816, 824 (Fed. Cir. 2016). The ’844 patent specification repeatedly describes the present invention and its embodiments as comprising a “core processor.” And while Broadcom contends the specification discloses two other processors, Broadcom Pet. at 31, these processors are mentioned only in passing before describing a core processor that controls a decoding process. *Compare* JX-0001 at 3:67 (reciting a “host CPU 114,” without further explanation) and *id.* at 4:4-7 and 4:31-33 (describing a “transport processor 102”) *with id.* at 5:7-19:63 (describing a core processor that controls hardware accelerators performing decoding functions). The Commission therefore rejects Broadcom’s attempt to obtain overbroad claim scope by divorcing the claims from the specification.

Respondents, on the other hand, argue that the term “a processor adapted to control a decoding process” should be limited to a “core decoder processor,” as found by the ID.

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Respondents Resp. at 35-41. The specification of the '844 patent, however, recites “core decoder processor” only once, JX-0001 at 5:11-12, but recites “core processor” more than one hundred times in describing the present invention and its embodiments, *id.* at 5:7-19:63. The Commission finds that the prevalence of the description of the “core processor” feature throughout the specification supports modifying the construction to include a “core processor.”

Broadcom also argues that it is erroneous to construe the term “a processor adapted to control a decoding process” to require control by a pipeline. Broadcom Pet. at 32-34. Broadcom contends the '844 patent discloses three embodiments in which the core decoder processor exercises varying levels of control, but Broadcom's own argument expressly acknowledges that two of its cited embodiments require that the processor control a pipeline, *id.* at 33, and its third cited embodiment discloses “exemplary pipeline control,” JX-0001 at 18:6-7. Broadcom also argues that requiring a pipeline inappropriately reads a limitation from the specification into the claims, *id.* at 34, but ignores the specification's repeated characterization of pipeline control as “the present invention,” and its prevalence throughout the embodiments. Given the '844 patent's repeated and consistent description of the invention as a processor controlling decoding by hardware accelerators according to a pipeline, it would be anomalous to construe the claimed invention as not requiring a pipeline. *See Virnetx, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1318 (Fed. Cir. 2014) (“The fact that anonymity is ‘repeatedly and consistently’ used to characterize the invention strongly suggests that it should be read as part of the claim.”).

Broadcom further contends that it is erroneous to construe the term to require pipeline control because the '844 patent specification discloses a single-stage pipeline. Broadcom Pet. at 33-34. The portion of the specification cited by Broadcom, however, merely states that certain decoding functions may be rearranged to occur in series in the same pipeline stage:

In an alternative embodiment of the present invention, the functions of two or more hardware modules are combined into one pipeline stage and the macroblock data is processed by all the modules in that stage sequentially. For example, in an exemplary embodiment, inverse transform operations for a given macroblock are performed during the same pipeline stage as IQ operations. In this embodiment, the inverse transform module 309 waits idle until the inverse quantizer 308 finishes and the inverse quantizer 308 becomes idle when the inverse transform operations start. This embodiment will have a longer processing time for the “packed” pipeline stage, and therefore such embodiments may have lower throughput. The benefits of the packed stage embodiment include fewer pipeline stages, fewer buffers and possibly simpler control for the pipeline.

JX-0001 at 16:64-17:11. A rearranged pipeline, however, is still a pipeline, and the following sentence of the specification explains that this “packed” pipeline still consists of multiple stages: “[t]he above-described macroblock-level pipeline advances stage-by-stage.” *Id.* at 17:12-13.

Moreover, Broadcom’s assertion that a pipeline can be a single stage is contrary to the portions of the specification requiring that a pipeline have multiple stages. *See, e.g., id.* at 15:25-27 (“the actions of the various hardware blocks are arranged in an execution **pipeline comprising a plurality of stages**”) (emphasis added); *id.* at 15:61-64 (“At any given stage in the pipeline, while a given function is being performed on a given macroblock, the next macroblock in the data stream is being worked on by the previous function in the pipeline.”). Furthermore, nearly the entire specification describes in detail the hardware and steps necessary to create the configurable “pipeline architecture of the present invention,” JX-0001 at 15:39, so interpreting the claims to cover a simple single-stage process would divorce the claims from the specification and is contrary to the teachings of the ’844 patent.

2. Infringement

After construing the disputed claim terms, the second and final step of a patent infringement analysis is “comparing the properly construed claims to the device accused of

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infringing.” *Markman*, 52 F.3d at 976. Here, the ID found that Broadcom failed to show that the [] product satisfies the limitation “a processor adapted to control a decoding process” under the ID’s construction, ID at 201, but found that Broadcom showed that the [] product satisfies every other limitation of claims 1-10 of the ’844 patent.⁸ The only infringement issue under review for the ’844 patent is whether the [] product satisfies the limitation “a processor adapted to control a decoding process” under the Commission’s modified construction. For the reasons discussed below, the Commission finds that Broadcom failed to show that the [] product satisfies the limitation, and thus finds that Broadcom failed to show infringement with respect to the ’844 patent.

As discussed in the previous section, the Commission construed “a processor adapted to control a decoding process” to mean “a core processor adapted to control a decoding process according to a processing pipeline,” in which the processor controls a multi-step process of performing a series of decoding functions. Broadcom acknowledges that the accused [] SoC does not control a decoding process according to such a pipeline, because the [] []. Broadcom IPHB at 163, 167-68. While Broadcom contends that the [] product’s control is akin to a “single-stage decoding pipeline,”⁹ the Commission finds that Broadcom’s “single-stage” argument is an admission that the [] does not operate according to a processing pipeline at all. A pipeline necessarily requires multiple stages, and Broadcom itself acknowledges that “a single stage is not a pipeline.” Broadcom Sub. at 7. Accordingly, the Commission finds that this single-step

⁸ Claims 2-10 of the ’844 patent all depend from claim 1.

⁹ Broadcom IPHB at 168 (“The []’s video decoder hardware, which performs the decoding process, is []”); Broadcom RPHB at 60 (referring to the []’s “single-stage decoding pipeline”); *see also* CX-0003C (Acton DWS) at Q/A 161 (testifying that the []”).

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process is not performed according to a processing pipeline, and thus concludes that Broadcom failed to show that the [] SoC discloses “a core processor adapted to control a decoding process according to a processing pipeline.”

In addition, the ID found that Broadcom failed to satisfy this limitation because, although Broadcom alleged that the [] satisfied this limitation, Broadcom IPHB at 163, Broadcom’s expert, Dr. Acton, testified to the contrary that the [] “controls the video decoder functionality.” ID at 199 (quoting CX-0003C (Acton WS) at Q/A 185); *see also* CX-0003C (Acton WS) at Q/A 183-86 (describing in detail how the [] [] controls the video decoder functionality).¹⁰ The Commission finds that Broadcom’s argument and evidence creates ambiguity as to what “processor” Broadcom accuses of satisfying this limitation, and thus Broadcom’s contradictory arguments and evidence further failed to show that this limitation is satisfied by a preponderance of the evidence. *See* RX-1079 (Stevenson DWS) at Q/A 62-64 (testifying that Dr. Acton’s testimony is contradictory).

3. Technical Prong of the Domestic Industry Requirement

In order to show a violation of section 337, a complainant must also satisfy the technical prong of the domestic industry requirement, which requires “a comparison of domestic products to the asserted claims.” *Crocs, Inc. v. Int’l Trade Comm’n*, 598 F.3d 1294, 1307 (Fed. Cir. 2010). Here, the ID found that Broadcom showed that the technical prong was satisfied for the [] product with respect to claims 1-13 of the ’844 patent under the ID’s constructions. The only technical prong issue under review for the ’844 patent is whether the [] product satisfies the limitation “a processor adapted to control a decoding process” under the

¹⁰ Elsewhere, however, Dr. Acton testified that the [] is the processor that controls the decoding process. CX-0003C at Q/A 155-60.

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Commission's modified construction. For the reasons discussed below, the Commission finds that Broadcom showed that the [] product satisfies the limitation "a processor adapted to control a decoding process" under the Commission's modified construction, and thus has established the technical prong of the domestic industry requirement for the '844 patent with respect to claims 1-13 of the '844 patent.

Broadcom's expert, Dr. Acton, testified that the Broadcom [] [] shows that the [] are core processors that control decoding according to a processing pipeline. CX-0003 (Acton DWS) at Q/A 234-39. That document states that the [] are processors that control decoding:

CX-0051C at 8. The document further explains that these processors are core processors that control decoding via a pipeline:

Id.

Respondents' only rebuttal was their argument that, because the control was shared between the [], no single processor in the [] controlled decoding as required by this limitation. Respondents' RPHB at 57-58. However, the Federal Circuit "has repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance

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carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” *Convolve, Inc. v. Compaq Computer Corp.*, 812 F.3d 1313, 1321 (Fed. Cir. 2016). Here, all of the asserted claims are “comprising” claims, and the specification expressly states that multiple processors may control the decoding process. *See, e.g.*, JX-0001 at 6:24-31 (describing an embodiment where the PVLD engine acts as a “coprocessor” that assists in decoding the data). Accordingly, Respondents’ only rebuttal fails because the claims permit two processors to collectively satisfy the limitation.

4. Invalidity

A patent is invalid as anticipated if “the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.” 35 U.S.C. § 102(a).¹¹ Such anticipation requires that “a single prior art reference discloses each and every limitation of the claimed invention.” *Schering Corp. v. Geneva Pharms.*, 339 F.3d 1373, 1378 (Fed. Cir. 2003). Anticipation must be shown by clear and convincing evidence. *Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 975 (Fed. Cir. 2010).

The ID found that Respondents had shown by clear and convincing evidence that U.S. Patent No. 5,982,459 (“Fandrianto”) (RX-0254) anticipates claims 1-10 of the ’844 patent, and that U.S. Patent No. 6,192,073 (“Reader”) (RX-0317) anticipates claims 1, 2, and 5-9 of the ’844 patent. The issues under review are whether Fandrianto and Reader disclose the limitation “a processor adapted to control a decoding process” of claim 1 under the Commission’s modified

¹¹ The America Invents Act (“AIA”) amended 35 U.S.C. § 102, effective for any patent application with filing date on or after March 18, 2013, Pub. L. No. 112–29. Because the application resulting in the patents at issue in this case were filed before that date, we refer to the pre-AIA version of § 102.

construction, and whether Fandrianto discloses the limitation “adapted to perform a decoding function on a digital media stream” of claim 1.

a. “A Processor Adapted to Control a Decoding Process”

The ID found that there was no dispute that Fandrianto and Reader each satisfied the limitation “a processor adapted to control a decoding process” under both Respondents’ and Broadcom’s proposed constructions. ID at 222-23, 243-44. No party disputed this finding in its petitions or submissions. For the reasons discussed below, the Commission finds that both Fandrianto and Reader satisfy this limitation under the Commission’s modified construction.

The Commission finds that Fandrianto satisfies the limitation “a processor adapted to control a decoding process” under the Commission’s modified construction. Broadcom did not contest that Fandrianto satisfies this limitation under any construction. Moreover, Fandrianto discloses a RISC processor that programs and activates a video processor to perform a sequence of subroutines:

On-chip SRAM **282** allows RISC processor **220** to download new subroutines for video processor **280**. RISC processor activates video processor **280** by writing to a command processor **960** which selects a subroutine from ROM **284** or RAM **282**. Command processor **960** contains a queue for a sequence of subroutines to be executed by video processor **280**. A RISC core **940** and a sequencer **970** decode microcode instructions from the selected subroutine and control a data path **970** which implements the microcode instructions. RISC core **940** and data path run until the subroutine is complete, then a next subroutine is performed.

RX-0324 at 13:1-11. Respondents’ expert, Dr. Stevenson, testified that this passage, as well as other passages showing that the RISC processor “supervises hardware resources,” shows that the RISC processor is a core decoder processor that controls a pipeline. RX-0383C (Stevenson DWS) at Q/A 166-69 (citing RX-0324 (Fandrianto) at 4:21-22, 5:14-15, 9:19-28, and 12:62-13:11). The Commission finds that Fandrianto’s disclosure of a RISC processor that downloads

a queue of subroutines for execution in a video processor is “a core processor adapted to control a decoding process according to a processing pipeline.”

The Commission finds that Reader satisfies the limitation “a processor adapted to control a decoding process” under the Commission’s modified construction. Broadcom did not contest that Reader satisfies this limitation under any construction. Reader discloses that the scalar processor is a “core processor” by disclosing a figure in which the “DSP CORE” contains “scalar processor **210**.” RX-0317 at Fig. 2. Reader discloses a processor that controls a decoding process according to a pipeline by describing that the scalar processor performs certain decoding on data, which is then passed to the bitstream processor for further decoding, and finally passed to the vector processor for still further decoding:

In decoding, the process is reversed. Scalar processor **210** demultiplexes the system data into video and audio components, and performs sequence layer, GOP, and picture layer decoding of the video data. The resulting GOBs or slices are provided to bitstream processor **245**. Processor **245** performs zig-zag processing and Huffman and RLC decoding. VP **220** receives the output of BP **245** and performs dequantization, IDCT, and motion compensation.

Id. at 5:23-30. Reader also discloses that the scalar processor controls this pipeline by initializing and synchronizing the bitstream and vector processors, and by controlling the interface with external devices. *Id.* at 1:30-34 (“The scalar processor . . . synchronizes operation of the vector and bitstream processors, and controls interface with external devices.”); *id.* at 4:47-49 (“When contexts are to be switched, scalar processor **210** saves the current contexts and initializes BP **245** to process a different context”). Reader further explains that all three processors can operate simultaneously on different blocks of data to maximize processing speed, thereby disclosing pipeline control. *Id.* at 4:59-61 (“Video data processing is divided between scalar processor **210**, vector processor **220** and bitstream processor **245** so as to achieve a high processing speed.”); *id.* at 5:34-36 (“Scalar processor **210**, vector processor **220** and bitstream

processor 245 can operate on different blocks of data in parallel.”). Respondents’ expert testified that these and other passages in Reader disclose a core decoder processor that controls a pipeline. RX-0383C (Stevenson DWS) at Q/A 81-86 (citing RX-0317 (Reader) at 1:14-34, 4:59-5:3, 5:23-44). The Commission finds that Reader’s disclosure of a scalar processor that initializes and synchronizes other hardware components to decode in parallel is “a core processor adapted to control a decoding process according to a processing pipeline.”

Additionally, Reader incorporates by reference the specification of the Samsung type MSP-1EX processor, RX-0317 at 3:20-24, which is attached to the original Reader patent application (RX-0318) as Appendix A (RX-0319) and provides more detail on the teachings on the patent. Appendix A explains that the scalar processor¹² is a “core processor” by depicting a “DSP CORE” that includes a “32-bit ARM7 RISC CPU.” RX-0319 at A53-54. The appendix further states that the scalar processor is adapted to control a decoding process because “ARM7 is in charge of CODEC initialization.” *Id.* at A-103; see also A-24 (“[t]he ARM7 RISC CPU is the master processor of the MSP”); A-21 (“MSP program execution always begins with the ARM7 CPU”). The appendix explains that the ARM7’s firmware controls a pipeline by downloading applications, scheduling tasks, managing resources, and synchronizing communications. *Id.* at A19-20. Specifically, the ARM7 demultiplexes and parses the audiovisual streams, and initializes the bitstream processor to decode a block; next, the bitstream processor performs decoding on the block; the vector processor then performs decoding on the block; and finally the ARM7 transmits the audiovisual data to the host. *Id.* at A-130-33. Respondents’ expert testified Appendix A further discloses that the scalar processor controls a

¹² Reader discloses that the scalar processor is a “32-bit RISC processor” that “conforms to the standard ARM7 instruction set known in the art.” RX-0317 at 3:59-61; *see also id.* at Fig. 2 (labeling the scalar processor 210 as an “ARM7 RISC CPU”).

pipeline. RX-0383C (Stevenson DWS) at Q/A 81-86 (citing RX-0318 at A-21, A-103, A-128-29, A-131, and A-141).

b. “Adapted to Perform a Decoding Function on a Digital Media Stream”

The second issue under review is whether Fandrianto satisfies the limitation “adapted to perform a decoding function on a digital media stream” of claim 1 of the ’844 patent. The ID found that Fandrianto satisfied this limitation. ID at 249-50. For the reasons discussed below, the Commission affirms the ID’s finding under modified reasoning.

The ID found that the evidence showed that Fandrianto’s hardware accelerators (the video processor, the H.221/BCH decoder, and the Huffman decoder) are adapted to perform a decoding function on a digital media stream. *Id.* at 249 (citing RX-0383C (Stevenson DWS) at Q/A 177). The ID also reasoned that “Dr. Acton has not addressed Dr. Stevenson’s opinion that the H.221/BCH decoder performs a decoding function.” *Id.* at 250 (citing CX-0579 (Acton RWS) at Q/A 125).

Broadcom argues that the ID erred in its finding because Dr. Acton did address Dr. Stevenson’s opinion. Broadcom Pet. at 36-38 (quoting CX-0579C (Acton RWS) at Q/A 125). Respondents argue that the ID did not overlook Dr. Acton’s testimony, but merely found that Dr. Acton’s testimony was not sufficiently persuasive to qualify as “addressing” Dr. Stevenson’s testimony. Respondents Resp. at 51.

The Commission has determined to vacate the ID’s statement that Dr. Acton failed to address Dr. Stevenson’s testimony. Dr. Acton specifically testified that Fandrianto’s H.221/BCH processor does not perform a decoding function:

Under either Respondents’ or Broadcom’s proposed claim constructions, it is my opinion that Fandrianto’s “H.261 compliant H.221/BCH bit stream parser/multiplexer” is not “a hardware accelerator . . . adapted to perform a decoding function on a digital media data stream,” because the “bit

stream parser 510” only separates different data types, such as, video and audio data, and does not perform any decoding, that is, decompression, functions. The purpose of Fandrianto’s the bit stream parser is to separate different data types, such as, video and audio data. Dr. Stevenson admits that this is the purpose of the H.261 compliant H.221/BCH bit stream parser/multiplexer. The ’844 patent specification describes this same function as processing the digital media data stream and not as a decoding function. Looking to the ’844 patent at 4:3-7, the ’844 patent explains that separating audio and video is done as the stream is received: “The transport processor **102** receives and processes a digital media data stream. The transport processor **102** provides the audio portion of the data stream to the audio decoder **104** and provides the video portion of the data stream to the digital video decoder **116**.” The ’844 patent does not describe separating the audio and video as a decoding function, such as those listed at 4:55-65: “Fundamental functions exist that are common to most or all of these formats. Such functions include, for example, programmable variable-length decoding (VLD), arithmetic decoding (AC), inverse quantization (IQ), inverse discrete cosine transform (IDCT), pixel filtering (PF), motion compensation (MC), and de-blocking/de-ringing (loop filtering or postprocessing) According to the present invention, these functions are accelerated by hardware accelerators.” The ’844 patent, at 16:2-6, also describes the function of parsing the video streams macroblocks’ headers as a decoding function. The ’844 patent distinguishes the parsing of headers and syntax of the video stream data/macroblocks as a decoding function and the separating of audio and video data as parsing that is done prior to video decoding.

CX-0579C (Acton RWS) at Q/A 125 (emphasis added). Accordingly, it was erroneous for the ID to rely upon Dr. Acton’s supposed failure to address Dr. Stevenson’s testimony to support a finding that Fandrianto satisfies this limitation.

The Commission, however, finds that Fandrianto satisfies the limitation “adapted to perform a decoding function on a digital media stream” for the other reasons cited in the ID. ID at 247-50. The ID relied upon Dr. Stevenson’s testimony that Fandrianto discloses the following hardware accelerators performing the following decoding functions: the Huffman codec and H.221/BCH decoder processing “non-byte-aligned data structures” of a digital media stream; the H.221/BCH decoder separating audio and video data from a digital media stream; and the

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Huffman codec performing variable length decoding on a digital media stream. RX-0383C at Q/A 177. Dr. Stevenson also noted that, although Dr. Acton now testifies that parsing is not “a decoding function,” Dr. Acton previously argued that data parsing satisfied this limitation in the context of infringement. *Id.* at Q/A 178. Dr. Stevenson further testified that Dr. Acton did not dispute that the “non-byte aligned data processing” was a decoding function. *Id.*

The Commission has considered Dr. Acton’s testimony and does not view it as persuasive. Dr. Acton testified that “a decoding function” excludes the parsing of data into video and audio components primarily because a single sentence in the ’844 patent specification referred to parsing as “processing”:

The transport processor **102** receives and **processes a digital media data stream**. The transport processor **102** provides the audio portion of the stream to the audio decoder **104** and provides the video portion of the data stream to the digital video decoder **116**.

JX-0001 at 4:3-7 (emphasis added). But the mere fact that a processor “processes” data does not mean that the process does not involve decoding. Moreover, Dr. Acton declined to testify that a person of ordinary skill in the art would not understand parsing to be “a decoding process,” but rather testified that parsing was not “a decoding process” under the particular terminology used in the ’844 patent. But if Broadcom believed that the claim limitation “a decoding process” required a special definition based on the specification, Broadcom should have sought to construe the term during claim construction. Dr. Acton’s testimony thus amounts to an untimely attempt to construe “a decoding process.”

Dr. Acton also testified that parsing should not be considered “a decoding function” because parsing is not one of the examples of decoding functions listed in 4:55-65 of the ’844 patent. CX-0579C (Acton RWS) at Q/A 125. The specification, however, clearly confirms that the examples are not limiting, JX-0001 at 4:56-57 (“Such functions include, **for example . . .**”)

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(emphasis added), and nothing in the patent limits the term “a decoding function” in any way. Moreover, claim 1 requires that the “decoding function” be performed on “a digital media data stream,” and the specification discloses parsing as a function that interprets a digital media data stream and separates the stream into video and audio portions. *Id.* at 4:3-7. Furthermore, the specification describes parsing as the first step in the “video decode data flow.” *Id.* at 4:29-33. Fandrianto also refers to parsing as a part of the decoding process. *E.g.*, RX-0324 at 4:64-5:1 (stating that “When VCP 110 acts as a decoder . . . RISC processor 220 and processing resources such as H.221/BCH decoder separate audio data from video data.”).

c. Conclusion

Based on the findings of the ID as modified above, the Commission finds that Respondents showed by clear and convincing evidence that claims 1-10 of the '844 patent are invalid as anticipated.

B. The '104 Patent

The Commission finds no violation of section 337 with respect to the '104 patent because Broadcom failed to show that the accused [] product satisfies the limitation “place the blended graphics image in a format suitable for blending” for infringement, and Broadcom failed to show that the domestic industry [] product satisfies the limitation “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” for the technical prong of the domestic industry requirement.

1. Claim Construction

There are two claim construction issues under review: (1) the construction of “the blended graphics image” limitation in claim 1 of the '104 patent; and (2) the construction of the “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” limitation in claim 1 of the '104 patent.

a. “The Blended Graphics Image”

For the limitation “a blended graphics image,” the ID adopted the parties’ agreed construction of “data representing a single view of a mixture of at least two graphics images.” ID at 33-34 (emphasis added). The ID separately construed “the blended graphics image” to mean “data representing a single view of a mixture of **all** graphics images to be blended.” *Id.* at 38 (emphasis added).

Broadcom contends that the ID’s construction is erroneous because it violates the principle of antecedent basis and is not supported by the claim language of specification. Broadcom Pet. at 51-52. Respondents argue that the ID’s construction is proper based on the specification, prosecution history, and a prior construction that Broadcom offered in a district court proceeding. Respondents Resp. at 3-12.

The Commission has determined to modify the construction of “the blended graphics image” to have the same construction as “a blended graphics image” under the principle of antecedent basis. It is a basic axiom of patent law that the “[s]ubsequent use of the definite articles ‘the’ or ‘said’ in a claim refers back to the same term recited earlier in the claim.” *Wi-LAN, Inc. v. Apple, Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016). Thus, both “a blended graphics image” and “the blended graphics image” refer to the exact same “blended graphics image,” and cannot have different constructions. Because the parties agreed “a blended graphics image” should be construed to mean “data representing a single view of a mixture of at least two graphics images,” the Commission construes that “the blended graphics image” to refer to that same “data representing a single view of a mixture of at least two graphics images.”

Although the ID concluded that it need not follow antecedent basis, the case it cited does not support that conclusion. ID at 39 (citing *Aventis Pharms. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1374 (Fed. Cir. 2013)). *Aventis* does not even address antecedent basis, but instead

holds that the term “substantially pure” may have different meanings in different portions of a patent based on the context. *Aventis Pharms.*, 715 F.3d at 1374-75. Accordingly, nothing in *Aventis* suggests that it is proper to ignore the principle of antecedent basis regarding the use of a definite article, or that it is proper to give different constructions to repeated instances of the same limitation within a claim.

The ID’s construction that “the blended graphics image” must contain “all graphics images to be blended” is also contrary to the claim language. Claim 1 of the ’104 patent requires that the processor “blend a plurality of graphics images . . . to generate a blended graphics image” and then “blend the blended graphics image with the video image.” JX-0003 at 60:54-61. These limitations require that two or more graphics images be blended together, and that the blended result then be blended with the video image. Nothing in the claim requires that the video be blended with “all graphics images to be blended,” and nothing in the specification, prosecution history, or intrinsic evidence suggests that the Commission should deviate from the plain language of the claims.

b. “Blend the Blended Graphics Image with the Video Image Using the Alpha Values and/or at Least One Value Derived from the Alpha Values”

The ID construed the limitation “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” of claim 1 of the ’104 patent to mean “blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” ID at 48. For the reasons discussed below, the Commission has determined to affirm the ID’s construction under modified reasoning.

Broadcom contends that the ID’s construction is erroneous because it improperly imports a limitation from the embodiments into the claims, and misinterprets Broadcom’s prior

statements on this limitation in a district court brief opposing a motion for a summary judgment of invalidity in *Broadcom Corp. v. SiRF Technology, Inc.*, Case No. 8:08-cv-00546-JVS-MLG (C.D. Cal. July 15, 2010) (RX-0311). Broadcom Pet. at 74-76. Broadcom argues that the construction should instead be given its plain and ordinary meaning. *Id.* Respondents argue that the ID correctly construed the term consistently with Broadcom's *SiRF* brief. Respondents Resp. at 13-15.

There is no dispute that the '104 patent discloses the ID's construction as the preferred embodiment of the invention. Specifically, the '104 patent discloses:

The formula that represents the preferred blending scheme is:

$$R(i)=A(i)*P(i)+(1-A(i)*P(i-1))$$

and

$$AR(i)=AR(i-1)*(1-A(i))$$

Where . . . A(i) represents the alpha value of the current pixel . . . AR(i) is the alpha value resulting from each instance of the operation, and AR(i-1) represents the intermediate alpha value at the location of the current pixel determined from all of the upper layers behind the current pixel . . ."

JX-0003 at 45:50-46:1 (emphasis added). The specification explains that the bolded formula is calculated at each layer, and "so that when all layers {i} have been processed, the result is that AR=the product of all (1-(A(i)) values for all upper layers." *Id.* at 46:22-23. Thus, the specification describes the preferred embodiment as blending video and graphics "using an alpha value derived from the product of one minus the alpha value for every graphics image." The disclosure of a preferred embodiment alone, however, does not support importing that embodiment into the claims. *Hill-Rom Servs. Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372-73 (Fed. Cir. 2014).

The specification may also expressly or implicitly disclaim subject matter. *SkinMedica*,

Inc. v. Histogen, Inc., 727 F.3d 1187, 1195-96 (Fed. Cir. 2013). Here, the specification distinguishes the invention from the conventional prior art by requiring a particular calculation:

In other words, in the preferred embodiment, at each stage of blending the upper layers, the pixels of the current layer are blended using the current alpha value, and also an intermediate alpha value is calculated as the product $(1-A(i)) \cdot (AR(i-1))$. **The key differences between this and the direct evaluation of the conventional formula are: (1) the calculation of the product of the set of $\{(1-A(i))\}$ for the upper layers, and (2) a virtual transparent black layer is used to initialize the process for blending the upper layers, since the lower layers that would normally be blended with the upper layers are not used in this point at the process.**

JX-0003 at 46:7-17 (emphasis added). The specification thus acknowledges that a difference between conventional prior art and the disclosed blending method is the calculation of the set of one minus the alpha value. Accordingly, even though claim 1 recites “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” the specification states that the invented blending scheme requires “using an alpha value derived from the product of one minus the alpha value for every graphics image,” and disclaims all other scope.

Additionally, in the *SiRF* district court case, Broadcom specifically admitted that claim 1 of the '104 patent required the second formula of the preferred embodiment, and that the formula is the difference between claim 1 and the prior art. Specifically, Broadcom's *SiRF* brief noted that the '104 patent disclosed the formula:

$$R(i)=A(i)*P(i)+(1-A(i))*P(i-1))$$

and

$$\mathbf{AR(i)=AR(i-1)*(1-A(i))}$$

and explained that “the first part of the formula borrows from standard prior art alpha blending,” and the “second (bolded) part of the formula distills the critical aspect of the invention, teaching

the computation of a ‘composite alpha value,’ which permits rich blending of graphics and video more quickly, and using less power and resources, than was previously possible.” RX-0311 at 5; *see also id.* at 7 (“The novel aspect of the invention is distilled in the second half of the formula.”). Broadcom goes on to state:

SiRF argues that the prior art “used a blending formulation ... that is substantially identical to the formulation used in the *first*—but not the second—part of the formula. Mot. at 14. Thus, SiRF’s motion actually concedes that the prior art it relies on used standard alpha blending, *not* the **novel alpha blending disclosed and claimed in the ’104 patent**.

Id. (emphasis added). Thus, although claim 1 recites blending “using the alpha values and/or at least one value derived from the alpha values,” Broadcom’s *SiRF* brief acknowledges that such blending was known in the prior art, but states that the claims are patentable over the prior art because they are limited to the second half of the formula.

Additionally, in support of its *SiRF* brief, Broadcom filed an expert declaration in the *SiRF* litigation acknowledging that claim 1 of the ’104 requires the second half of the formula, and that the second half of formula is what renders claim 1 valid. Specifically, Broadcom’s expert, Dr. Schonfeld, testified that

While the first half of the formula quoted above borrows from prior art alpha blending methods, the novel aspect of the invention is distilled in the second (bolded) half of the formula, as well as in the subsequent use of the second half of the formula for blending the blended graphics image with a video image. Specifically, the second half of the formula teaches the computation of a “composite alpha value” for the blended graphics image. The formula calculates the product of the set of $\{(1-A(i))\}$ for the graphics images being blended, thus using all the alpha values associated with the graphics images being blended to compute a “composite alpha value” for the blended graphics images.

RX-0313 at ¶ 46. He further testified that “[t]he Eagle reference (and the other prior art that Dr. Reinman relies on) disclosed only traditional alpha blending, as represented in the first half (but

not the second half) of the formula taught in column 45 of the patent.” *Id.* at ¶ 49.

Because the *SiRF* case settled, Broadcom’s *SiRF* brief does not create issue preclusion or judicial estoppel. *See Levi Straus & Co. v. Abercrombie & Fitch Trading Co.*, 719 F.3d 1367, 1371 (Fed. Cir. 2013) (issue preclusion requires that the issue actually be litigated); *New Hampshire v. Maine*, 532 U.S. 742, 750-51 (2001) (judicial estoppel requires that a party have succeeded in advancing its position). Still, tribunals may consider extrinsic evidence that “can help educate the court regarding the field of the invention and can help the court determine what a person of ordinary skill in the art would understand claims terms to mean.” *Philips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (*en banc*). The Commission finds that Broadcom’s *SiRF* brief and its expert’s declaration provide a helpful education on the prior art, the invention disclosed in the ’104 patent, and the differences between the claimed invention and the prior art. The Commission concludes that disclaimer in the specification, particularly when viewed in light of Broadcom’s detailed explanation and expert declaration in its *SiRF* materials, supports affirming the ID’s finding construing the limitation “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” to mean “blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.”

The Commission also finds that Broadcom’s brief and expert declaration in the *SiRF* litigation contradict Broadcom’s arguments and Dr. Havilcek’s expert testimony on claim construction in the present investigation,¹³ and finds that the contradiction undermines the credibility of Dr. Havilcek. Broadcom’s brief and expert declaration in the *SiRF* litigation are

¹³ CX-0004C (Havilcek DWS) at Q/A 43-48.

consistent with testimony of Respondents' expert, Dr. Medoff, in the present investigation,¹⁴ and the Commission finds that the testimonies of Dr. Medoff and Dr. Schonfeld are more persuasive than the testimony of Dr. Havilcek.

2. Infringement

There are two infringement issues under review: (1) whether the [] product satisfies "the blended graphics image" limitation under the Commission's modified construction; and (2) whether the [] product satisfies the "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values" limitation under the Commission's affirmance of the ID's construction. The Commission, however, did not review the ID's finding that the [] product does not satisfy the limitation "place the blended graphics image in a format suitable for blending," and thus has already found that Broadcom has not established infringement for the '104 patent.

a. "The Blended Graphics Image"

The ID found that Broadcom failed to show that the [] product satisfied the limitation "the blended graphics image" under the ID's construction of "data representing a single view of a mixture of all graphics images to be blended." ID at 60-61. The ID also found that, if the construction of "the blended graphics image" were changed to follow antecedent basis, then Broadcom successfully showed that the [] product satisfied the limitation "the blended graphics image." *Id.* at 56-57. No party petitioned for review of the ID's finding under the antecedent basis construction. Because the Commission determined to modify the ID's construction to follow antecedent basis, the Commission also affirms the ID's finding that the [] product satisfies this limitation for infringement.

¹⁴ RX-0382C (Medoff DWS) at Q/A 127-128.

b. “Blend the Blended Graphics Image with the Video Image Using the Alpha Values and/or at Least One Value Derived from the Alpha Values”

The ID found that there was no dispute that the [] products satisfied the limitation “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” under the construction adopted in the ID. ID at 66. No party petitioned for review of that finding. Because the Commission determined to affirm the ID’s construction, the Commission also affirms the ID’s finding that the [] product satisfies this limitation for infringement.

3. Technical Prong of the Domestic Industry Requirement

There are two technical prong issues under review: (1) whether the domestic industry [] product satisfies “the blended graphics image” limitation under the Commission’s modified construction; and (2) whether the domestic industry [] product satisfies the “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” limitation under the Commission’s affirmance of the ID’s construction.

a. “The Blended Graphics Image”

The ID found that Broadcom failed to show that the [] product satisfied the limitation “the blended graphics image” under the ID’s construction of “data representing a single view of a mixture of all graphics images to be blended.” ID at 79-80. The ID also found that, if the construction of “the blended graphics image” were changed to follow antecedent basis, then Broadcom successfully showed that the [] product satisfied the limitation “the blended graphics image.” *Id.* at 77-78, 80-81. No party petitioned for review of the ID’s finding under the antecedent basis construction. Because the Commission determined to modify the ID’s construction to follow antecedent basis, the Commission also affirms the ID’s finding

that the [] product satisfies this limitation for infringement under the antecedent basis construction.

b. “Blend the Blended Graphics Image with the Video Image Using the Alpha Values and/or at Least One Value Derived from the Alpha Values”

The ID found that Broadcom failed to show that the [] product satisfied the limitation “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” under his construction of “blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” ID at 84.

Broadcom contends that the ID erroneously concluded that the [] product did not satisfy this limitation even under the ID’s construction, as the evidence shows that the []

Broadcom Pet. at 76-77. Respondents argue that the ID correctly found Broadcom failed to explain how the [], and thus failed to show “blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” Respondents Resp. at 29-30.

The Commission affirms the ID’s finding that Broadcom failed to show that the [] product satisfied this limitation for the reasons set forth in the ID.

4. Invalidity

The Commission determined to review invalidity issues related to the limitations “the blended graphics image” and “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” The ID found Respondents failed to show that any claim of the ’104 patent is invalid, and the ID’s findings

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indicate that modifying the construction of “the blended graphics image” alone would not result in a finding of invalidity of any claim. Accordingly, the issue of whether any prior art reference discloses the limitation “the blended graphics image” under the modified construction has no impact on the outcome of the investigation, and the Commission has determined to take no position on the issue.

The Commission also determined to review a conditional finding on obviousness. The ID found that Respondents failed to show that any claim of the '104 patent is invalid by clear and convincing evidence under the constructions adopted in the ID. The ID found, however, if the Commission were to adopt Broadcom's constructions for both “the blended graphics image” and “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” claim 1 and 10 of the '104 patent would be invalid as obvious based on U.S. Patent No. 6,266,100 (“Gloudemans”) (RX-0073) in view of “Compositing Digital Images” (“Porter & Duff”) (RX-0244). ID at 163. The Commission, however, declined to adopt Broadcom's construction for “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” Accordingly, the issue of whether Gloudemans and Porter & Duff render claims 1 and 10 obvious under a rejected claim construction has no impact on the outcome of the investigation, and the Commission has determined to take no position on the issue.

III. CONCLUSION

For the foregoing reasons, we terminate the investigation with a finding of no violation of section 337.

PUBLIC VERSION

By order of the Commission.

A handwritten signature in black ink, appearing to read 'Lisa R. Barton'.

Lisa R. Barton
Secretary to the Commission

Issued: September 11, 2019

**CERTAIN SEMICONDUCTOR DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS CONTAINING THE SAME**

Inv. No. 337-TA-1047

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **OPINION, COMMISSION** has been served upon the following parties as indicated, on September 11, 2019.



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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

**CERTAIN SEMICONDUCTOR
DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS
CONTAINING THE SAME**

Investigation No. 337-TA-1047

**NOTICE OF COMMISSION DETERMINATION TO REVIEW IN PART A
FINAL INITIAL DETERMINATION FINDING NO VIOLATION OF
SECTION 337; SCHEDULE FOR BRIEFING; EXTENSION OF TARGET DATE**

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review in part a final initial determination (“ID”) issued by the presiding administrative law judge (“ALJ”), finding no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. 1337. The Commission has also set a schedule for briefing. Additionally, Commission has determined to extend the target date for the completion of the investigation to September 19, 2018.

FOR FURTHER INFORMATION CONTACT: Robert Needham, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, SW, Washington, D.C. 20436, telephone (202) 708-5468. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, SW, Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (<https://www.usitc.gov>). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at <https://edis.usitc.gov>. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on April 12, 2017, based on a complaint filed by Broadcom Corporation (“Broadcom”) of Irvine, California. 82 FR 17688. The complaint alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 (“section 337”), in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products

containing the same that infringe U.S. Patent Nos. 7,310,104; 7,342,967; 7,590,059; 8,068,171; and 8,284,844. *Id.* The Commission’s notice of investigation named as respondents MediaTek Inc. of Hsinchu City, Taiwan, MediaTek USA Inc. of San Jose, California, and MStar Semiconductor Inc. of ChuPei Hsinchu Hsien, Taiwan (together, “MediaTek”); Sigma Designs, Inc. of Fremont, California (“Sigma”); LG Electronics Inc. of Seoul, Republic of Korea and LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey (together, “LG”); Funai Electric Company, Ltd., of Osaka, Japan, Funai Corporation, Inc. of Rutherford, New Jersey, and P&F USA, Inc. of Alpharetta, Georgia (together, “Funai”); and Vizio, Inc., of Irvine, California (“Vizio”). *Id.* The Office of Unfair Import Investigations is not participating in this investigation. *Id.*

Several parties were terminated from the investigation based on settlement. Specifically, the Commission terminated the investigation with respect to Funai, Order No. 31 (Nov. 7, 2017), *not reviewed* Notice (Dec. 12, 2017); MediaTek, Order No. 35 (Nov. 29, 2017), *not reviewed* Notice (Dec. 19, 2017); and LG, Order No. 42 (Apr. 9, 2018), *not reviewed* Notice (May 4, 2018). Accordingly, only respondents Sigma and Vizio (together, “Respondents”) remained in the investigation at the time of the final ID.

The Commission also terminated two patents and several claims based on Broadcom’s partial withdrawal of the complaint. Specifically, the Commission terminated the investigation with respect to the ’967 patent, the ’171 patent, claims 21-30 of the ’059 patent, and claim 14 of the ’844 patent. Order No. 24 (Oct. 10, 2017), *not reviewed* Notice (Oct. 24, 2017). Broadcom also elected to withdraw claims 5 and 11-13 of the ’844 patent in its post-hearing brief. ID at 7. Accordingly, at the time of the final ID, the only remaining claims were 1, 10, 11, 16, 17, and 22 of the ’104 patent; claims 1-4, 6-10, of the ’844 patent; and claims 11-20 of the ’059 patent.

On May 11, 2018, the ALJ issued a final ID finding no violation of section 337. Specifically, he found that Respondents did not infringe any claim, that the asserted claims of the ’844 patent are invalid, and that Broadcom did not satisfy the technical prong of the domestic industry requirement for the ’104 patent.

On May 29, 2018, Broadcom and Respondents each petitioned for review of the ID. On June 6, 2018, the parties opposed each other’s petitions.

Having examined the record of this investigation, including the ALJ’s final ID, the petitions for review, and the responses thereto, the Commission has determined to review the final ID in part. Specifically, the Commission has determined to review the following issues: (1) the construction of “a processor adapted to control a decoding process” in claim 1 of the ’844 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (2) the finding that Fandrianto satisfies the limitation “adapted to perform a decoding function on a digital media stream” of claim 1 of the ’844 patent; (3) the construction of “the blended graphics image” in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; (4) the construction of “blend the blended

graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” in claim 1 of the ’104 patent, as well as related issues of infringement, invalidity, and the technical prong of the domestic industry requirement with respect to the limitation; and (5) the finding that claims 1 and 10 of the ’104 patent would be rendered obvious by Gloudemans in view of Porter & Duff under Broadcom’s proposed claim constructions.

The parties are requested to brief their positions on the issues under view with reference to applicable law and the evidentiary record. In connection with its review, the Commission is interested in briefing on the following issues:

1. Should the construction of the term “a processor adapted to control a decoding process” of the ’844 patent include the concept of “orchestrate,” and what is the difference between “control” and “orchestrate” in the context of this patent?
2. Should the construction of the term “a processor adapted to control a decoding process” of the ’844 patent include the concept of a “pipeline” or “stage”?
3. In construing the term “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” in claim 1 of the ’104 patent, under what legal theory (if any) may the Commission base its construction upon Broadcom’s arguments in the district court case *Broadcom Corp. v. SiRF Technology, Inc.*, Case No. 8:08-cv-00546-JVS-MLG (C.D. Cal. July 15, 2010)?
4. If your responses to the questions above contend that one or more of the final ID’s claim constructions should be changed, please explain how each change in claim construction would impact the issues of infringement, invalidity, and the technical prong of the domestic industry requirement.

The parties have been invited to brief only the discrete issues described above, with reference to the applicable law and evidentiary record. The parties are not to brief other issues on review, which are adequately presented in the parties’ existing filings.

In connection with the final disposition of this investigation, the Commission may (1) issue an order that could result in the exclusion of the subject articles from entry into the United States, and/or (2) issue a cease and desist order that could result in the respondent being required to cease and desist from engaging in unfair acts in the importation and sale of such articles. Accordingly, the Commission is interested in receiving written submissions that address the form of remedy, if any, that should be ordered. If a party seeks exclusion of an article from entry into the United States for purposes other than entry for consumption, the party should so indicate and provide

information establishing that activities involving other types of entry either are adversely affecting it or likely to do so. For background, see *Certain Devices for Connecting Computers via Telephone Lines*, Inv. No. 337-TA-360, USITC Pub. No. 2843 (December 1994) (Commission Opinion).

If the Commission contemplates some form of remedy, it must consider the effects of that remedy upon the public interest. The factors the Commission will consider include the effect that an exclusion order and/or a cease and desist order would have on (1) the public health and welfare, (2) competitive conditions in the U.S. economy, (3) U.S. production of articles that are like or directly competitive with those that are subject to investigation, and (4) U.S. consumers. The Commission is therefore interested in receiving written submissions that address the aforementioned public interest factors in the context of this investigation. The Commission is particularly interested in briefing on the following issue:

1. If the Commission were to issue remedial orders in this investigation, could the demand for the excluded articles be fulfilled by others?

If the Commission orders some form of remedy, the U.S. Trade Representative, as delegated by the President, has 60 days to approve or disapprove the Commission's action. See Presidential Memorandum of July 21, 2005, 70 FR 43251 (July 26, 2005). During this period, the subject articles would be entitled to enter the United States under bond, in an amount determined by the Commission and prescribed by the Secretary of the Treasury. The Commission is therefore interested in receiving submissions concerning the amount of the bond that should be imposed if a remedy is ordered.

WRITTEN SUBMISSIONS: The parties to the investigation are requested to file written submissions on the issues identified in this notice. Parties to the investigation, interested government agencies, and any other interested parties are encouraged to file written submissions on the issues of remedy, the public interest, and bonding. Such submissions should address the recommended determination by the ALJ on remedy and bonding, which issued on May 23, 2018. Broadcom is also requested to submit proposed remedial orders for the Commission's consideration. Broadcom is additionally requested to state the date that the '059, '844 and '104 patents expire, the HTSUS numbers under which the subject articles are imported, and to supply a list of known importers of the subject articles. The written submissions, exclusive of any exhibits, must not exceed 60 pages, and must be filed no later than close of business on July 27, 2018. Reply submissions must not exceed 30 pages, and must be filed no later than the close of business on August 3, 2018. No further submissions on these issues will be permitted unless otherwise ordered by the Commission.

Persons filing written submissions must file the original document electronically on or before the deadlines stated above and submit 8 true paper copies to the Office of the Secretary by noon the next day pursuant to section 210.4(f) of the Commission's Rules of Practice and Procedure (19 CFR § 210.4(f)). Submissions should refer to the investigation number ("Inv. No. 337-TA-1047") in a prominent place on the cover page

and/or the first page. (*See Handbook for Electronic Filing Procedures, http://www.usitc.gov/secretary/fed_reg_notices/rules/handbook_on_electronic_filing.pdf*). Persons with questions regarding filing should contact the Secretary (202-205-2000).

Any person desiring to submit a document to the Commission in confidence must request confidential treatment. All such requests should be directed to the Secretary to the Commission and must include a full statement of the reasons why the Commission should grant such treatment. *See* 19 C.F.R. § 201.6. Documents for which confidential treatment by the Commission is properly sought will be treated accordingly. All information, including confidential business information and documents for which confidential treatment is properly sought, submitted to the Commission for purposes of this Investigation may be disclosed to and used: (i) by the Commission, its employees and Offices, and contract personnel (a) for developing or maintaining the records of this or a related proceeding, or (b) in internal investigations, audits, reviews, and evaluations relating to the programs, personnel, and operations of the Commission including under 5 U.S.C. Appendix 3; or (ii) by U.S. government employees and contract personnel^[1], solely for cybersecurity purposes. All nonconfidential written submissions will be available for public inspection at the Office of the Secretary and on EDIS.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. 1337), and in part 210 of the Commission's Rules of Practice and Procedure (19 CFR part 210).

By order of the Commission.



Lisa R. Barton
Secretary to the Commission

Issued: July 17, 2018

^[1] All contract personnel will sign appropriate nondisclosure agreements.

**CERTAIN SEMICONDUCTOR DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS CONTAINING THE SAME**

Inv. No. 337-TA-1047

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served upon the following parties as indicated, on July 17, 2018.



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PUBLIC VERSION

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

In the Matter of

**CERTAIN SEMICONDUCTOR
DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS
CONTAINING THE SAME**

Inv. No. 337-TA-1047

FINAL INITIAL DETERMINATION

Administrative Law Judge David P. Shaw

Pursuant to the notice of investigation, 82 Fed. Reg. 17688 (Apr. 12, 2017), this is the initial determination in Certain Semiconductor Devices and Consumer Audiovisual Products Containing the Same, United States International Trade Commission Investigation No. 337-TA-1047.

It is held that no violation of section 337 of the Tariff Act, as amended, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation, of certain semiconductor devices and consumer audiovisual products containing the same, with respect to U.S. Patent Nos. 7,310,104, 7,590,059, and 8,284,844.

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TABLE OF ABBREVIATIONS

The following abbreviations may be used in this Initial Determination:

ABBREVIATION	FULL WORD OR PHRASE
ALJ	Administrative Law Judge
CDX	Complainant's Demonstrative Exhibit
CPX	Complainant's Physical Exhibit
CX	Complainant's Exhibit
Dep.	Deposition
EDIS	Electronic Document Imaging System
JX	Joint Exhibit
RDX	Respondents' Demonstrative Exhibit
RPX	Respondents' Physical Exhibit
RWS	Rebuttal Witness Statement
RX	Respondents' Exhibit
SoC or SOC	System on a Chip
Tr.	Transcript
WS	Witness Statement

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I. BACKGROUND

A. Institution of the Investigation

On March 7, 2017, complainant Broadcom Corporation filed a complaint alleging that multiple respondents unlawfully import certain semiconductor devices and consumer audiovisual products containing the same, including, without limitation, certain System-on-Chip and similar processing components and circuits used in digital televisions and other consumer audiovisual products. Compl., ¶ 1. The complaint asserted the following five patents:

- U.S. Patent No. 8,284,844 (“the ‘844 patent”);
- U.S. Patent No. 7,590,059 (“the ‘059 patent”);
- U.S. Patent No. 8,068,171 (“the ‘171 patent”);
- U.S. Patent No. 7,310,104 (“the ‘104 patent”); and
- U.S. Patent No. 7,342,967 (“the ‘967 patent”).

Id.

By publication of a notice in the Federal Register on April 12, 2017, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted this investigation to determine:

[W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products containing the same by reason of infringement of one or more of claims 1–14 of the ‘844 patent; claims 11–30 of the ‘059 patent; claims 1–5 and 7 of the ‘171 patent; claims 1, 10, 11, 16, 17 and 22 of the ‘104 patent; and claims 1–4 of the ‘967 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337[.]

82 Fed. Reg. 17688. The Commission did not direct the administrative law judge to take evidence, information, or argument regarding the public interest in this investigation. *See id.*

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The Commission named Broadcom Corporation as complainant. *Id.* The Commission named the following companies as respondents:

- MediaTek Inc.;
- MediaTek USA Inc.;
- MStar Semiconductor Inc.;
- Sigma Designs, Inc.;
- LG Electronics Inc.;
- LG Electronics U.S.A., Inc.;
- Funai Electric Company, Ltd.;
- Funai Corporation, Inc.;
- P&F USA, Inc.; and
- Vizio, Inc.

Id. The Office of Unfair Import Investigations did not participate as a party in the investigation.

Id.

B. The Private Parties

1. Broadcom

“Broadcom” is complainant Broadcom Corporation. Broadcom’s complaint provides the following background:

Founded by Henry Samueli and Henry Nicholas in 1991 in Los Angeles, California, Broadcom has grown to be a global leader in the semiconductor industry. Broadcom provides one of the industry’s broadest portfolios of highly-integrated SoCs that seamlessly deliver voice, video, data, and multimedia connectivity in the home, office, and mobile environments. From its headquarters in Irvine, California, Broadcom has expanded its footprint across the United States and around the world, employing thousands of individuals globally and in the United States. A brief

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overview of Broadcom's history can be found on its website at: <https://www.broadcom.com/company/about-us/company-history/>.

Compl., ¶ 13.

Broadcom describes itself as follows:

Broadcom is a California corporation with its principal place of business at 5300 California Avenue, Irvine, CA 92617. In 2016 it was acquired by Avago Technologies, Ltd. and currently operates as a wholly-owned subsidiary of the merged entity now known as Broadcom Limited. CX-0001C (Aberle WS) at Q/A 10-11. Broadcom's Set-Top Box Solutions is one of five major applications for Broadcom Limited's wired infrastructure segment. Broadcom's Set-Top Box Division ("STB Division") is responsible for the design, development, and distribution of complete SoC platform solutions for cable, satellite, Internet Protocol, over-the-top, and terrestrial set-top boxes. *Id.* at Q/A 13.

Broadcom Br. at 5.

2. Funai

The "Funai" respondents are Funai Electric Company, Ltd.; Funai Corporation, Inc. and P&F USA, Inc. The investigation was terminated with respect to Funai, based on a settlement. *See* Order No. 31 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 631303)).

3. LG

The "LG" respondents are LG Electronics, Inc. and LG Electronics USA, Inc. The investigation was terminated with respect to LG based on a settlement. *See* Order No. 42 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 644240)).

4. MediaTek and MStar

The "MediaTek" respondents are MediaTek Inc. and MediaTek USA Inc., and "MStar" is respondent MStar Semiconductor, Inc. The investigation was terminated with respect to

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MediaTek and MStar, based on a settlement. *See* Order No. 35 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 631859)).

5. Sigma

“Sigma” is respondent Sigma Designs, Inc. Sigma “is a corporation organized under the laws of California headquartered at 47467 Fremont Boulevard, Fremont, CA 94538 and is a provider of system on chip solutions used to enable set top boxes, smart TVs, media connectivity devices, and internet of things devices.” *See* Sigma Resp. to Am. Compl., ¶ 24. Sigma is the parent corporation for other Sigma entities. *Id.*

Sigma describes itself as follows:

Respondent Sigma is a California corporation based in Milpitas, California. It is a leading provider of SoC solutions. Sigma is the parent corporation for other Sigma entities located around the world. Sigma is an SoC supplier to downstream manufacturers. Sigma is not in the business of manufacturing downstream audiovisual products, such as TVs and set top boxes.

Resps. Br. at 1.

6. VIZIO

“VIZIO” is respondent VIZIO, Inc. VIZIO is “a California corporation with its principal place of business located at 39 Tesla, Irvine, California, 92618.” *See* VIZIO Resp. to Compl., ¶ 30. VIZIO admits that it sells televisions and displays (*e.g.*, LCD/LED flat panel TVs) in the United States, [] *Id.*; *see* Compl., ¶30.

VIZIO describes itself as follows:

Respondent VIZIO, Inc. is a leading high-definition television (HDTV) brand in America and is a California corporation headquartered in Irvine, California. []

].

Resps. Br. at 1.

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C. Procedural History

The chief administrative law judge assigned this investigation to administrative law judge Theodore R. Essex on April 6, 2017. *See* Notice to the Parties (EDIS Doc. ID No. 607770). On April 18, 2017, this investigation was reassigned to the undersigned, administrative law judge David P. Shaw. *See* Notice to the Parties (EDIS Doc. ID No. 608976).

The administrative law judge issued the procedural schedule on May 10, 2017. *See* Order No. 6 (Procedural Schedule). The procedural schedule set the target date for completion of the investigation as August 13, 2018, which is 16 months from institution. *Id.*; *see also* Order No. 5 (Setting Target Date) (citing 19 C.F.R. § 210.51(a); 19 C.F.R. § 210.42(a)(1)(i); 19 C.F.R. § 201.14(a)).

On June 1, 2017, Broadcom filed a motion seeking leave to amend the complaint and notice of investigation. Motion Docket No. 1047-010. In particular, Broadcom sought leave “to file an amended Complaint and to amend the Notice of Investigation to add the following claims against Sigma: claims 1-4 of the ‘844 patent and claims 11-30 of the ‘059 patent.” Mot. at 1. The administrative law judge granted the motion in part. *See* Order No. 12 (Broadcom was allowed to present new allegations against Sigma, but the notice of investigation was not amended because Broadcom’s motion did not seek to add additional patents or additional respondents.). On July 12, 2017, Broadcom filed an amended complaint. The parties subsequently moved to modify the procedural schedule, which was granted. *See* Order No. 17 (Amended Procedural Schedule).

In accordance with the amended procedural schedule, the parties filed claim construction briefs on August 17 and 24, 2017. *See* Order No. 6 (Procedural Schedule). The parties subsequently filed supplemental briefs pursuant to Order Nos. 21 and 22.

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On October 6, 2017, Broadcom moved to terminate the investigation in part as to the following claims:

- The '967 Patent: all asserted claims (claims 1, 2, 3, 4);
- The '059 Patent: claims 21-30;
- The '171 Patent: all asserted claims (1, 2, 3, 4, 5, 7); and
- The '844 Patent: claim 14.

The administrative law judge granted the motion in an initial determination. *See* Order No. 24 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 626698)).

On October 30, 2017, Broadcom and Funai filed a joint motion seeking to terminate the investigation with respect to Funai, based on a settlement agreement. The administrative law judge granted the motion in an initial determination. *See* Order No. 31 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 631303)).

On November 3, 2017, Broadcom and respondents MediaTek, and MStar filed a joint motion seeking to terminate the investigation with respect to MediaTek and MStar, based on a settlement agreement. The administrative law judge granted the motion in an initial determination. *See* Order No. 35 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 631859)).

A prehearing conference was held on December 6, 2017, with the evidentiary hearing beginning immediately thereafter. *See, e.g.,* Prehearing Tr. (Dec. 6, 2017); Order No. 34 (Allocation of Hearing Time). The hearing concluded on December 11, 2017. *See, e.g.,* Tr. (Dec. 6-11, 2017). The parties were requested to file post-hearing briefs not to exceed 300 pages, and to file reply briefs not to exceed 100 pages. *See* Pre-Hr'g Tr. 10-11.

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On February 28, 2017, Broadcom filed its post-hearing brief, which asserts the following claims:

- claims 1, 10, 11, 16, 17, and 22 of the ‘104 Patent;
- claims 1-4, 6-10, and 13 of the ‘844 Patent; and
- claims 11-20 of the ‘059 Patent.

See generally Broadcom Br. Pursuant to Order No. 2 (Ground Rules), the parties also submitted a joint outline of the issues to be decided in the Final Initial Determination. *See* Joint Outline of the Issues to Be Decided in the Final Initial Determination (EDIS Doc. ID No. 633530) (“Joint Outline”).

On April 3, 2018, Broadcom and the LG respondents filed a joint motion seeking to terminate the investigation with respect to LG, based on a settlement agreement. The administrative law judge granted the motion in an initial determination. *See* Order No. 42 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 644240)).

On April 5, 2018, the administrative law judge extended the target date by one month, following the Broadcom-LG settlement. *See* Order No. 41 (initial determination not reviewed per Commission Notice (EDIS Doc. ID No. 644249)).

D. The Accused Products

Broadcom argues that the accused products “are semiconductor devices and consumer audiovisual products containing those semiconductor devices.” Broadcom Br. at 8. Broadcom argues that the accused products include SoC semiconductor devices and certain televisions, Blu-ray players, and other consumer audiovisual products that contain any infringing SoCs. *Id.*

1. Sigma

Broadcom argues:

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Sigma makes SoCs. The Accused Sigma Products include, without limitation, the SX-6, SX-7, SX-8, and UXL SoCs. Acc. Prods. Stmt., Ex. E. In the Rep. Prod. Stip., Sigma identified the [] representative products. Rep. Prod. Stip. at 2.

Broadcom Br. at 8.¹

Sigma's overview of these products argues that the products do not infringe the asserted claims. *See* Resps. Br. at 12.

Based on the parties' stipulation, the administrative law judge finds that the [] products.²

2. VIZIO

Broadcom argues:

¹ On September 1, 2017, Broadcom and Sigma filed a stipulation that states: "[]" Supplement to Joint Stipulation regarding Identification of Representative Products (EDIS Doc. ID No. 621949) at 4.

² A single product may be representative of multiple products when the "products operate similarly with respect to the claimed limitation." *Spansion, Inc. v. Int'l Trade Comm'n*, 629 F.3d 1331, 1351-52 (Fed. Cir. 2010); *see also* *TiVo, Inc. v. EchoStar Commc'ns Corp.*, 516 F.3d 1290, 1308 (Fed. Cir. 2008) ("there is nothing improper about an expert testifying in detail about a particular device and then stating that the same analysis applies to other allegedly infringing devices that operate similarly, without discussing each type of device in detail."); *Kaneka Corp. v. SKC Kolon Pl, Inc.*, 198 F. Supp. 3d 1089, 1119 (C.D. Cal. 2016) ("A patentee can prove infringement by showing that just 'some samples' or even 'a sample' of the product is found to meet all the limitations of a patent's claims."). The complainant bears the burden of showing that the representative product behaves in a manner similar to the products it represents. *See Spansion*, 629 F.3d at 1332 ("Appellants contend that the ALJ improperly shifted the burden to Appellants to establish that the non-modeled accused packages would behave differently than those that were modeled. ***Rather than improper burden shifting, the ALJ properly found that Appellants simply failed to rebut the substantial evidence set forth by Tessera.***") (emphasis added); *L & W, Inc. v. Shertech, Inc.*, 471 F.3d 1311, 1318 (Fed. Cir. 2006) (the "burden of proof on infringement . . . falls on Shertech, the patentee"); *see also* *Network Protection Sciences, LLC v. Fortinet, Inc.*, 2013 WL 5402089, *2-*4 (N.D. Cal. 2013) (denying defendant's motion for summary judgment of no infringement where the defendant argued the plaintiff should have provided claim charts for each individual accused product).

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VIZIO sells televisions and other consumer audiovisual products. The Accused VIZIO Products all include a []. Acc. Prods. Stmt., Ex. F.2[.] In the Rep. Prod. Stip., VIZIO deferred to Sigma's designation of representative products. Rep. Prod. Stip. at 2.

Broadcom Br. at 8.³

VIZIO argues:

VIZIO's accused products are low-cost, high-quality televisions with []. RX-1086C.0003-0004. The technical aspects of the accused VIZIO products are [

]. *Id.* at Q8-9, Q15. VIZIO [], which are unrelated to the asserted claims. *See* RX-1086C.0003-0004.

Resps. Br. at 12.

Based on the parties' stipulation, the administrative law judge finds that VIZIO products [] are representative of VIZIO products [].

E. The Domestic Industry Products

Broadcom identified the [] as representative of its domestic industry products. *See* Broadcom Br. at 102-03, 192-93, 267. Broadcom's Reply clarifies that "the [] is representative of all of the Broadcom DI Products, which are set forth in Broadcom's Disclosure of Domestic Industry Products (July 14, 2017)." Broadcom Reply at 90; *see also* Order No. 6 at 2 (requiring Broadcom to file a list of all products it would rely upon to satisfy the domestic industry requirement). Broadcom's submission identifies the following 31 Broadcom products:

[]

³ On September 1, 2017, Broadcom and VIZIO filed a stipulation that states: "Regarding VIZIO audiovisual products[

]." Supplement to Joint Stipulation regarding Identification of Representative Products (EDIS Doc. ID No. 621949) at 4.

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[

]

Id. at 1-2 (EDIS Doc. ID No. 617271).

Respondents dispute that Broadcom has met its burden of showing that the [] is representative. *See, e.g.*, Resps. Br. at 294-95.

The administrative law judge has determined that the [] is representative of the models Broadcom has identified. Broadcom has carried its burden to show that the product upon which it relies is representative. In particular, Mr. Hellman, who has been a Broadcom engineer since 2004, and is a Distinguished Engineer in Broadcom's Set-top Box division, testified that the Broadcom SoCs in question all "have the same basic compositor function for combining video and graphics." *See* CX-0002C (Hellman WS) at Q/A 4-7, 50-58, 87-95.

While respondents have critiqued Broadcom's evidence, they offer no affirmative evidence or expert opinion demonstrating that Broadcom's domestic industry products operate differently or that specific Broadcom products do not practice claims from the '104, '844, and '059 Patents. Moreover, Mr. Hellman's testimony shows he is aware that Broadcom SoCs have been subject to revisions, and that there are differences among the various Broadcom products, yet the basic decoding and blending functionalities in Broadcom products have not changed in any relevant way, and the display and combination of video and graphics is fundamental to each of the set-top box chips. *See Id.* at Q/A 95; Hellman Tr. 55-57, 62.

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Accordingly, the administrative law judge finds that the [] is representative of Broadcom's products.

F. Technological Background

The parties filed a joint technology stipulation on August 31, 2017 (EDIS Doc. ID No. 621858).

II. JURISDICTION

Broadcom has filed a complaint alleging a violation of section 337. The Commission, therefore, has subject matter jurisdiction. *See Amgen, Inc. v. United States Int'l Trade Comm'n*, 902 F.2d 1532, 1535-37 (Fed. Cir. 1990).

In addition, Broadcom, Sigma, and VIZIO have appeared and presented evidence and arguments on the merits in this investigation. No party has contested the Commission's jurisdiction over it. The Commission, therefore, has personal jurisdiction over the parties.

The Commission also has *in rem* jurisdiction, as Sigma and VIZIO have stipulated that they import their respective accused products. *See* JX-0009C (Broadcom/Sigma Stipulation) at 2 ("Sigma shall not dispute that that the importation requirement of 19 U.S.C. § 1337(a)(1)(B) is met as to each of the Accused Products."); JX-0010C (Broadcom/VIZIO Stipulation) at 2 ("The parties to this Stipulation will not dispute that the importation requirement for this Investigation is satisfied with respect to VIZIO as to the VIZIO Televisions."); *see also Certain Male Prophylactic Devices*, Inv. No. 337-TA-546, Initial Determination (June 30, 2006) (relevant portion unreviewed). Further, the respondents have stated that "Respondents do not contest the ITC's jurisdiction in this Investigation." Resps. Br. at 12.

Accordingly, the Commission has personal, subject matter, and *in rem* jurisdiction.

III. GENERAL PRINCIPLES OF LAW

A. Claim Construction

Claim construction begins with the plain language of the claim.⁴ Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent.⁵ *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc), *cert. denied*, 546 U.S. 1170 (2006).

In some instances, claim terms do not have particular meaning in a field of art, and claim construction involves little more than the application of the widely accepted meaning of commonly understood words. *Phillips*, 415 F.3d at 1314. “In such circumstances, general purpose dictionaries may be helpful.” *Id.*

In many cases, claim terms have a specialized meaning, and it is necessary to determine what a person of skill in the art would have understood the disputed claim language to mean. “Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to ‘those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean.’” *Phillips*, 415 F.3d at 1314 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir.

⁴ Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vanderlande Indus. Nederland BV v. Int’l Trade Comm.*, 366 F.3d 1311, 1323 (Fed. Cir. 2004); *Vivid Tech., Inc. v. American Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

⁵ Factors that may be considered when determining the level of ordinary skill in the art include: “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984).

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2004)). The public sources identified in Phillips include “the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Id.* (quoting *Innova*, 381 F.3d at 1116).

In cases in which the meaning of a claim term is uncertain, the specification usually is the best guide to the meaning of the term. *Phillips*, 415 F.3d at 1315. As a general rule, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff’d*, 517 U.S. 370 (1996). The specification is, however, always highly relevant to the claim construction analysis, and is usually dispositive. *Phillips*, 415 F.3d at 1315 (quoting *Vitronics Corp. v. Conceptoronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). Moreover, “[t]he construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.” *Id.* at 1316.

Claims are not necessarily, and are not usually, limited in scope to the preferred embodiment. *RF Delaware, Inc. v. Pacific Keystone Techs., Inc.*, 326 F.3d 1255, 1263 (Fed. Cir. 2003); *Decisioning.com, Inc. v. Federated Dep’t Stores, Inc.*, 527 F.3d 1300, 1314 (Fed. Cir. 2008) (“[The] description of a preferred embodiment, in the absence of a clear intention to limit claim scope, is an insufficient basis on which to narrow the claims.”). Nevertheless, claim constructions that exclude the preferred embodiment are “rarely, if ever, correct and require highly persuasive evidentiary support.” *Vitronics*, 90 F.3d at 1583. Such a conclusion can be mandated in rare instances by clear intrinsic evidence, such as unambiguous claim language or a clear disclaimer by the patentees during patent prosecution. *Elekta Instrument S.A. v. O.U.R. Sci.*

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Int'l, Inc., 214 F.3d 1302, 1308 (Fed. Cir. 2000); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319 (Fed. Cir. 2002).

If the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence may be considered. Extrinsic evidence consists of all evidence external to the patent and the prosecution history, and includes inventor testimony, expert testimony, and learned treatises. *Phillips*, 415 F.3d at 1317. Inventor testimony can be useful to shed light on the relevant art. In evaluating expert testimony, a court should discount any expert testimony that is clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent. *Id.* at 1318. Extrinsic evidence may be considered if a court deems it helpful in determining the true meaning of language used in the patent claims. *Id.*

B. Infringement

1. Direct Infringement

Under 35 U.S.C. §271(a), direct infringement consists of making, using, offering to sell, or selling a patented invention without consent of the patent owner. The complainant in a section 337 investigation bears the burden of proving infringement of the asserted patent claims by a “preponderance of the evidence.” *Certain Flooring Products*, Inv. No. 337-TA-443, Comm’n Notice of Final Determination of No Violation of Section 337, 2002 WL 448690, at *59, (Mar. 22, 2002); *Enercon GmbH v. Int’l Trade Comm’n*, 151 F.3d 1376 (Fed. Cir. 1998).

Literal infringement of a claim occurs when every limitation recited in the claim appears in the accused device, *i.e.*, when the properly construed claim reads on the accused device

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exactly.⁶ *Amhil Enters., Ltd. v. Wawa, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir. 1996); *Southwall Tech. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed. Cir. 1995).

If the accused product does not literally infringe the patent claim, infringement might be found under the doctrine of equivalents.⁷ “Under this doctrine, a product or process that does not literally infringe upon the express terms of a patent claim may nonetheless be found to infringe if there is ‘equivalence’ between the elements of the accused product or process and the claimed elements of the patented invention.” *Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 21 (1997) (citing *Graver Tank & Mfg. Co. v. Linde Air Products Co.*, 339 U.S. 605, 609 (1950)). “The determination of equivalence should be applied as an objective inquiry on an element by element basis.”⁸ *Id.* at 40.

“An element in the accused product is equivalent to a claim limitation if the differences between the two are insubstantial. The analysis focuses on whether the element in the accused device ‘performs substantially the same function in substantially the same way to obtain the same result’ as the claim limitation.” *AquaTex Indus. v. Techniche Solutions*, 419 F.3d 1374, 1382 (Fed. Cir. 2005) (quoting *Graver Tank*, 339 U.S. at 608); accord *Absolute Software*, 659 F.3d at 1139-40.⁹

⁶ Each patent claim element or limitation is considered material and essential. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991). If an accused device lacks a limitation of an independent claim, the device cannot infringe a dependent claim. See *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n.9 (Fed. Cir. 1989).

⁷ The doctrine of equivalents is not asserted in this investigation. See Joint Outline; Broadcom Br.; Resps. Br. at 54, 132, 138, 236.

⁸ “Infringement, whether literal or under the doctrine of equivalents, is a question of fact.” *Absolute Software, Inc. v. Stealth Signal, Inc.*, 659 F.3d 1121, 1130 (Fed. Cir. 2011).

⁹ “The known interchangeability of substitutes for an element of a patent is one of the express objective factors noted by *Graver Tank* as bearing upon whether the accused device is substantially the same as the patented invention. Independent experimentation by the alleged

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Prosecution history estoppel can prevent a patentee from relying on the doctrine of equivalents when the patentee relinquished subject matter during the prosecution of the patent, either by amendment or argument. *AquaTex*, 419 F.3d at 1382. In particular, “[t]he doctrine of prosecution history estoppel limits the doctrine of equivalents when an applicant makes a narrowing amendment for purposes of patentability, or clearly and unmistakably surrenders subject matter by arguments made to an examiner.” *Id.* (quoting *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1344 (Fed. Cir. 2005)).

2. Indirect Infringement¹⁰

a) Induced Infringement

Section 271(b) of the Patent Act provides: “Whoever actively induces infringement of a patent shall be liable as an infringer.” 35 U.S.C. § 271(b).

“To prevail on a claim of induced infringement, in addition to inducement by the defendant, the patentee must also show that the asserted patent was directly infringed.” *Epcon Gas Sys. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1033 (Fed. Cir. 2002). Further, “[s]ection 271(b) covers active inducement of infringement, which typically includes acts that intentionally cause, urge, encourage, or aid another to directly infringe a patent.” *Arris Group v. British Telecomm. PLC*, 639 F.3d 1368, 1379 n.13 (Fed. Cir. 2011). The Supreme Court held that “induced infringement under § 271(b) requires knowledge that the induced acts constitute patent infringement.” *Global-Tech Appliances, Inc. v. SEB S.A.*, 563 U.S. 754, 766 (2011). The Court

infringer would not always reflect upon the objective question whether a person skilled in the art would have known of the interchangeability between two elements, but in many cases it would likely be probative of such knowledge.” *Warner Jenkinson*, 520 U.S. at 36.

¹⁰ Broadcom does not allege indirect infringement in this investigation. See generally Joint Outline; Broadcom Br.; Resps. Br. at 54, 132, 138, 236.

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further held: “[g]iven the long history of willful blindness^[11] and its wide acceptance in the Federal Judiciary, we can see no reason why the doctrine should not apply in civil lawsuits for induced patent infringement under 35 U.S.C. § 271(b).” *Id.* at 768 (footnote omitted).

b) Contributory Infringement

Section 271(c) of the Patent Act provides: “Whoever offers to sell or sells within the United States or imports into the United States a component of a patented machine, manufacture, combination or composition, or a material or apparatus for use in practicing a patented process, constituting a material part of the invention, knowing the same to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use, shall be liable as a contributory infringer.” 35 U.S.C. § 271(c).

Section 271(c) “covers both contributory infringement of system claims and method claims.”¹² *Arris*, 639 F.3d at 1376 (footnotes omitted). To hold a component supplier liable for contributory infringement, a patent holder must show, inter alia, that (a) the supplier’s product was used to commit acts of direct infringement; (b) the product’s use constituted a material part of the invention; (c) the supplier knew its product was especially made or especially adapted for

¹¹ “While the Courts of Appeals articulate the doctrine of willful blindness in slightly different ways, all appear to agree on two basic requirements: (1) the defendant must subjectively believe that there is a high probability that a fact exists and (2) the defendant must take deliberate actions to avoid learning of that fact. We think these requirements give willful blindness an appropriately limited scope that surpasses recklessness and negligence.” *Global-Tech*, 563 U.S. at 769.

¹² “Claims which recite a ‘system,’ ‘apparatus,’ ‘combination,’ or the like are all analytically similar in the sense that their claim limitations include elements rather than method steps. All such claims can be contributorily infringed by a component supplier.” *Arris*, 639 F.3d at 1376 n.8.

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use in an infringement” of the patent; and (d) the product is not a staple article or commodity of commerce suitable for substantial noninfringing use. *Id.*

C. Validity

One cannot be held liable for practicing an invalid patent claim. *See Pandrol USA, LP v. AirBoss Railway Prods., Inc.*, 320 F.3d 1354, 1365 (Fed. Cir. 2003). Nevertheless, each claim of a patent is presumed to be valid, even if it depends from a claim found to be invalid. 35 U.S.C. § 282; *DMI Inc. v. Deere & Co.*, 802 F.2d 421 (Fed. Cir. 1986).

A respondent that has raised patent invalidity as an affirmative defense must overcome the presumption by “clear and convincing” evidence of invalidity. *Checkpoint Systems, Inc. v. United States Int’l Trade Comm’n*, 54 F.3d 756, 761 (Fed. Cir. 1995).

1. Patent Eligibility

Whether patent claims are directed to subject matter that is patentable under 35 U.S.C. § 101 is an issue of law. *CLS Bank Int’l v. Alice Corp Pty.*, 717 F.3d 1269, 1276 (2013) (en banc) (citing *Bancorp Servs., LLC v. Sun Life Assurance Co. of Can.*, 687 F.3d 1266, 1273 (Fed. Cir. 2012)). “While there may be cases in which the legal question as to patentable subject matter may turn on subsidiary factual issues,” a patentee must clearly identify the fact issues that must be resolved in order to address patentability. *See In re Comiskey*, 554 F.3d 967, 975 (Fed. Cir. 2009). *Comiskey* further explains:

[T]he law remains unsettled as to whether the presumption of patent validity under 35 U.S.C. § 282 applies to subject matter eligibility challenges under 35 U.S.C. § 101.” Notice of Commission Determination (1) to Review an Initial Determination Granting Respondents’ Motion for Summary Determination that Certain Asserted Claims are Directed to Ineligible Subject Matter Under 35 U.S.C. § 101; and (2) on Review to Affirm the Initial Determination with Modification, Inv. No. 337-TA-963 (Apr. 4, 2016) (“Notice”) at 2. In its Notice, the Commission held in that instance that: “Regardless of whether or not such a presumption

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applies, the record here warrants a finding that the asserted patent claims are directed to ineligible subject matter.

Id.

Section 101 of the Patent Act sets forth four categories of patentable inventions:

“Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.” 35 U.S.C. §101; *see also Intellectual Ventures I LLC v. Capital One Bank (USA)*, 792 F.3d 1363, 1366 (Fed. Cir. 2015). The Supreme Court has recognized three exceptions to 35 U.S.C. § 101, holding ineligible for patenting “[l]aws of nature, natural phenomena, and abstract ideas.” *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 714 (Fed. Cir. 2014), *cert denied. sub nom. Ultramercial, LLC v. WildTangent, Inc.*, 135 S. Ct. 2907 (2015) (quoting *Alice Corp. Pty. Ltd. v. CLS Bank Int’l*, 134 S. Ct. 2347, 2354 (2014)) (“*Alice*”). “Patents that merely claim well-established, fundamental concepts fall within the category of abstract ideas.” *Cyberfone Sys., LLC v. CNN Interactive Grp., Inc.*, 558 Fed. Appx. 988, 991 (Fed. Cir. 2014) (citing *Bilski v. Kappos*, 561 U.S. 593, 611-12 (2010)).

An invention, however, “is not rendered ineligible for patent simply because it involves an abstract concept.” *Alice*, 134 S. Ct. at 2354 (citing *Diamond v. Diehr*, 450 U.S. 175, 187 (1981)). The courts have recognized that “[a]t some level, all inventions . . . embody, use, reflect, rest upon, or apply laws of nature, natural phenomena or abstract ideas.” *Ultramercial*, 772 F.3d at 715 (quoting *Alice*, 134 S. Ct. at 2354).

To identify claims that are ineligible, the Supreme Court has articulated a two-step test. *Genetic Techs. Ltd. v. Merial L.L.C.*, 818 F.3d 1369, 1374 (Fed. Cir. 2016). In the first step, the court must decide whether a claim is drawn to an abstract idea. *Id.* (citing *Alice*, 134 S. Ct. at

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2355). If the patent claims an abstract idea, the court in the second step seeks to identify an “‘inventive concept’ sufficient to ‘transform’ the claimed abstract idea into a patent-eligible application.” *Alice*, 134 S. Ct. at 2357 (quoting *Mayo Collaborative Servs. v. Prometheus Laboratories, Inc.*, 132 S. Ct. 1289, 1294, 1298 (2012) (“*Mayo*”). The claim limitations must disclose additional features indicating more than “well-understood, routine, conventional activity.” *Mayo*, 132 S. Ct. at 1292. The limitations must “‘narrow, confine, or otherwise tie down the claim so that, in practical terms, it does not cover the full abstract idea itself.’” *Cyberfone*, 558 Fed. Appx. at 992 (quoting *Accenture Global Servs., GmbH v. Guidewire Software, Inc.*, 728 F.3d 1336, 1341 (Fed. Cir. 2013), *cert. denied*, 134 S. Ct. 2871 (Jun. 30, 2014)).

Configuring a standard, computerized system to implement an abstract idea does not make the claimed configuration patent-eligible. Manipulation of abstractions on a computer “‘cannot meet the test because they are not physical objects or substances, and they are not representative of physical objects or substances.’” *Ultramercial*, 772 F.3d at 717 (quoting *In re Bilski*, 545 F.3d 943, 963 (Fed. Cir. 2008)); *see also Bancorp Servs.*, 687 F.3d at 1278, *cert. denied*, 134 S. Ct. 2870 (2014) (“[A]dding a ‘computer aided’ limitation to a claim covering an abstract concept, without more, is insufficient to render the claim patent eligible.”) (quoting *Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1333 (Fed. Cir. 2012)). The use of sensors does not render such a system patent-eligible. “[M]onitoring, recording, and inputting information represent insignificant ‘data-gathering steps,’ and “thus add nothing of practical significance to the underlying abstract idea.” *Wireless Media Innovations, LLC v. Maher Terminals, LLC*, 100 F. Supp.3d 405, 416 (D.N.J. 2015), *aff’d*, 636 Fed. Appx. 1014, (Fed. Cir. 2016) (quoting *CyberSource Corp. v. Retail Decisions, Inc.*, 654 F.3d 1366, 1370 (Fed. Cir. 2011)); *see also*

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OIP Technologies, Inc. v. Amazon.com, Inc., 788 F.3d 1359, 1364 (Fed. Cir. 2015), *cert. denied*, 136 S. Ct. 701 (Dec. 14, 2015) (invalidating patent implementing the abstract idea of price optimization on a generic computer); accord *Certain Activity Tracking Devices, Sys., & Components Thereof*, Inv. No. 337-TA-963, Order No. 54 at 13-14 (Apr. 27, 2016) (unreviewed).

Claims that are not merely drawn to abstract ideas implemented by the use of computers, however, may be eligible. Specifically, claims directed to improving computer functioning by the use of unconventional methods may appropriately be patented. See *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335 (Fed. Cir. 2016) (“[W]e find it relevant to ask whether the claims are directed to an improvement to computer functionality versus being directed to an abstract idea, even at the first step of the *Alice* analysis.”).

Indeed, the use of generic computer technology, however “specific” to the particular environment, will not provide eligibility, if the functionality described constitutes an abstract idea. See *TLI Comm’ns LLC v. AV Auto., LLC*, 823 F.3d 607, 611 (Fed. Cir. 2016) (“*TLP*”) (holding that 35 U.S.C. § 101 applies where “the specification makes clear that the recited physical components merely provide a generic environment in which to carry out the abstract idea of classifying and storing digital images in an organized manner”).

In *TLI*, the Federal Circuit considered and held invalid a method for uploading digital photos from a mobile device. *TLI*, 823 F.3d at 609. The Federal Circuit clarified that a relevant inquiry under step one is “whether the claims are directed to an improvement to computer functionality versus being directed to an abstract idea.” *Id.* at 612 (quoting *Enfish*, 822 F.3d at 1335). The Circuit contrasted claims “directed to an improvement in the functioning of a computer with claims ‘simply adding conventional computer components to well-known

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business practices . . . or ‘generalized steps to be performed on a computer using conventional computer activity.’” *Id.* (quoting *Enfish*, 822 F.3d at 1338).

2. Anticipation

Anticipation under 35 U.S.C. § 102 is a question of fact. *z4 Techs., Inc. v. Microsoft Corp.*, 507 F.3d 1340, 1347 (Fed. Cir. 2007). Section 102 provides that, depending on the circumstances, a claimed invention may be anticipated by variety of prior art, including publications, earlier-sold products, and patents. *See* 35 U.S.C. § 102 (*e.g.*, section 102(b) provides that one is not entitled to a patent if the claimed invention “was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States”).

The general law of anticipation may be summarized, as follows:

A reference is anticipatory under § 102(b) when it satisfies particular requirements. First, the reference must disclose each and every element of the claimed invention, whether it does so explicitly or inherently. *Eli Lilly & Co. v. Zenith Goldline Pharms., Inc.*, 471 F.3d 1369, 1375 (Fed. Cir. 2006). While those elements must be “arranged or combined in the same way as in the claim,” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008), the reference need not satisfy an *ipsissimis verbis* test, *In re Bond*, 910 F.2d 831, 832 33 (Fed. Cir.1990). Second, the reference must “enable one of ordinary skill in the art to make the invention without undue experimentation.” *Impax Labs., Inc. v. Aventis Pharms. Inc.*, 545 F.3d 1312, 1314 (Fed. Cir. 2008); *see In re LeGrice*, 49 C.C.P.A. 1124, 301 F.2d 929, 940-44 (1962). As long as the reference discloses all of the claim limitations and enables the “subject matter that falls within the scope of the claims at issue,” the reference anticipates -- no “actual creation or reduction to practice” is required. *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1380-81 (Fed. Cir. 2003); *see In re Donohue*, 766 F.2d 531, 533 (Fed. Cir. 1985). This is so despite the fact that the description provided in the anticipating reference might not otherwise entitle its author to a patent. *See Vas Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1562 (Fed. Cir. 1991) (discussing the “distinction between a written description adequate

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to support a claim under § 112 and a written description sufficient to anticipate its subject matter under § 102(b)").

In re Gleave, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

3. Obviousness

Under section 103 of the Patent Act, a patent claim is invalid "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."¹³ 35 U.S.C. § 103. While the ultimate determination of whether an invention would have been obvious is a legal conclusion, it is based on "underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *Eli Lilly and Co. v. Teva Pharmaceuticals USA, Inc.*, 619 F.3d 1329 (Fed. Cir. 2010).

The objective evidence, also known as "secondary considerations," includes commercial success, long felt need, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 13-17 (1966); *Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006). "[E]vidence arising out of the so-called 'secondary considerations' must always when present be considered en route to a determination of obviousness." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538 (Fed. Cir. 1983). Secondary considerations, such as commercial success, will not always dislodge a determination of obviousness based on analysis of the prior art. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 426 (2007) (commercial success did not alter conclusion of obviousness).

¹³ The standard for determining whether a patent or publication is prior art under section 103 is the same as under 35 U.S.C. § 102, which is a legal question. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568 (Fed. Cir. 1987).

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“One of the ways in which a patent’s subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *KSR*, 550 U.S. at 419-20. “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.*

Specific teachings, suggestions, or motivations to combine prior art may provide helpful insights into the state of the art at the time of the alleged invention. *Id.* at 420. Nevertheless, “an obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way.” *Id.* “Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* A “person of ordinary skill is also a person of ordinary creativity.” *Id.* at 421.

Nevertheless, “the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007); *see KSR*, 550 U.S. at 416 (a combination of elements must do more than yield a predictable result; combining elements that work together in an “unexpected and fruitful manner” would not have been obvious).¹⁴

¹⁴ Further, “when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious.” *KSR*, 550 U.S. at 416 (citing *United States v. Adams*, 383 U.S. 39, 52 (1966)).

4. Written Description

The issue of whether a patent is invalid for failure to meet the written description requirement of 35 U.S.C. § 112, ¶ 1 is a question of fact. *Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 670 F.3d 1171, 1188 (Fed. Cir. 2012). A patent's written description must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed. The test for sufficiency of a written description is "whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id.* (quoting *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc)).

5. Indefiniteness

The definiteness requirement of 35 U.S.C. § 112 ensures that the patent claims particularly point out and distinctly claim the subject matter that the patentee regards to be the invention. *See* 35 U.S.C. § 112, ¶ 2; *Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings*, 370 F.3d 1354, 1366 (Fed. Cir. 2004). If a claim's legal scope is not clear enough so that a person of ordinary skill in the art could determine whether or not a particular product infringes, the claim is indefinite, and is, therefore, invalid. *Geneva Pharm., Inc. v. GlaxoSmithKline PLC*, 349 F.3d 1373, 1384 (Fed. Cir. 2003).¹⁵

Thus, it has been found that:

When a proposed construction requires that an artisan make a separate infringement determination for every set of circumstances in which the composition may be used, and when such determinations are likely to result in differing outcomes (sometimes infringing and sometimes not), that construction is likely to be indefinite.

¹⁵ Indefiniteness is a question of law. *IGT v. Bally Gaming Int'l, Inc.*, 659 F.3d 1109 (Fed. Cir. 2011).

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Halliburton Energy Servs. v. M-I LLC, 514 F.3d 1244, 1255 (Fed. Cir. 2008).

The Supreme Court addressed the issue of indefiniteness, and stated that a finding of indefiniteness should not be found if the claims, “viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014) (“*Nautilus*”).

A patent is not indefinite if the claims, “viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty.” *Nautilus*, 134 S. Ct. at 2124. “If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity.” *Certain Consumer Electronics And Display Devices With Graphics Processing And Graphics Processing Units Therein*, Inv. No. 337-TA-932, Order No. 20 (Apr. 2, 2015) (quoting *Phillips*, 415 F.3d at 1327).

The burden is on the accused infringer to come forward with clear and convincing evidence to prove invalidity. *See Young v. Lumenis, Inc.*, 492 F.3d 1336, 1344 (Fed. Cir. 2007) (“A determination that a patent claim is invalid for failing to meet the definiteness requirement in 35 U.S.C. § 112, ¶ 2 is a legal question reviewed de novo.”).

D. Domestic Industry

A violation of section 337(a)(1)(B), (C), (D), or (E) can be found “only if an industry in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned, exists or is in the process of being established.” 19 U.S.C. § 1337(a)(2). Section 337(a) further provides:

(3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with

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respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned—

- (A) significant investment in plant and equipment;
- (B) significant employment of labor or capital; or
- (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(3).

These statutory requirements consist of an economic prong (which requires certain activities)¹⁶ and a technical prong (which requires that these activities relate to the intellectual property being protected). *Certain Stringed Musical Instruments and Components Thereof*, Inv. No. 337-TA-586, Comm’n Op. at 13 (May 16, 2008) (“*Stringed Musical Instruments*”). The burden is on the complainant to show by a preponderance of the evidence that the domestic industry requirement is satisfied. *Certain Multimedia Display and Navigation Devices and Systems, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-694, Comm’n Op. at 5 (July 22, 2011) (“*Navigation Devices*”).

1. Economic Prong

With respect to the economic prong, and whether or not section 337(a)(3)(A) or (B) is satisfied, the Commission has held that “whether a complainant has established that its

¹⁶ The Commission practice is usually to assess the facts relating to the economic prong at the time that the complaint was filed. See *Certain Coaxial Cable Connectors and Components Thereof and Products Containing Same*, Inv. No. 337-TA-560, Comm’n Op. at 39 n.17 (Apr. 14, 2010) (“We note that only activities that occurred before the filing of a complaint with the Commission are relevant to whether a domestic industry exists or is in the process of being established under sections 337(a)(2)-(3).”) (citing *Bally/Midway Mfg. Co. v. U.S. Int’l Trade Comm’n*, 714 F.2d 1117, 1121 (Fed. Cir. 1983)). In some cases, however, the Commission will consider later developments in the alleged industry, such as “when a significant and unusual development occurred after the complaint has been filed.” See *Certain Video Game Systems and Controllers*, Inv. No. 337-TA-743, Comm’n Op., at 5-6 (Jan. 20, 2012) (“[I]n appropriate situations based on the specific facts and circumstances of an investigation, the Commission may consider activities and investments beyond the filing of the complaint.”).

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investment and/or employment activities are significant with respect to the articles protected by the intellectual property right concerned is not evaluated according to any rigid mathematical formula.” *Certain Printing and Imaging Devices and Components Thereof*, Inv. No. 337 TA 690, Comm’n Op. at 27 (Feb. 17, 2011) (“*Printing and Imaging Devices*”) (citing *Certain Male Prophylactic Devices*, Inv. No. 337 TA-546, Comm’n Op. at 39 (Aug. 1, 2007)). Rather, the Commission examines “the facts in each investigation, the article of commerce, and the realities of the marketplace.” *Id.* “The determination takes into account the nature of the investment and/or employment activities, ‘the industry in question, and the complainant’s relative size.’” *Id.* (citing *Stringed Musical Instruments* at 26).

With respect to section 337(a)(3)(C), whether an investment in domestic industry is “substantial” is a fact-dependent inquiry for which the complainant bears the burden of proof. *Stringed Musical Instruments* at 14. There is no minimum monetary expenditure that a complainant must demonstrate to qualify as a domestic industry under the “substantial investment” requirement of this section. *Id.* at 25. There is no need to define or quantify an industry in absolute mathematical terms. *Id.* at 26. Rather, “the requirement for showing the existence of a domestic industry will depend on the industry in question, and the complainant’s relative size.” *Id.* at 25-26.

2. Technical Prong

“With respect to section 337(a)(3)(A) and (B), the technical prong is the requirement that the investments in plant or equipment and employment in labor or capital are actually related to ‘articles protected by’ the intellectual property right which forms the basis of the complaint.” *Stringed Musical Instruments* at 13-14. “The test for satisfying the ‘technical prong’ of the industry requirement is essentially same as that for infringement, *i.e.*, a comparison of domestic

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products to the asserted claims.” *Alloc, Inc. v. Int’l Trade Comm’n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). “With respect to section 337(a)(3)(C), the technical prong is the requirement that the activities of engineering, research and development, and licensing are actually related to the asserted intellectual property right.” *Stringed Musical Instruments* at 13.

IV. U.S. PATENT NO. 7,310,104

A. Overview of the ‘104 Patent

The ‘104 Patent (JX-0003), entitled “Graphics display system with anti-flutter filtering and vertical scaling feature,” issued on December 18, 2007. The application that would issue as the ‘104 Patent, Application No. 11/511,042, was filed on August 28, 2006, and is a continuation of several applications that claim priority to Provisional Application No. 60/107,875 (filed on November 9, 1998). The ‘104 Patent discloses a circuit for generating a blended graphics image.

B. Claim Construction

1. Level of Ordinary Skill in the Art

Broadcom’s expert, Dr. Havlicek, testified as follows:

Q17. Have you formed an opinion as to what the level of ordinary skill would have been for a person of ordinary skill in the art at the time of the invention of the ‘104 patent?

A. Yes.

Q18. And what is that opinion?

A. My opinion is that a person of ordinary skill in the art at the time of the invention of the ‘104 patent would have had a Bachelor’s Degree in Electrical Engineering, Computer Science, or a similar discipline, with one to two years of experience in this or a related field. The person of ordinary skill in the art would also have been familiar with software or hardware related to digital signal image and video processing.

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Q19. Have you formed an opinion as to the definition for a person of ordinary skill in the art that the Respondents have proposed?

A. Yes.

Q20. And what is that opinion?

A. My opinion is Respondents' definition for a person of ordinary skill in the art is similar to my definition and if Respondents' proposed definition were adopted, it would not change any of my opinions regarding the '104 patent.

CX-0004C (Havlicek WS) at Q/A 17-20.

Respondents argue:

One of ordinary skill would have had a Bachelor's degree in Electrical Engineering, or Computer Science, and at least two years of experience in the field of graphics and image and video processing, or an equivalent degree and/or experience. Superior education would compensate for a deficiency in experience, and vice-versa. Dr. Medoff agreed that the level of skill he proposed for the '104 Patent was "broadly similar" to Broadcom's. Tr. (Medoff) at 708:21-25; CX-0004C (Havlicek) Q18.

Resps. Br. at 188.

Broadcom replies: "[t]he differences between the levels of ordinary skill in the art proposed by Broadcom and Respondents are minimal and do not effect analyses in this Investigation." Broadcom Reply at 2.

In view of the subject matter of the patent, and the expert testimony on this issue, the administrative law judge has determined that a person of ordinary skill in the art, at the time of the invention, would have had a bachelor's degree in electrical engineering, computer science, or a similar discipline, with one to two years of experience in image processing or a related field. The person of ordinary skill in the art would also have been familiar with software or hardware related to digital signal image and video processing. *See* CX-0004C (Havlicek WS) at Q/A

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17-20. Dr. Medoff's opinion did not differ substantially from that of Dr. Havlicek. *See* Medoff Tr. 708.

2. Agreed Constructions

The parties have submitted three agreed constructions, as follows:

Claim Term	Relevant Claims	Agreed Construction
"video image"	1, 11, and 17	"data representing a single view from a continuous feed of views transmitting a still or moving picture"
"graphics image"	1, 10, 11, 16, 17, and 22	"data representing a single view of image content including text, graphical pictures, patterns, and the like"
"a plurality of alpha values associated with the graphics images"	1, 11, and 17	"two or more alpha values associated with the graphics images"

Broadcom Br. at 22; CX-0004C (Havlicek WS) at Q/A 15; Resps. Br. at 188-89;

RX-0304.00010-14 (Final Order on Special Master's Report).

Respondents note that Broadcom asserted the '104 Patent against *SiRF* Technology in 2008. Resps. Br. at 188. Respondents report that the U.S. District Court for the Central District of California construed several terms of the '104 Patent claims and that the parties have agreed to construe the above terms "precisely as the *SiRF* Court construed them." *Id.* (citing RX-0304 (*Broadcom Corp. v. SiRF Tech., Inc.*, 8:08-cv-00546-JVS-MLG, Doc. No. 289, Final Order re Special Master's Report and Recommendations Concerning Claim Construction (July 15, 2010)).

3. Disputed Constructions

The parties present three claim construction issues for resolution:

- Construction of the terms "a blended graphics image," "the blended graphics image," and "blended graphics image"
- Whether the claimed steps must be performed to completion in order

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- Construction of the phrases: “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” / “blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values”

Joint Outline at 1-2; Broadcom Br. at 22-27; Resps. Br. at 189-201.

a) *“a blended graphics image,” “the blended graphics image,” and “blended graphics image”*

Broadcom argues that the term “blended graphics image” has an agreed construction and that separate constructions for the terms “a blended graphics image” and “the blended graphics image,” are not necessary. Broadcom Br. at 23. Respondents argue that construing the terms separately avoids reading the “requirement that first all graphics must be blended together before blending with the video image” out of the claim. Resps. Br. at 189.

The administrative law judge has determined that separate consideration is warranted, as the indefinite article “a” and the definite article “the” affect the scope of the claim, and the issues in this investigation.

(1) “blended graphics image”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
data representing a single view of a mixture of at least two graphics images	Respondents do not offer a construction for “blended graphics image” apart from the indefinite and definite articles that always precede the term.

See Broadcom Br. at 22; *see generally* Resps. Br. at 189-97. In reply, Broadcom focuses its argument on the differences between the terms “a blended graphics image” and “the blended graphics image.” Broadcom Reply at 3.

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The administrative law judge has determined it is not necessary to construe the term “blended graphics image” in isolation, without considering the definite and indefinite articles that always precede the term. The ‘104 Patent uses the words “blended graphics image” 26 times, and the words appear in the specification twice. *See generally* JX-0003. The words “blended graphics image” are always preceded by an indefinite article or definite article. *Id.* at 44:39-46, 60:45-62:52. Accordingly, the administrative law judge declines to adopt Broadcom’s argument that the term “blended graphics image” warrants its own construction. *See Phillips*, 415 F.3d at 1314 (quoting *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) for the proposition that “the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms”); *see also Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 (Fed. Cir. 2017) (considering the context of the surrounding words and citing *ACTV v. Walt Disney*).

(2) “a blended graphics image,”

Although Broadcom argues that a separate construction is not necessary, the parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
data representing a single view of a mixture of at least two graphics images	data representing a single view of a mixture of at least two graphics images

See Broadcom Br. at 22-23 (Broadcom argues that “A separate construction is not necessary.”); Resps. Br. at 190. In its reply, Broadcom notes that “[a]ll parties agree that the term ‘a blended

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graphics image’ should be construed as ‘data representing a single view of a mixture of at least two graphics images.’” Broadcom Reply at 3.¹⁷

The administrative law judge finds that in view of the parties’ dispute concerning the use of an article in connection with “blended graphics image,” it is necessary to construe “a blended graphics image.” The administrative law judge construes the phrase “a blended graphics image” to mean “data representing a single view of a mixture of at least two graphics images.”

Claims 1, 11, and 17 use the term “a blended graphics image.” *See* JX-0003 at 60:45-62:52. Respondents argue that claim 1 is representative, and Broadcom argues that “‘a blended graphics image’ and ‘the blended graphics image’ are used consistently throughout the claims and in all instances[.]” Broadcom Br. at 23; Resps. Br. at 190. Claim 1 of the ‘104 Patent, which Broadcom divides into six limitations, follows:

1. [A] One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:

[B] at least one interface operable to receive one or both of video and audio; and

[C] at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:

[D] blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate ***a blended graphics image*** for storage in the at least one memory,

[E] process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

¹⁷ The *SiRF* Court provides a discussion of the terms “graphics,” “video image,” “graphics image,” “a blended graphics image,” and “the blended graphics image” that is relevant background to the parties’ arguments. *See* RX-0304 at 3-14.

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[F] blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

JX-0003 at 60:45-63 (emphasis added). The claim requires a processor capable of blending a plurality of graphics images—*i.e.*, at least two images—to generate a blended graphics image.

Id. Further, the parties’ proposed construction, which is adopted by the administrative law judge, does not impermissibly enlarge or narrow the claim scope.

(3) “the blended graphics image,”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
data representing a single view of a mixture of at least two graphics images	data representing a single view of a mixture of all graphics images to be blended

See Broadcom Br. at 22-23 (Broadcom argues that “A separate construction is not necessary.”);

Resps. Br. at 197.

Broadcom argues, in part:

The term “the blended graphics image” merely refers to back to “a blended graphics image” or data representing a single view of a mixture of at least two graphics images. Under the basic canons of claim construction, “a claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent.” . . .

In fact, “a blended graphics image” and “the blended graphics image” are used consistently throughout the claims and in all instances, mean data representing a single view of a mixture of at least two graphics images. [CX-0004C (Havlicek WS)] at Q/A 26. Specifically, the ‘104 Patent states that the blended graphic image can be blended with video and then additional blended graphic images can subsequently be blended with the video as discussed at column 32, lines 48-53 of the ‘104 Patent: “[t]he graphical elements are displayed on the TV screen by compositing the display buffer containing the graphical elements with optionally

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other graphics and video contents while blending the subject display buffer with all layers behind it using the alpha per pixel values created in the preceding steps.” CX-0004C (Havlicek WS) at Q/A 31.

Broadcom Br. at 23-24. Broadcom, and its expert, Dr. Havlicek, point to FIGS. 5 and 28 of the ‘104 Patent and additional sections in the specification (*e.g.*, col. 32, ll. 48-54 and col. 45, ll. 25-30) in arguing that the patent teaches “the blended graphics image can be blended with video and then additional blended graphic images” rather than requiring a scheme where all graphics images must be blended together before they are blended with video. Broadcom Br. at 23-25 (“Nowhere does the patent require that the graphics must be *all* blended together first, then only after you blend all the graphics together do you blend this blended graphics image with the video.”).

Respondents argue that the claim language, the specification, the prosecution history, Broadcom’s counsel’s description of the ‘104 Patent, and the *SIRF* Court’s claim construction order all support respondents’ proposed construction. Resps. Br. at 190-97.

Broadcom replies that the term “a blended graphics image” is the antecedent for “the blended graphics image,” and that “the blended graphics image” must receive the same construction under “the well-settled law of antecedent basis.” Broadcom Reply at 4 (citing *Wi-Lan, Inc. v. Apple, Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016) (“Subsequent use of the definite articles ‘the’ or ‘said’ in a claim refers back to the same term recited earlier in the claim.”)).

With regard to the specification, Broadcom also argues:

The ‘104 Patent specification never states that the only way to perform the claimed invention is to first blend all graphics images, then to blend this final graphics image with video, as Respondents suggest. Rather, the specification states that the graphics system disclosed an efficient solution that blends together a group of graphics images that will all receive common processing, applying that processing once to the group (as opposed to once to each

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graphics image in the group), and then blending the processed group with a video image. JX-0003 ('104 Patent) at 45:25-30; CX-0004C (Havlicek WS) at Q/A 31. This sequence may be repeated where there is a plurality of groups that would receive a distinct processing common to the group and then blended with a single video image. *Id.*

Id. (emphasis omitted). Apart from citing col. 45, ll. 47-62 of the '104 Patent, Broadcom cites the same evidence and presents similar argument from its post-hearing brief. *Compare* Broadcom Br. at 22-25 (citing JX-0003 at 32:48-53 and 45:25-30; CX-0004C (Havlicek WS) at Q/A 22-35) *with* Broadcom Reply at 5 (citing JX-0003 at 45:47-62 in addition to *id.* at 32:48-53 and 45:25-30; CX-0004C (Havlicek WS) at Q/A 22-35).

With respect to the prosecution history, Broadcom argues that “the claims were allowed not because all graphics are first blended together and then blended with video, as Respondents suggest, but instead because two or more graphics were blended together before being blended with video.” Broadcom Reply at 6 (emphasis omitted). Broadcom argues:

The prior art considered by the Examiner in both the original prosecution, and in the reexamination fell into two main categories. The Category A prior art included blending graphics together in a one-step method without blending these graphics with video. CX-0578C (Havlicek WS) at Q/A 28-30 and 39-65. The Category B prior art took single graphics (not blended graphics) and then blended these single graphics with video in a one-step method. *Id.* The claims were allowed over both Category A and B references because the '104 Patent family was the first to blend any graphics images together prior to blending this blended graphic with video. RX-0216 ('930 Patent F.H.); JX-0006 ('104 Patent F.H.); RX-0216 (Reexam F.H.).

Id. (emphasis omitted). Broadcom argues that it argued, and the Examiner accepted, that the claims were patentable “not because they required blending all graphics prior to blending this blending graphic with video, but because they recited blending together two or more graphics (“a

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blended graphics image”) and then blending that blended graphic with video.” *Id.* at 7-8 (citing RX-0216.00026-27 and RX-0231.0031-34).

The administrative law judge construes “the blended graphics image” to mean “data representing a single view of a mixture of all graphics images to be blended” (which is respondents’ proposed construction). The claim language, the specification, and the prosecution history support the construction.

The language of claim 1 presents a coherent, self-standing paradigm for blending graphics and video images. For example, graphics images are blended into a blended graphics image in limitation [D], the blended graphics image is placed in a format suitable for blending with video in limitation [E], and the blended graphics image is blended with video in limitation [F]. Additionally, none of the claims, independent or dependent, contemplate an additional step of blending a second blended graphics image with video. *See Harris Corp. v. Fed. Exp. Corp.*, 502 F. App’x 957, 963 (Fed. Cir. 2013) (construing the phrase “transmitting the accumulated, stored generated aircraft data” to mean “transmitting **all** the aircraft data that has been accumulated or stored or generated” (bolding added) and noting that “although the claim does not expressly require that ‘all’ of the accumulated data must be transmitted, it similarly lacks any indication that some subset of the accumulated data should be transmitted, and if so what that subset should be.”).

With regard to Broadcom’s antecedent-basis argument, Broadcom argues that the words “blended graphics image” require consistent (*i.e.*, identical) treatment, particularly given “the well-settled law of antecedent basis.” *See* Reply at 3-4 (citing *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001); *Wi-Lan, Inc. v. Apple, Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016) (“Subsequent use of the definite articles ‘the’ or ‘said’ in a claim refers back to the same

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term recited earlier in the claim.”)). However, the Federal Circuit has noted that “the same claim term can have different constructions depending upon the context of how the term is used within the claims and specification.” *Aventis Pharm. Inc. v. Amino Chemicals Ltd.*, 715 F.3d 1363, 1374 (Fed. Cir. 2013) (citing *Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008) (“the patentee’s mere use of a term with an antecedent does not require that both terms have the same meaning.”)). Thus, the analysis is not as preordained as Broadcom suggests.

The specification also supports construing “the blended graphics image” to mean “data representing a single view of a mixture of all graphics images to be blended” (which is respondents’ proposed construction). The ‘104 Patent discusses blending in Section X, which is titled “Blending of Graphics and Video Surfaces.” *See* JX-0003 at 44:26-50:9. The beginning of Section X explains:

The graphics display system *of the present invention* is capable of processing an analog video signal, a digital video signal and graphics data simultaneously. In the graphics display system, the analog and digital video signals are processed in the video display pipeline while the graphics data is processed in the graphics display pipeline. After the processing of the video signals and the graphics data have been completed, they are blended together at a video compositor. The video compositor receives video and graphics data from the video display pipeline and the graphics display pipeline, respectively, and outputs to the video encoder (“VEC”).

The system may employ a method of compositing a plurality of graphics images and video, which includes blending the plurality of graphics images into a blended graphics image, combining a plurality of alpha values into a plurality of composite alpha values, and blending the blended graphics image and the video using the plurality of composite alpha values.

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Id. at 44:27-46 (emphasis added).¹⁸ Section X then discusses “a process of blending video and graphics surfaces,” as depicted in FIG. 28, as follows:

Referring to FIG. 28, a flow diagram of a process of blending video and graphics surfaces is illustrated. The graphics display system resets in step 902. In step 904, the video compositor blends the passthrough video and the background color with the scaled video window, using the alpha value which is associated with the scaled video window. The result of this blending operation is then blended with the output of the graphics display pipeline. The graphics output has been pre-blended in the graphics blender in step 904 and filtered in step 906, and blended graphics contain the correct alpha value for multiplication by the video output. The output of the video blend function is multiplied by the video alpha which is obtained from the graphics pipeline and the resulting video and graphics pixel data stream are added together to produce the final blended result.

Id. at 44:47-62.¹⁹ The specification then discusses processes for “blending graphics windows into a combined blended graphics output” and “blending graphics, video and background color” in relation to FIGS. 29 and 30, as follows:

Referring to FIG. 29, a flow diagram of a process of blending graphics windows is illustrated. The system preferably resets in step 920. In step 922, the system preferably checks for a vertical

¹⁸ Respondents contend that the phrase “the present invention” in Section X limits the claims. *See* Resps. Br. at 191-92 (citing *Verizon Service Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007)). The specification, however, does not uniformly characterize the cited portion of the specification (JX-0003 at 44:28-38) as “the present invention.” *See Absolute Software, Inc. v. Stealth Signal, Inc.*, 659 F.3d 1121, 1136 (Fed. Cir. 2011) (“... we have found that use of the phrase ‘present invention’ or ‘this invention’ is not always so limiting, such as where the references to a certain limitation as being the ‘invention’ are not uniform, or where other portions of the intrinsic evidence do not support applying the limitation to the entire patent.”). For example, the “Field of the Invention,” “Summary of the Invention,” and numerous sections of the “Detailed Description of the Invention” refer to “the present invention.” *See generally* JX-0003.

¹⁹ Broadcom argues that the phrase “In step 904, . . .” contains a typo and that “step 904” should read “step 908.” *See* Broadcom Br. at 25, n.4. Respondents contend that there is no typo. *See* Resps. Br. at 10, n.2. In 2010, the *SiRF* Court stated that it “appears to be a typographical error that should refer to step 908.” *See* RX-0304 at 14 n.8. Despite knowing of this error for many years, Broadcom has not specified how it attempted to correct the error.

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sync (VSYNC). If a VSYNC has been received, the system in step 924 preferably loads a line from the bottom most graphics window into a graphics line buffer. Then the system in step 926 preferably blends a line from the next graphics window into the line buffer. Then the system in step 928 preferably determines if the last graphics window visible on a current display line has been blended. If the last graphics window has not been blended, the system continues on with the blending system in step 926.

...

Referring to FIG. 30, a flow diagram of a process of receiving blended graphics 950, a video window 952 and a passthrough video 954 and blending them. A background color preferably is also blended in one embodiment of the present invention. As step 956 indicates, the video compositor preferably displays each pixel as they are composited without saving pixels to a frame buffer or other memory.

When the video signals and graphics data are blended in the video compositor, the system in step 958 preferably displays the passthrough video 954 outside the active window area first. . . .

Within the active window area, the system in step 960 preferably blends the background color first. . . . Finally, the system in step 968 blends the graphics window on top of the composited video window and outputs composited video 970 for display.

JX-0003 at 2:60-64, 48:12-60.

These portions of the specification support construing “the blended graphics image” to include all graphics images to be blended, as the processes described in FIGS. 28-30 specify that all graphics blending is done prior to blending with the video image. While Broadcom points to JX-0003 at 45:25-30, 45:47-62, and 32:48-53, these portions of the specification do not suggest that graphics groups may be separately processed and blended with the same video image.

The prosecution history also supports the construction. In a parent application (Appl. No. 11/097,028, which issued as U.S. Patent No. 7,098,930), the applicant argued that claim 1 was

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patentable over Mills (U.S. Patent No. 5,923,385) and Dye (U.S. Patent No. 6,108,014). The rejected claim follows:

1. (Original) A display system comprising:

a graphics processing system for blending a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image, wherein the graphics processing system also processes the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image;

a memory for storing the blended graphics image; and

a compositor for blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

RX-1392 at 3. The applicant argued claim 1 was patentable over the combination of Mills and Dye because the combination did not teach every limitation. *Id.* at 7-8. In particular, the applicant explained:

... claim 1 of the present application is directed to a two step process of blending. First, the graphics images are blended using the associated alpha values to generate a blended graphics image, wherein the graphics processing system also processes the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image. Secondly, the blended graphics image is then blended with the video image using the alpha values and/or at least one value derived from the alpha values. ***This way, the graphic images can first be processed together by the graphics processor separately/differently from the video, which is not necessarily processed by the graphics processor.*** The blended graphics image in a format suitable for blending with a video image, is then blended with the video. Also, the blended graphics image is blended with the video using the alpha values and/or at least one value derived from the alpha values.

FIG. 2A and Col. 13, lines 24-49 of Mills cited by the Examiner discloses only one step blending. ... There is no teaching or suggestion that any of the graphics images are first blended, and later blended with a video.

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RX-1392 at 8-9 (underlining in original, bold and italics added).

This passage demonstrates how the applicant understood the invention and informs the meaning of the claim language. *Phillips*, 415 F.3d at 1317 (“the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.”).²⁰ In particular, in describing the purpose of the two-step process so that the graphics images can “be processed together,” the applicant indicated that all of the graphics images to be blended so that “this way” they can be processed at the same time, which informs the construction. Broadcom notes that the applicant later argued that “any of the graphics images are first blended, and later blended with a video,” *see* Broadcom Reply at 6-7. This, however, does not support Broadcom’s suggestions that the specification discloses an iterative, multi-step, or some other unannounced process.

Broadcom further relies on expert testimony to advance their arguments. Given that Broadcom’s expert’s testimony essentially dovetails with its arguments, the administrative law judge finds that this extrinsic evidence is not particularly significant, vis-à-vis the intrinsic record, when “determining ‘the legally operative meaning of claim language.’” *See Phillips*, 415 F.3d at 1317.

b) Whether the claimed steps must be performed to completion in order

Respondents argue:

²⁰ Respondents argue that Broadcom disavowed claim scope in responding to the obviousness objection. It is not necessary, however, to find whether the applicant’s statements were a clear and unambiguous surrender of scope, because the statements inform, and are sufficient to support, the construction Respondents have proposed.

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A proper construction of “a blended graphics image” and “the blended graphics image” requires that each step in claims 1, 11, and 17 is performed in the order recited in the claims. Each claim requires that “the blended graphics image” that is to be blended with the video image is the final graphics blend of any graphics to be blended. All graphics blending steps occur before any blending with video. As explained above, the specification and prosecution history require that the claims are construed so that the claimed order of steps is limiting – meaning that all graphics images to be blended with a video image are first blended before blending with a video image.

Respondents expect Broadcom to argue that the steps in the independent claims may occur in any order. Broadcom’s position is directly contradicted by the plain language in the independent claims and the examples and figures in the specification. . . .

Resps. Br. at 197.

In the Joint Outline, Broadcom indicates that it has briefed this issue on page 22 of its Post-Hearing Brief. *See* Joint Outline at 1. Broadcom’s brief, however, does not address this issue. *See generally* Broadcom Br., Section IV(B)(1).

In reply, Respondents argue:

Broadcom does not dispute Respondents’ contention that the claimed steps must be performed to completion in order. CPostHg. Br. at ii, 22-27. Therefore, “‘the blended graphics image’ that is to be blended with the video image is the final graphics blend of any graphics to be blended. All graphics blending steps occur before any blending with video.” RX-0058.0005.

Resps. Reply at 18.

Broadcom’s reply does not address the issue. *See generally* Broadcom Reply, Section II(B) (respondents’ argument is not addressed).

The administrative law judge has determined that “a blended graphics image” and “the blended graphics image” must be construed to require that each step in claims 1, 11, and 17 is performed in the order recited in the claims for the reasons provided in respondents’ brief,

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especially because the claims require the graphics image to be blended with video to be a graphics image that has itself already been “blended,” *i.e.*, “blended graphics image.” In this context, it makes sense that each step in claims 1, 11 and 17 must be performed in order and to completion. Furthermore, this ordering requirement does not change the constructions of “a blended graphics image” and “the blended graphics image” that are discussed above.

- c) *“blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” / “blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values”*

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image

See Broadcom Br. at 26; Resps. Br. at 201.

Broadcom’s argument is:

This term does not need to be construed, as it is clear and would have had a well-understood meaning to a POSA at the time of the invention, and there is no need to further construe the phrase or use other words to explain what the phrase means. CX-0004C (Havlicek WS) at Q/A 43-46. In light of the claim language and the specification of the ‘104 Patent, a POSA would understand that the alpha values associated with the graphic images that were blended to form the blended graphics image may be used to blend the blended graphics image with the video image. *Id.* Indeed, this is exactly what the claim says. Nothing in the specification or file history contradicts this well-known meaning.

Broadcom Br. at 26-27.

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Respondents argue that the applicant acted as his own lexicographer and disclaimed scope in disclosing a particular formula for blending graphics. Resps. Br. at 198-99.

Respondents argue:

The allegedly novel blending method of the '104 Patent relies, in part, on generating a composite alpha value. As graphics images are blended together, the composite alpha value is updated. The specification describes that "at each stage of the blending, an intermediate alpha value is maintained for later use for blending with the layers that are not to be filtered (referred to as the "lower" layers)." JX-0003 at 45:46-49. In other words, the specification describes updating a composite alpha value while blending the graphics images together and using that composite alpha value to perform the final blending of the blended graphics image to the video image. The patent discloses the blending formula. In particular, the formula for generating the composite alpha value is disclosed as the second half:

$$R(i)=A(i)*P(i)+(1-A(I))*P(i-1)$$

and

$$AR(i)=AR(i-1)*(1-A(i)).$$

Id. at 45:46-57 (emphasis added). The composite alpha value is the result of the "calculation of the product of the set of $\{(1-A(i))\}$ for the upper layers" *Id.* at 46:11-14. The specification's formula makes clear that the blending of the blended graphics image and video image must use the composite alpha value, and the composite alpha value is "[t]he calculation of the product of the sets of $\{1-A(i)\}$ " *Id.* at 46:18-20. As the graphics images are blended to create the blended graphics images, "by repeatedly calculating $AR(i)=AR(i-1)*(1-A(i))$ at each layer, such that when all layers $\{i\}$ have been processed, the result is that AR =the product of all $(1-A(i))$ values for all upper layers." *Id.* at 46:20-23; *see also id.* at 5:18-24 ("The display engine ... blends the graphics windows to create blended graphics output having a composite alpha value that is based on alpha values for individual graphics windows, alpha values per pixel, or both."). Thus, the composite alpha value is "derived from the product of one minus the alpha value for every graphics image," as Respondents propose.

After blending the graphics images together and generating the composite alpha value, "the $AR(n)$ value at each pixel that results

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from the blending of the upper layers and any subsequent processing is used to be multiplied with the composite lower layer.” *Id.* at 46:41-43. In other words, the composite alpha value is used to blend the blended graphics images (upper layers) with the video image (composite lower layer). Thus, the specification discloses using the composite value (or AR(n)) to blend the final blended graphics image to the video image.

Resps. Br. at 199-200. Respondents then argue that “Broadcom emphasized the difference between the ‘104 Patent and conventional methods of blending in the *SiRF* litigation[.]” *Id.* at 200.²¹

Broadcom’s entire reply follows:

Respondents ignore the broad claim language and instead, limit the claims to a specific embodiment. Respondents argue that the claim term “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” should be limited to “blend[ing] the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” RPostHB at 198-201. Respondents’ proposed claim construction should be rejected.

First, Respondents’ proposed construction requiring only “an alpha value” is contrary to the ‘104 Patent and the claim language (“using the alpha values”), which discloses that there may be a plurality of alpha values associated with a single graphics image. CX-0004C (Havlicek WS) at Q/A 43-46. This is supported at least in col. 45, ll. 4-5 of the ‘104 Patent that states that “[t]he alpha values {A(i)} are in general different for every layer for every pixel of every layer.”

Second, Respondents’ construction improperly eliminates words from the claim language itself. Specifically, Respondents ignore the claim language of “using the alpha values and/or at least one value derived from the alpha values.” *Id.*

²¹ In the *SiRF* litigation, Broadcom argued that “[t]he novel aspect of the invention is distilled in the second half of the formula. . . . when blending two images according to the above formula, the images are blended by mixing the alpha value of the pixel of one image with the alpha value of the corresponding pixel of the next image. . . . It is the second part of the formula set out above that teaches the computation of a ‘composite alpha value’ for the blended graphics image.” RX-0311 at 7 (Broadcom’s Opposition to Defendants’ Motion for Summary Judgment).

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Third, nothing in the intrinsic evidence supports Respondents attempt to add the limitation of “the product of one minus the alpha value for every graphics image” to the claim language. *Id.* at Q/A 43-46. While Respondents’ proposed construction is taken from the equation which appears in column 45 of the ‘104 Patent, it is applicable only to a single embodiment, and may be a per pixel alpha value, per image alpha value, per region alpha value, etc. *Id.* Other embodiments in the ‘104 Patent may derive blending values from the alpha values in different ways. *Id.* In alternate embodiments, the equation for AR(i) must also be changed relative to the preferred embodiment. *Id.* In such cases the blending value AR(i) would no longer be derived from “the product of one minus the alpha value for every graphics image” but would instead take some other form. *Id.* Accordingly, Respondents’ construction of this limitation should be rejected.

Broadcom Reply at 10-11.

The administrative law judge construes the phrases “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” and “blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” to mean “blending the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image” (which is respondents’ construction). Broadcom’s proposed construction of “plain and ordinary meaning” does not provide a basis for understanding these phrases or their limits. In the *SiRF* litigation, Broadcom argued that the formula represents a “novel aspect” of the invention. *See* RX-0311 at 7 (Broadcom’s Opposition to Defendants’ Motion for Summary Judgment). Broadcom’s current construction is susceptible to departure from the bounds of the claims and Broadcom’s prior explanation of the phrases. Respondents’ construction, on the other hand, provides a framework for understanding the claim’s bounds. Finally, although Broadcom argues that the construction limits the claim to a

single embodiment, it has not cited to the portions of the specification that would be excluded under respondents' construction.

C. Whether Sigma Infringes the Asserted Claims

Broadcom asserts claims 1, 10, 11, 16, 17, and 22 against Sigma's SX-6 SoC, which the parties agree is representative of Sigma's []. Broadcom Br. at 47. Broadcom argues infringement under its constructions and respondents' constructions.²² See Broadcom Br. at 27-62. The parties' claim-construction-dependent disputes, however, distill to limitations 1[E] and 1[F].

1. Claim 1

Claim 1 of the '104 Patent, which Broadcom divides into six limitations, follows:

1. [A] One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:

[B] at least one interface operable to receive one or both of video and audio; and

[C] at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:

[D] blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,

[E] process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

²² The doctrine of equivalents is not asserted in this investigation as to any patent. See Joint Outline; Broadcom Br.; Resps. Br. at 54, 132, 138, 236.

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[F] blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

JX-0003 at 60:45-63; *see* Broadcom Br. at 30-31. Each limitation is discussed below.

a) Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:

Broadcom argues:

The preamble of claim 1 recites “One or more circuits for processing graphics and video images to produce a blended image.” There is no dispute that the SX-6, a “System on a Chip” (SoC) for digital television (DTV) products, includes one or more circuits for processing graphics and video images to produce a blended image. CX-0004C (Havlicek WS) at Q/A 136-138; CX-0512C (Bellers Dep. Tr.) at 28:5-15, 29:4-8. Mr. Snell also agreed that the SX-6 meets the limitations of the preamble. Tr. (Snell) at 524:3-14.

In particular, the SX-6 includes a[

J. CX-0004C (Havlicek WS) at Q/A 137 (citing CX-0512C (Bellers Dep. Tr.) at 28:5-15, 29:4-8). Thus, the SX-6 SoC satisfies the preamble of claim 1 of the ‘104 Patent.

Broadcom Br. at 31.

Sigma does not clearly rebut this argument, and its expert, Mr. Snell, agreed that the SX-6 satisfied the preamble. *See generally* Resps. Br., Section VI(C)(2)(a) (the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (the limitation is not contested); *see* Snell Tr. 524.

The evidence shows that Sigma’s SX-6 SoC includes one or more circuits for processing graphics and video images to produce a blended image. *See* Snell Tr. 524; *see also* CX-0004C

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(Havlicek WS) at Q/A 137. Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies the preamble under either party's constructions.

b) Limitation [B]: at least one interface operable to receive one or both of video and audio; and

Broadcom argues:

Element [B] of claim 1 requires "at least one interface operable to receive one or both of video and audio." Sigma admits, and the evidence shows, that the SX-6 practices this claim element. Mr. Snell agreed that the SX-6 meets the limitation of element [B]. Tr. (Snell) at 526:5-14. Specifically, [

] It is undisputed that the SX-6 satisfies this limitation of claim 1.

Broadcom Br. at 31-32.

Sigma does not clearly rebut this argument, and its expert, Mr. Snell, agreed that the SX-6 satisfied this limitation. *See generally* Resps. Br., Section VI(C)(2)(a) (the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (the limitation is not contested); *see* Snell Tr. 526.

The evidence shows that Sigma's SX-6 SoC includes an interface that can receive video and audio. *See* Snell Tr. 526; *see also* CX-0004C (Havlicek WS) at Q/A 139; CX-0350C (SX-6 Datasheet) at 3, 4. Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation under either party's constructions.

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- c) ***Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:***

Broadcom argues that “the SX-6 includes a [],” which is also called the Host CPU. Broadcom Br. at 32. Broadcom argues the Host CPU is “is operably coupled to at least the video input ([]) and to memory ([]).” *Id.* Broadcom further argues that the Host CPU “is operably coupled to the [].” *Id.* at 32-33. Broadcom further contends:

[

].]

Broadcom Br. at 33.

Sigma does not clearly rebut this argument, and its expert, Mr. Snell, agreed that the SX-6 satisfied this limitation. *See generally* Resps. Br., Section VI(C)(2)(a) (the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (the limitation is not contested); *see* Snell Tr. 526.

The evidence shows that Sigma’s SX-6 SoC includes at least one processor that is operably coupled to an interface and memory. *See* Snell Tr. 526; *see also* CX-0004C (Havlicek WS) at Q/A 61, 140-41 (and the evidence cited therein). Accordingly, the administrative law

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judge has determined that Sigma's SX-6 SoC satisfies this limitation under either party's constructions.

- d) Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,*

Broadcom argues that "the SX-6 includes a [] that is operable to blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image that is then stored in memory." Broadcom Br. at 34. Broadcom relies on Dr. Havlicek's testimony, Mr. Snell's testimony, the SX-6 Datasheet (CX-0350C), Sigma's interrogatory responses, and deposition testimony from Erwin Bellers, Sigma's corporate representative. *Id.* at 34-36. Broadcom argues:

Supporting evidence includes Figure SX-6-RPBD (annotated at CDX-0002C.22), which shows that the Host CPU is operably coupled to the []

[] for blending with a video image to produce a blended image for display. *Id.*

Id. at 34-35.

Sigma does not clearly rebut this argument, and its expert, Mr. Snell, agreed that the SX-6 satisfied this limitation. *See generally* Resps. Br., Section VI(C)(2)(a) (the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (the limitation is not contested); Snell Tr. 527. At the hearing, Mr. Snell testified as follows:

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Q. Let's go to claim element 4. "Blend a plurality of graphics images using a plurality of alpha values associated with the graphics image to generate a blended graphics image for storage in the at least one memory." Now, you don't dispute that that element exists in the SX6 either, do you?

A. No.

Snell Tr. 527.

The evidence shows that Sigma's SX-6 SoC blends graphics images using a plurality of alpha values associated with the graphics images. *See* Snell Tr. 527; CX-0004C (Havlicek WS) at Q/A 142-46 (citing CX-0350C (SX-6 Datasheet) at 30, 31) (the additional evidence Broadcom cites is not necessary to show infringement). Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation under either party's constructions.

e) ***Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and***

(1) Analysis of Broadcom's Argument

Broadcom argues:

... Under Broadcom's proposed construction for "blended graphics image" and the plain and ordinary meaning for "format suitable for blending with a video image," the SX-6 includes [

] to process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image. CX-0004C (Havlicek WS) at Q/A 61, 147. A POSA would understand a blended graphics image must be in the same format as a video image in order to blend the blended graphics image with the video image. *Id.* For example, the blended graphics image and the video image must have the same color space, color depth (bit depth), pixel aspect ratio, and spatial scale. *Id.*

Under Broadcom's proposed construction, Sigma does not dispute that the SX-6 includes [] that blends at least two graphics images to generate a blended graphics image and then

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processes the images so that the blended graphics image may be blended with video, meaning that the blended graphics image and video image must be in the same format. Mr. testified that the SX-6 satisfies this element [E] (element 5) under Broadcom's construction. Tr. (Snell) at 535:13-22. Thus, Sigma has no non-infringement position under Broadcom's proposed construction of the "blended graphics image."

Broadcom Br. at 37.

Sigma's expert, Mr. Snell, also testified as follows:

Q. Okay. Let's assume, then, for a minute that the blended graphics image as used in element 5 is the same as a blended graphics image as used in element 4, okay?

A. It's a hypothetical.

Q. It is a hypothetical, yes. Can we have that assumption for a minute?

A. For a minute.

Q. Okay. Based on that assumption, would the SX6 contain claim element 5?

A. Based on that assumption, I would say yes.

Snell Tr. 535.

Sigma does not clearly rebut this argument in its opening brief. *See generally* Resps. Br., Section VI(C)(2)(a) (the limitation is not contested under Broadcom's construction).²³ In reply, Sigma argued:

In the section relating to Respondents' construction, Broadcom attempts to rebut Sigma's evidence. However, Broadcom again assumes the [] is operable to complete these processing, formatting, and placing functions based solely on a marketing document. CPostHg. Br. at 48-52. Mr. Snell testified, based on his source code analysis, that all of those functions must appear in the []

²³ Sigma's pre-hearing brief does not explicitly state which constructions its non-infringement arguments utilize. *See* Resps. Pre-Hr'g Br. at 308-17.

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J. RPostHg. Br. at 232-35. Broadcom did not provide any source code or analysis thereof to support its theories and, thus, has presented no evidence about the actual operation of the SX6. *See* generally CPostHg. Br. at 36-37, 48-52; RPostHg. Br. at 232-35. Thus, Sigma's evidence through Mr. Snell should be given more weight.

Resps. Reply at 90-91. Sigma also argues that Mr. Snell did not admit infringement under Broadcom's constructions:

During the hearing, Mr. Snell was asked about a hypothetical situation in which Broadcom's claim construction position was accepted for the term "the blended graphics image." Tr. (Snell) 535:13-22. Broadcom now misconstrues Mr. Snell's testimony as relating to the *entire limitation*. CPostHg. Br. at 29. The correct context for Mr. Snell's testimony was apparent during cross-examination when he testified that the SX6 does not infringe limitation 1[E] for additional reasons other than limitation 1[F]. Tr. (Snell) 554:12-15. On redirect, Mr. Snell further explained that the SX6 does not "place the blended graphics image in a format suitable for blending with a video image" under both proposed claim constructions. Tr. (Snell) 556:13-559:9. Broadcom's argument should be rejected.

Id. at 91.²⁴

Having considered the parties arguments, the administrative law judge has determined that Broadcom has shown that Sigma's SX-6 SoC, under Broadcom's construction, meets this limitation. In particular, the [

J). *See* CX-0004C

(Havlicek WS) at Q/A 61, 147 (and the evidence cited therein); *see also* CX-0350C (Sigma SX-6 datasheet) at 40 ([

²⁴ At Snell Tr. 554-555, Mr. Snell appears to apply respondents' constructions. Likewise, the redirect testimony—Snell Tr. 556-561—does not completely clarify which constructions Mr. Snell applied in responding to Broadcom's counsel's questioning. The redirect testimony does, however, indicate that Mr. Snell presented a non-infringement opinion under respondents' constructions.

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J). Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation under Broadcom's construction.

(2) Analysis of Respondents' Argument

(a) "The Blended Graphics Image"

Broadcom argues that limitation [E] is satisfied under respondents' constructions. *See* Broadcom Br. at 48-49 (arguing that "the [] of the SX-6 is operable to blend graphics images together to generate and process 'the blended graphics images,' which includes 'all' or 'final' graphics images to be displayed."). Broadcom relies on Dr. Havlicek's testimony (CX-0004C (Havlicek WS) at Q/A 61-62), 147, 150-54, the SX-6 datasheet (CX-0350C at 29-30), and to a limited extent, Mr. Snell's testimony (RX-1406C (Snell WS) at Q/A 59). *Id.* at 48-52. Broadcom argues, in part:

The evidence shows that if the SX-6 is to display a single blended graphic, such as a volume box, and no other menus, the SX-6 is operable to blend "all" graphics images together into a blended graphics image and process those images such that the "blended graphics image" is in a format suitable for blending with video. CX-0004C (Havlicek WS) at Q/A 150. There would be no subsequent blending of other graphics images if the only blended graphics image is, for example, a volume box that is created by the []. *Id.* In this scenario, the SX-6 would blend all of the graphics images in the [] that ultimately would be blended with a given video image. No other graphics image would be subsequently blended on a separate []. *Id.* Thus, the SX-6 is capable of blending all graphics images prior to blending the graphics images with the video image.

Id. at 49.

Sigma argues that the "SX6 sequentially blends graphics with video and does not create "the blended graphics image," as properly construed, to blend with the video image. Sigma argues that it blends multiple graphics images sequentially, []:

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RDX-0021C illustrates sequential blending in the []].

Annotated SX6 Block Diagram

[] RDX-0021C (RX-0624C/CX-0162C); RX-1406C at QA28-30. Specifically, in the SX6, video []

]). *Id.*

Resps. Br. at 226-27. Mr. Snell further testifies that the SX-6 uses a []. *See* RX-1046C (Snell WS) at Q/A 32. Sigma argues that because graphics images are blended sequentially, the “[] the SX6 simply does not blend graphics together prior to blending each individual [] with the video. [RX-1046C (Snell WS) at Q/A 32-35]. Thus, [] does not create a final blended graphics image, ‘the blended graphics image’ as that term is used in the ‘104 Patent.” Resps. Br. at 228.

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Broadcom replies that Sigma “did not discuss” the [] and that:

The blended graphics image generated by [

].”

Broadcom Reply at 18. Broadcom further argues that “as Dr. Havlicek explained, the SX6 may provide control signals to selectively enable and disable [] in order to conserve power when on screen graphics are not needed, which is most of the time in a typical consumer television.” *Id.* at 19 (citing CX-0004C (Havlicek WS) at Q/A 64). In Q/A 64, Dr. Havlicek testified:

Q64. In general, what do you and Mr. Snell agree on concerning how the SX6 functions?

A. I agree with Mr. Snell that as stated in paragraphs 106 111 of his report the SX6 [] is capable of blending graphics images with video Mr. Snell further states that the SX6 may sequentially blend graphics layers with video. I do not agree with Mr. Snell that the SX6 OSD always sequentially blends all OSD layers with video. *In my opinion*, the SX6 provides [

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]

CX-0004C (Havlicek WS) at Q/A 64 (emphasis added).

Sigma replies, in part, that Dr. Havlicek did not review the appropriate source code, that Dr. Havlicek's opinions are conclusory, and that there is no evidence that the [

]” Resps. Br. at 87-88; RX-1406C (Snell WS) at Q/A 43.

Having considered the parties' arguments, the administrative law judge has determined that Broadcom has not shown that Sigma's SX-6 SoC satisfies this limitation under respondents' construction.

The evidence that Broadcom relies upon is not sufficient to show infringement under respondents' constructions. In particular, Dr. Havlicek's testimony in Q/A 64 and Q/A 150 is unsupported because the “control signals []” are not identified. Further, Dr. Havlicek's witness statement did not address the SX-6 source code. Havlicek Tr. 383.

Indeed, the evidence shows that the SX-6 SoC does not generate “the blended graphics image” because it blends graphics sequentially, which in this instances means that some graphics images are blended with video before being blended with additional graphics. *See, e.g.*, RX-1406C (Snell WS) at Q/A 32-35, 37 (“The blended graphics image does not exist because some graphics images are blended with video before being blended with additional graphics in the Sigma []”).

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Accordingly, Sigma's SX-6 SoC does not satisfy this limitation under respondents' construction, which is also the construction of the administrative law judge. *See* § IV(B)(3)(a)(3), *supra*. Thus, it is the determination of the administrative law judge that ultimately infringement of claim 1 cannot be found.

(b) *"Place the Blended Graphics Image in a Format Suitable for Blending"*

Broadcom has argued, in part:

... the SX-6 SoC satisfies element [E] of claim 1 under Respondents' proposed construction because the blended graphics image must be processed into the same format as the video image. In other words, the blended graphics image must be adjusted based on the video image in order for it to be properly blended with the video image.

...

... The [] is operable to "adjust the blended graphic image based on the video image" by converting the format, including for example size and color space, of a graphics image and/or a blended graphics image to be in the format of the video image as it enters []. [CX-0004C (Havlicek WS) at Q/A 153]. Whatever format the video image is in as it enters the [] is the format that the blended graphics image must be in order to blend with the video image. *Id.* Accordingly, the blended graphics image will always be adjusted based on the format of the video image as the video image enters the []. *Id.*

Broadcom Br. at 51-52.

Sigma also argues, in part, that it does not infringe because:

The SX6 also does not process or place the blended graphics image in a format suitable for blending with a video image. RX-1406C at QA47-62. This is because: (1) "the blended graphics image" does not exist in the SX6; and (2) Broadcom has failed to provide evidence that the blended graphics image (under either parties' construction) is placed in a format suitable for blending with a video image. *Id.* Broadcom cites ambiguous marketing datasheets that do not prove the SX6 meets this limitation. In this instance,

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the marketing data sheet is not intended to show all of the engineering details, which are necessary for proving infringement of the '104 Patent by a preponderance of the evidence.

Resps. Br. at 232. Sigma argues that Dr. Havlicek did not establish that formatting “occurs in the [] in the SX6.” *Id.* at 233 (emphasis in original). Put in slightly different words: “the SX6 Block Diagram Dr. Havlicek relies on shows that the SX6 formats [].” *Id.* (citing RX-1406C (Snell WS) at Q/A 53-57). Sigma also argues that the “marketing datasheet Dr. Havlicek relies on to prove infringement is ambiguous as to key functions related to the '104 Patent and does not even describe the [] that blends graphics and video images together.” *Id.*

Broadcom replies:

In addition, Sigma argues that the SX6 does not place the blended graphics image in a format suitable for blending with a video image under Sigma's construction. Sigma states that the graphics images and video images to be blended are []. Respondents' Brief, p. 233. Although Sigma discusses [], Sigma ignores the fact that the graphics image may need to be converted [] if it enters the SX6 SoC in another format, []. In this example, the graphics image would need to be converted from []

[] on graphics images. CX-0004C (Havlicek WS) at Q/A 147; CX-0350C.0029 (SX6 Datasheet). The SX6 []

[] of the video image that it will be blended with. CX-0004C at Q/A 147.

Broadcom Reply at 20.

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Having considered the parties' arguments, the administrative law judge has determined that Broadcom has not shown that Sigma's SX-6 SoC places the blended graphics image in a format suitable for blending. Broadcom and Dr. Havlicek present hedged arguments that a graphics image in the SX-6 "may need to be converted to [] if it enters the SX6 SoC in another format, such as YUV." Broadcom Reply at 20. Dr. Havlicek testifies:

Q147. What is your opinion as to whether the Sigma SX6 SoC satisfies the "process" limitation of claim 1?

... In one example, *it is possible* that the SX6 2D graphic processor *may need* to perform color space conversions between YUV and RGB graphics data formats, [

]....

CX-0004C (Havlicek WS) at Q/A 147. This is an image of Section 3.8.2.2 from the datasheet:

[

]

CX-0350C at 40. This evidence is too conjectural, and therefore not sufficient, to support an infringement finding. Additionally, the evidence that Sigma cites, RX-1406C (Snell WS) at Q/A 47-62, indicates that the [], which does not satisfy the limitation. Accordingly, Sigma's SX-6 SoC does not satisfy this limitation.

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f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

(1) Analysis of Broadcom's Argument

Broadcom argues, in part:

The SX-6 is operable to only use the first [] is not necessary and does not contribute to a final display. *Id.*

...

Sigma's Mr. Bellers further explained, referring to the [

] CX-0512C (Bellers Dep. Tr.) at 28:5-19, 29:4-8.

Broadcom Br. at 38, 39-40.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(C)(2)(a) (apart from "the blended graphics image," the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (same).

The evidence shows that Sigma's SX-6 SoC, under Broadcom's construction, blends the blended graphics image with a video image using alpha values. *See* CX-0004C (Havlicek WS) at Q/A 155-57; CX-0512C (Bellers Dep. Tr.) at 28-29. In particular, the SX-6's [] *Id.* Mr. Bellers testified that the SX-6 SoC uses alpha values in blending. CX-0512C (Bellers Dep. Tr.) at 28-29. Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation under Broadcom's construction.

(2) Analysis of Respondents' Argument

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Broadcom argues that even under respondents' construction the SX-6 SoC infringes when only one graphics image is blended onto what is shown on a screen:

The [] of the SX-6 blends graphics images is *operable to* create a "final" blended graphics image, [

]. CX-0004C (Havlicek WS) at Q/A 150, 157. Again, when only one menu or other graphics image such as a volume box is being displayed on the screen, the only one menu will be created in the [

] of the SX-6 as the "final graphics blend of any graphics to be blended," per Respondents' proposed construction. Sigma agrees. "Sigma does not dispute that there is a [

] (Sigma's First Amended Objections and Responses to Complainant Broadcom Corporation's Second Set of Interrogatories (Nos.6-65), Ex. D at 5).

...

... If there are no graphics images present on [

]. Thus, the SX-6 is operable to blend the final blended graphics image from the 2D graphic processor with the video to create a final display image.

Broadcom Br. at 53-54. Broadcom further argues that the SX-6 SoC blends using alpha values:

... More specifically, the evidence shows that the [] supports "[

]. *Id.*

Id. at 57.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(C)(2)(a) (apart from “the blended graphics image,” which is discussed above, the limitation is not contested); Resps. Reply, Section IV(B)(2)(a) (same).

Accordingly, provided limitation [E] is met, the administrative law judge finds that the SX-6 SoC satisfies limitation [F] because the [] of the SX-6 SoC can blend graphics images to create a “final” blended graphics image, and the blended graphics image can then be read from memory and routed through [].

2. Claim 10

Dependent claim 10 follows:

10. The one or more circuits according to claim 1 wherein the at least one processor is operable to convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format.

JX-0003 at 61:29-33.

Broadcom argues, in part:

... The SX-6 SoC is operable to convert the graphics data format of at least one graphics image prior to blending the graphics images together in the []. By subsequently performing further color space conversions on the other graphics images as needed, the plurality of graphics images have a common graphics data format. CX-0004C (Havlicek WS) at Q/A 162-63 (citing CX-0350C (SX-6 Datasheet) at 29; CX-0513C

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(Ignaszewski Dep. Tr.) at 72:24 – 73:23). Mr. Snell agrees and states that the “[

] RX-1406C (Snell WS) at Q/A 60.

Broadcom Br. at 40-41.

Respondents argue:

Claim 10 is dependent from claim 1. JX-0003. Therefore, the Sigma Accused SoCs do not infringe claim 10 for the same reasons that the Sigma Accused SoCs do not infringe claim 1. RX-1406C at QA63-66. Broadcom has also not proven that the Sigma Accused SoCs “convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format.” *Id.* A computer program (software) would be needed to direct the operation of this [

] function. *Id.*

Resps. Br at 235.

Having considered the parties’ arguments, and assuming claim 1 is infringed, the administrative law judge has determined that the SX-6 SoC converts graphics data from one of the graphics images prior to blending, so that the images to be blended have a common format, as claim 10 requires. In particular, the [

] CX-0004C (Havlicek WS) at Q/A 163; CX-0350C (SX-6 Datasheet) at 39.

Accordingly, the SX-6 would infringe claim 10, if claim 1 were infringed.

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3. Claim 11

Claim 11 of the '104 Patent, which Broadcom divides into five limitations, follows:

11. [A] At least one circuit for generating a display image using a plurality of graphics images and a video image, the at least one circuit operational to, at least:

[B] blend the plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image, [C] wherein the graphics images and/or the blended graphics image is processed to place the blended graphics image in a format suitable for blending with the video image;

[D] store the blended graphics image in a memory; and

[E] blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values to generate the display image.

JX-0003 at 61:34-46; *see* Broadcom Br. at 42.

In general, Broadcom argues that the SX-6 SoC “also infringes independent claim 11 for the same reasons as discussed above with respect to independent claim 1.” Broadcom Br. at 42.

Broadcom then address each limitation separately. *Id.* at 42-44.

Sigma’s entire argument for claim 11 is:

Claim 11 has many of the same limitations as claim 1. Claim 11 requires:

at least one circuit operational to: ... [1] [process] the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with the video image; ... and [2] blend the blended graphics image with the video image.

JX-0003. These are the same two limitations that the SX6 did not infringe with respect to claim 1. RX-1406C at QA67-68. Therefore, the SX6 does not infringe claim 11 for the same reasons as claim 1. *Id.*

Resps. Br. at 235.

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The administrative law judge previously determined that respondents infringe claim 1 under Broadcom's constructions but not respondents' constructions (which were adopted in part herein). Based upon the reasoning presented with respect to claim 1, and the evidence and argument Broadcom presented in its brief with respect to claim 11, the administrative law judge has determined that the SX-6 SoC would also infringe claim 11 under Broadcom's constructions, but does not respondents' constructions.

4. Claim 16

Dependent Claim 16 follows:

16. The at least one circuit of claim 11, wherein the at least one circuit is further operational to format convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format.

JX-0003 at 62:7-11.

Broadcom argues:

Dependent claim 16 is similar to claim 10. The SX-6 SoC includes a [] in a manner to convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format. CX-0004C (Havlicek WS) at Q/A 173-74; *see also id.* at Q/A 162-63 (citing CX-0350C (SX-6 Datasheet) at 29; CX-0513C (Ignaszewski Dep. Tr.) at 72:24 – 73:23). For the same reasons as discussed above with respect to claim 10, the SX-6 SoC infringes claim 16 of the '104 Patent.

Broadcom Br. at 44.

Respondents' entire argument is:

Claim 16 is dependent from claim 11. JX-0003. Therefore, the SX6 does not infringe claim 16 for the same reasons as claims 1 and 11. RX-1406C at QA69-72. Broadcom has also not proven

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that the SX6 meets the “format convert graphics data format” limitation for the same reasons as claim 10. *Id.*

Resps. Br. at 236.

The administrative law judge previously determined that respondents would infringe claim 10 if all of Broadcom’s proposed claim construction were adopted (which is not the case). Based upon the reasoning presented with respect to claim 10, and the evidence and argument Broadcom presented in its brief with respect to claim 16, the administrative law judge has determined that the SX-6 SoC would also infringe claim 16.

5. Claim 17

Claim 17 of the ‘104 Patent, which Broadcom divides into five limitations, follows:

17. [A] A computer-readable storage, having stored thereon a computer program having a plurality of code sections for generating a display image using a plurality of graphics images and a video image, the code sections executable by a processor for causing the processor to perform the operations comprising:

- [B] blending the plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image,
- [C] wherein the graphics images and/or the blended graphics image is processed to place the blended graphics image in a format suitable for blending with the video image;
- [D] storing the blended graphics image in a memory; and
- [E] blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values to generate the display image.

JX-0003 at 62:12-27; *see* Broadcom Br. at 44-45.

In general, Broadcom relies on the argument and evidence it presented for claim 1 in arguing that respondents infringe claim 17. *See* Broadcom Br. at 44-46.

Respondents’ entire argument for claim 17 is:

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Claim 17 has many of the same limitations as claim 1. In particular, claim 17 requires:

Code sections executable by a processor for causing the processor to perform the operations comprising: ... [1] process[ing the graphics images and/or the blended graphics image] to place the blended graphics image in a format suitable for blending with the video image; and [2] blending the blended graphics image with the video image.

JX-0003. These are the same two limitations that the SX6 did not infringe with respect to claims 1 and 11. RX-1406C at QA73-74. The SX6 does not infringe claim 17 for the same reasons. *Id.*

Resps. Br. at 236.

The administrative law judge previously determined that respondents infringe claims 1 and 11 under Broadcom's constructions. Based upon the reasoning presented with respect to claims 1 and 11, and the evidence and argument Broadcom presented in its brief with respect to claim 11, the administrative law judge has determined that the SX-6 SoC would also infringe claim 11 under Broadcom's constructions. The SX-6 SoC would not, however, infringe under respondents' constructions, and does not infringe under the constructions adopted by the administrative law judge.

6. Claim 22

Broadcom's entire argument is:

Dependent claim 22 is similar to claim 10. The evidence shows that this limitation is met for the same reasons provided above with respect to claim 10. CX-0004C (Havlicek WS) at Q/A 185-86; *see also id.* at Q/A 162-63 (citing CX-0350C (SX-6 Datasheet) at 29; CX-0513C (Ignaszewski Dep. Tr.) at 72:24 – 73:23). For the same reasons as discussed above with respect to claim 10, the SX-6 SoC infringes claim 22 of the '104 Patent.

Broadcom Br. at 47.

Respondents' entire argument is:

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Claim 22 is dependent from claim 17. JX-0003. Therefore, the SX6 does not infringe claim 22 for the same reasons as claims 1, 11, and 17. RX-1406C at QA75-78. Broadcom has also not proven that the SX6 meets the “format convert graphics data format ...” limitation for the same reasons as claims 10 and 16. *Id.*

Resps. Br. at 236.

The administrative law judge previously determined that the SX-6 SoC would infringe claim 10 under Broadcom’s proposed claim constructions, but not under respondents’ proposed constructions or those adopted by the administrative law judge. Based upon the reasoning and evidence presented with respect to claim 10 and its dependent, asserted claims, the administrative law judge has determined that the SX-6 SoC would also infringe claim 22 only under Broadcom’s proposed claim constructions.

D. Whether VIZIO Infringes the Asserted Claims

Broadcom’s entire argument is:

The Accused VIZIO Products []. *See* Acc. Prods. Stmt. Specifically, the accused VIZIO products at issue in this Investigation are the VIZIO products that [] identified in Exhibit F to the Joint Statement Regarding Identification of Accused Products. The evidence shows that any consumer audiovisual product containing an accused SoC, including the [], which, as discussed above is representative of the other accused [], infringes claims 1, 10, 11, 16, 17, and 22 of the ‘104 Patent under either parties’ proposed constructions as discussed above. *See, e.g.,* CX-0004C (Havlicek WS) at Q/A 129, 187-88.

Broadcom Br. at 62.

VIZIO acknowledges that the accused VIZIO products [] and argues that its products “do not infringe the asserted ‘104 claims [].” Resps. Br. at 236-37. VIZIO faults Broadcom

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and Dr. Havlicek for not testing VIZIO's televisions or ascertaining "[

]." *Id.* at 237.

Broadcom replies that VIZIO has not cited any of its own documents and that "Sigma had all the information regarding the chips' functionality in VIZIO TVs." Broadcom Reply at 22. Broadcom also argues that VIZIO does not [], which are the focus of the infringement inquiry. *See id.*; *see also* RX-1086C (Hwang WS) at Q/A 13-16 (describing that [

].

VIZIO's reply argues, in part, that "Broadcom's brief confirms that Broadcom did not take any measures to confirm that [

] associated with VIZIO's products." Resps. Reply at 92.

Having considered the parties' arguments, the administrative law judge has determined that the accused VIZIO products either infringe, or do not infringe, [

]. VIZIO did not present (*e.g.*, cite) any expert testimony opining that its televisions do not infringe the asserted claims. Similarly, while VIZIO faults Broadcom for the thoroughness of its argument, VIZIO does not present any argument explaining how the alleged deficiencies are material. Accordingly, the administrative law judge has determined that the accused VIZIO products must receive [

].

E. Whether Broadcom Practices Claims 1-6 and 9-22

In general, Broadcom argues that "Broadcom's technical expert, Dr. Havlicek testified that he analyzed the [] SoC and determined that it practices claims 1-6 and 9-22 of

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the ‘104 Patent.” Broadcom Br. at 103 (citing CX-0004C (Havlicek WS) at Q/A 189-259), 104-114.

Respondents argue that:

[T]he [] product does not practice the claim limitations of “process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image” of claim 1 and “the graphics images and/or the blended graphics image is processed to place the blended graphics image in a format suitable for blending with the video image” of claims 11 and 17.

Resps. Br. at 238-41. Respondents’ reply contains brief, new challenges to limitations [a], [c], and [d] of claim 1, as well as claim 8. Resps. Reply at 30-31.

Claims 1-6 and 9-22 are addressed below.

1. Claim 1

- a) *Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:*

Broadcom argues:

The parties do not dispute that the [] includes one or more circuits having a video compositor for blending graphics images with video images. CX-0004C (Havlicek WS) at Q/A 195. To the extent the preamble is found to be limiting, the evidence shows that the [] SoC meets this limitation. CX-0004C (Havlicek WS) at Q/A 194-95. Dr. Havlicek testified that a functional block diagram of the [] (CDX-0002.25) from page 17 of Broadcom Hardware Data Module [], CX-0057C, shows circuits for processing graphics and video images to produce a blended image. CX-0004C (Havlicek WS) at Q/A 195. Thus, the [] SoC satisfies the preamble of claim 1 of the ‘104 Patent.

Broadcom Br. at 103.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(D) (the limitation is not contested); Resps. Reply, Section IV(C) (same).

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In any event, the evidence shows that the [] includes one or more circuits for processing graphics and video images to produce a blended image. *See* CX-0004C (Havlicek WS) at Q/A 189-195. Accordingly, the administrative law judge has determined that the [] practices the preamble under either party's constructions.

b) Limitation [B]: at least one interface operable to receive one or both of video and audio; and

Broadcom argues:

There appears to be no dispute that the [] includes an interface operable to receive video or audio. The evidence shows that the [] SoC is operable to receive one or both of video and audio. CX-0004C (Havlicek WS) at Q/A 196-97. Dr. Havlicek testified that the []

[] CX-0004C (Havlicek WS) at Q/A 196-97. Thus, the [] SoC satisfies this limitation of claim 1.

Broadcom Br. at 104.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(D) (the limitation is not contested); Resps. Reply, Section IV(C) (same).

The evidence shows that the []

[]. *See* CX-0004C (Havlicek WS) at Q/A 196-97; CX-0057C at 34. Accordingly, the administrative law judge has determined that the [] practices this limitation under either party's constructions.

c) Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:

Broadcom argues:

The evidence shows that the [] satisfies this limitation, as well. CX-0004C at Q/A 198-99. Dr. Havlicek

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testified that as shown in Figure 1-1 of CX-0057C (Broadcom Hardware Data Module [], CDX-0002.25, []

].
CX-0004C at Q/A 199. Thus, the [] SoC satisfies this limitation of claim 1.

Broadcom Br. at 104.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(D) (the limitation is not contested); Resps. Reply, Section IV(C) (same).

The evidence shows that the []
]. *See* CX-0004C (Havlicek WS) at Q/A 198-99; CX-0057C at 16, 17, 44, and 94. Accordingly, the administrative law judge has determined that the [] practices this limitation under either party's constructions.

d) Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,

Broadcom argues:

The evidence shows that this limitation is satisfied. CX-0004C (Havlicek WS) at Q/A 200-01. Dr. Havlicek testified that the []

].
Id. Thus, the [] SoC satisfies this limitation of claim 1.

Broadcom Br. at 104.

Sigma does not clearly rebut this argument. *See generally* Resps. Br., Section VI(D) (the limitation is not contested); Resps. Reply, Section IV(C) (same).

The evidence shows that the []
] blends graphics images using a plurality of alpha values associated with the graphics images.

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See CX-0004C (Havlicek WS) at Q/A 200-01; CX-00057 at 63; CX-0052C at 259. Accordingly, the administrative law judge has determined that the [] practices this limitation under either party's constructions.

e) Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

(1) Analysis of Broadcom's Argument

Broadcom argues:

Under Broadcom's proposed construction for "blended graphics image" and the plain and ordinary meaning for "format suitable for blending with a video image" Dr. Havlicek testified that in the []

[] (CX-0052C). *Id.* Thus, also the [] SoC satisfies this limitation of claim 1 of the '104 Patent under Broadcom's proposed construction of "blended graphics image."

Under Broadcom's proposed construction, Respondents do not dispute that the [] that blends at least two graphics images to generate a blended graphics image and then processes the images so that the blended graphics image may be blended with video, meaning that the blended graphics image and video image must be in the same format.

Broadcom Br. at 105.

Respondents argue that Dr. Havlicek has not shown how the [] blends graphics images based on a prior explanation that "'the blended graphics image must be in the same format as the video image' in order to blend" and that Dr. Havlicek has not "explain[ed] how the [] product's capability to perform color conversion shows that it also processes a graphics image" to place the image in a format suitable for blending. Resps. Br. at 238-39.

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Having considered the parties arguments, the administrative law judge has determined that Broadcom has shown that the [], under Broadcom's construction, meets this limitation. *See* CX-0004C (Havlicek WS) at Q/A 202. In particular, the []

[]. *Id.* at 202-04; CX-0057 at 56, 63, 88-103; CX-0052 at 259. Accordingly, the administrative law judge has determined that the [] practices this limitation under Broadcom's constructions.

(2) Analysis of Respondents' Arguments

(a) "The Blended Graphics Image"

Broadcom argues that the [] practices limitation [E] under respondents' constructions. *See* Broadcom Br. at 106 (arguing that the evidence "shows that the [] SoC satisfies this limitation of the Asserted Claims under Respondents' proposed constructions for this phrase."). Broadcom relies on Dr. Havlicek's testimony (CX-0004C (Havlicek WS) at Q/A 204). *Id.* Broadcom argues:

Dr. Havlicek testified that the [] is operable to "convert" or "adjust" the blended graphics image "to make the format of the blended graphics image compatible for blending." *Id.* at Q/A 204. Thus, the [] is operable to "adjust the blended graphic image based on the video image" by converting the format, including for example size and color space, of a graphics image and/or a blended graphics image to be in the format of the video image as it enters the video compositor. Dr. Havlicek explained that whatever format the video image is as it enters the video compositor is the format that the blended graphics image must be in order to blend with the video image. *Id.* at Q/A 204. The blended graphics image will always be adjusted based on the format of the video image as the video image enters the OSD blender. *Id.* at Q/A 204.

Id. at 106.

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Respondents argue, in part, that “the [] does not practice claim 1 because, according to Dr. Havlicek’s reasoning, the graphics image that is blended with video in the [] is not a “blended graphics image.” See Resps. Br. at 239. Respondents also argue:

Moreover, Broadcom has failed to establish that the [] product practices the claims under Respondents’ construction for the terms “a blended graphics image,” “the blended graphics image,” “blended graphics image,” “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” and “blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” RX-1080C.0022-24 at Q72-77. In his testimony, Dr. Havlicek cites to four figures in the [] documentation that allegedly show that “the main video compositors are operable to blend a blended graphics image with video,” stating that “[t]his allows the graphics system to be separated from the video.” CX-0004C.0076 at Q206. However, none of the figures Dr. Havlicek cites prove that [] blends the final blended graphics image with video. RX-1080C.0020 at Q73.

Id. at 239-40.

Having considered the parties’ arguments, the administrative law judge has determined that Broadcom has not shown that the [] practices this limitation under respondents’ construction of the term “the blended graphics image,” which was adopted herein. In Q/A 204, Dr. Havlicek testifies that:

Q204. How, if at all, does your opinion depend on the claim constructions that are adopted by the Judge?

A. Not at all. . . .

. . .

[T]he [] satisfies Respondents’ proposed construction for “the blended graphics image.” The 2D graphics engine in the [] is operable to blend graphics images together in arbitrary combinations including the ones indicated by the proposed constructions. For example, it is operable to blend together all of the graphics images that will receive a common

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processing prior to being blended with a video image, it is operable to blend together all of the graphics images that will ultimately be blended with a given video image, and it is operable to blend together all or some of the graphics images that will be blended onto a certain line or patch or region of a video image.

CX-0004C (Havlicek WS) at Q/A 204. Dr. Havlicek's opinion that "the [] is operable to blend graphics images together in arbitrary combinations" does not sufficiently establish how the [] works, or that the [] prepares "data representing a single view of a mixture of all graphics images to be blended," as respondents' construction requires. The evidence does not show that the [] blends "the blended graphics image," as required by the claim. See RX-1080C (Reader RWS) at Q/A 72-73 ("None of the identified evidence . . . shows the [] as blending the final blended graphics image with video."). Accordingly, it has not been shown that the [] practices this limitation under respondents' construction, as adopted by the administrative law judge. See § IV(B)(3)(a)(3), *supra*.

(b) *"Place the Blended Graphics Image in a Format Suitable for Blending"*

Broadcom has argued:

. . . Dr. Havlicek testified that the [] is operable to "convert" or "adjust" the blended graphics image "to make the format of the blended graphics image compatible for blending." *Id.* at Q/A 204. Thus, the [] is operable to "adjust the blended graphic image based on the video image" by converting the format, including for example size and color space, of a graphics image and/or a blended graphics image to be in the format of the video image as it enters the video compositor. Dr. Havlicek explained that whatever format the video image is as it enters the video compositor is the format that the blended graphics image must be in order to blend with the video image. *Id.* at Q/A 204. The blended graphics image will always be adjusted based on the format of the video image as the video image enters the OSD blender. *Id.* at Q/A 204.

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Broadcom Br. at 106.

Respondents argue that Broadcom cannot show the [] practices the “processing” limitation because Dr. Havlicek has not fully explained how the [] works. Resps. Br. at 238-39 (*e.g.*, “Dr. Havlicek fails to explain how the [] product’s capability to perform color conversion shows that it also processes a graphics image such that it has the same pixel aspect ratio and spatial scale as the video image and simply relies on the output of the [] being ‘suitable for blending.’”).

Having considered the parties’ arguments, the administrative law judge has determined that Broadcom has shown that the [] practices this disputed aspect of limitation [E]. In particular, Dr. Havlicek testified that the []

[] that format a blended graphics image in accordance with a video image. *See* CX-0004C (Havlicek WS) at Q/A 204 (“Whatever format the video image is as it enters the video compositor is the format that the blended graphics image must be in order to blend with the video image. The blended graphics image will always be adjusted based on the format of the video image as the video image enters the OSD blender.”). Finally, while respondents fault Dr. Havlicek for providing allegedly incomplete examples of how the [] practices this limitation, respondents’ expert does not offer an alternative explanation of how the [] processes graphics images. Accordingly, the administrative law judge has determined that the [] practices the “plac[ing] the blended graphics image in a format suitable for blending with a video image” aspect of limitation [E] under respondents’ interpretation of this limitation.

- f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.*

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(1) Analysis of Broadcom's Argument

Broadcom argues, in part:

Dr. Havlicek also testified that he agrees that the claim phrase “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” should be given its plain and ordinary meaning as understood by a POSA. CX-0004C (Havlicek WS) at Q/A 159, 206. The [] SoC satisfies this limitation under Broadcom's proposed construction for the reasons provided. *Id.* at Q/A 205-206.

Broadcom Br. at 107.

Respondents do not clearly rebut this argument (*i.e.*, Broadcom's argument under its own construction). *See generally* Resps. Br., Section VI(D); Resps. Reply, Section IV(C) (same).

Having considered the parties arguments, the administrative law judge has determined that Broadcom has shown that the [], under Broadcom's construction, meets this limitation. *See* CX-0004C (Havlicek WS) at Q/A 205-06; CX-0052C at 108, 117-18; CX-0057C at 63. In particular, the [], which blend blended graphics images with video. *Id.* Accordingly, the administrative law judge has determined that the [] practices this limitation under Broadcom's constructions.

(2) Analysis of Respondents' Argument

Broadcom argues:

The evidence shows that the [] satisfies Respondents' proposed construction for the term “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” which is “blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” Dr. Havlicek explained why the [] generally performs blending of graphics images with graphics images using the []. *Id.* at Q/A 206. Further, Table 1-4 at page 68 of the Broadcom Hardware Data Module []

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] shows the selection of alpha values that are supported in the []. *Id.*

Specifically, Dr. Havlicek testified that the alpha values associated with both the source and destination graphics images may be selected for use in the blending operation. *Id.* Moreover, the note that appears immediately below the table explains that there is an “invert” bit that supports blending with “one-minus” the alpha values shown in Table 1-4. *Id.* Therefore, sequentially blending graphics images with the invert bit selected results in an overall alpha value “derived from the product of one minus the alpha value for every graphics image.” *Id.* This value would then be used to blend the blended graphics image with the video image in the [] main compositor as required by Respondents’ proposed construction. *Id.*

Broadcom Br. at 107-08.

Respondents argue that:

Broadcom has failed to establish that the [] product practices the claims under Respondents’ construction for the terms “a blended graphics image,” “the blended graphics image,” “blended graphics image,” “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” and “blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” RX-1080C.0022-24 at Q72-77. In his testimony, Dr. Havlicek cites to four figures in the [] documentation that allegedly show that “the main video compositors are operable to blend a blended graphics image with video,” stating that “[t]his allows the graphics system to be separated from the video.” CX-0004C.0076 at Q206. However, none of the figures Dr. Havlicek cites prove that [] blends the final blended graphics image with video. RX-1080C.0020 at Q73.

...

Finally, Broadcom has failed to show that [] blends the blended graphics image with the video image using an alpha value derived from the product of one minus alpha value for every graphics image. RX-1080C.0021-22. Dr. Havlicek focuses his analysis on the “one minus alpha” portion of the alpha blending equation without addressing the remaining requirements of Respondents’ claim construction. Specifically, Dr. Havlicek cites

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to Table 1-4 in the [] documentation (CX-0057C), stating that a note to the table identifies the existence of an “‘invert bit’ that supports blending with ‘one-minus’ the alpha values” and that, therefore, “sequentially blending graphics image with the invert bit selected results in an overall alpha value ‘derived from the product of one minus the alpha value for every graphics image.’” CX-0004C.0074; CX-0057C.0068. However, nothing in this analysis shows how the blending would make use of an alpha value that is derived from the product of one minus the alpha value for every graphics image. RX-1080C.0021. The existence of the invert bit alone does not explain how any alpha values are derived..

Resps. Br. at 239-41.

Having considered the parties arguments, the administrative law judge has determined that Broadcom has not shown that the [] practices this limitation under respondents’ construction. *See* RX-1080C (Reader RWS) at Q/A 79. Although Dr. Havlicek points to “Table 1-4 at page 68 of the Broadcom Hardware Data Module []” as showing alpha values that are supported in the [] (e.g., CX-0004C (Havlicek WS) at Q/A 206), it is not clear how the table satisfies the formula in respondents’ construction or that adopted by the administrative law judge. *See* RX-1080C (Reader RWS) at Q/A 79 (“absent from Dr. Havlicek’s analysis is how the blending would make use of an alpha value that is “derived from the product of one minus the alpha value for every graphics image.”). Accordingly, the administrative law judge has determined that the [] does not practice this limitation.

2. Claims 2-6 and 9-22

Respondents have not presented any argument for the dependent claims. *See generally* Resps. Br. at 238-41; Resps. Reply at 93.

The administrative law judge previously determined that the [] practices claim 1 under Broadcom’s constructions, but not respondents’ constructions or those adopted herein. Based upon the reasoning presented with respect to claim 1, and the evidence and

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argument Broadcom presented in its brief with respect to the claims 2-6 and 9-22, the administrative law judge has determined that the [] also practices the additional limitations of the claims 2-6 and 9-22, and would therefore practice those claims under Broadcom's constructions (especially of claim 1), but not respondents' constructions or those adopted herein.

F. Anticipation – Eagle

In general, respondents argue that the “Eagle Graphics/Audio Media Compositor” (RX-0087) (“Eagle”) “discloses, alone or in combination, discloses claims 1-6 and 9-22 of the ‘104 Patent under all proposed constructions.” Resps. Br. at 241, 244.

Respondents also argue that Eagle was published on February 27, 1997 and “is prior art under 35 U.S.C. §§ 102(a) and 102(b).” *Id.* at 241. Respondents note that Eagle is “listed on the face of the ‘104 Patent.” *Id.* Broadcom does not contest that Eagle is prior art to the ‘104 Patent. *See* Joint Outline at 3; Broadcom Br. at 114-15. It is found that Eagle is prior art to the ‘104 patent.

1. Claim 1

- a) *Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:*

Respondents' entire argument is:

Eagle discloses “One or more circuits for processing graphics and video images to produce a blended image.” RX-0382C.000039 at Q152; RDX.0093.00001-5. Eagle discloses a “highly integrated device designed specifically for audio-video ‘set-top box’ (STB) type applications” with advanced graphics and audio capabilities. RX-0382C.000039 at Q152; RX-0087.0001; RDX-0093C.00002[;] Tr. (Medoff) at 699:5-700:18. Eagle states that the integrated device provides “graphics display and manipulation” and “compositing of graphics with video.” RX-0382C.000039 at Q152; RX-0087.0001; RDX-0093C.00003. As Dr. Medoff

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explained, Figure 4 provides a “very clear diagram of Eagle’s implementation of a two-step blending process.” Tr. (Medoff) at 704:4-11. Specifically, Figure 4 illustrates the functional components of the integrated device. RX-0382C.000039 at Q152; RX-0087.00007; RDX-0093C.00004. Eagle provides an “overlay” capability enabling graphics to be overlaid on external video (*i.e.*, a blended image of graphics and video images), through alpha blending and/or chroma keying. RX-0382C.000039 at Q152; RX-0087.00009; RDX-0093C.00004-5. Eagle thus discloses one or more circuits for processing graphics and video images to produce a blended image.

Resps. Br. at 246.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 119 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Eagle discloses a circuit as described in the preamble. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 152 (and the evidence cited in the answer, except for RDX-0093); RX-0087 (Eagle) at 7. Accordingly, the administrative law judge has determined that Eagle discloses subject matter that satisfies the preamble.

b) Limitation [B]: at least one interface operable to receive one or both of video and audio; and

Respondents’ entire argument is:

Eagle discloses “at least one interface operable to receive one or both of video and audio.” RX-0382C.000039 at Q153; RDX.0093.00005-14. The chip of Eagle was designed to process “both digital and analog audio and video.” RX-0382C.000039 at Q153; RX-0087.00003; RDX-0093C.00006. Eagle discloses several configurations for processing audio and video, including MPEG audio and video. RX-0382C.000039 at Q153; RX-0087.00002-4; RDX-0093C.00006-8. Eagle also discloses the ability to process analog audio and video. RX-0382C.000039 at Q153; RX-0087.00002-4; RDX-0093C.00008-9. The ability to receive one or both of video and audio is illustrated in Figures 1 and 2. RX-0382C.000039 at Q153; RX-0087.00004; RDX-0093C.00008-9. The chip includes “glue-less interfaces to all

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components, including ... audio and video inputs/outputs.” RX-0382C.000039 at Q153; RX-0087.00001; RDX-0093C.00007. Eagle also shows the “PCM Audio In” interface (another example of an audio input for CPU-generated audio), and a “Host Interface” for providing an interface between the integrated device and an external processor for providing, among other signals, graphics, video, or audio signals for processing. RX-0382C.000039 at Q153; RX-0087.00007, RX-0087.00024; RDX-0093C.00009-11. Furthermore, Figure 10 of Eagle shows the signal input/output (“I/O”) pins of the integrated device, showing inputs for “VIDEO IN #1,” “VIDEO OUT,” “AUDIO IN,” and “AUDIO OUT.” RX-0382C.000039 at Q153; RX-0087.00028; RDX-0093C.00012-13. Therefore, Eagle discloses at least one interface operable to receive one or both of video and audio.”

Resps. Br. at 246-47.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 119 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Eagle discloses a circuit including the interface described in limitation [B]. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 153 (and the evidence cited in the answer, except for RDX-0093); RX-0087 (Eagle) at 3, 16, 24. Accordingly, the administrative law judge has determined that Eagle discloses subject matter that satisfies this limitation.

- c) ***Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:***

Respondents’ entire argument is:

Eagle discloses “at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits.” RX-0382C.000039-40 at Q154; RDX-0093C.0014-20. Eagle discloses a central processing unit (“CPU”) which interfaces with other functional components of the integrated device through the Host Interface. RX-0382C.000040 at Q154; RX-0087.00005, 00007, 00023, Fig. 4; RDX-0093C.00018-20. Eagle is referred to as a “big-endian”

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device, compatible with different processors, such as the Power PC series from IBM. RX-0382C.000040 at Q154; RX-0087.00005; RDX-0093C.00016. Eagle has signal I/O for CPU-related controls, like “CPU_RW” and “CPU_AACK,” and provides an interface between the CPU, memory, the audio/video inputs, and the other components of the device through the Host Interface. RX-0382C.000040 at Q154; RX-0087.00024, 00028; RDX-0093C.00011-12, 0018. Therefore, the CPU is operably coupled to the audio and video inputs discussed with respect to limitation 1[a] (*i.e.*, “at least one interface”). RX-0382C.000040 at Q154; RX-0087.00028, Fig. 10; RDX-0093C.00012, 00014-18.

The CPU is operably coupled to a dynamic random access memory (“DRAM”), as illustrated at least in in Figures 1, 2, and 4. RX-0382C.000039-40 at Q154; RX-0087.00004, 0007; RDX-0093C.00014, 00016, 00018; *see also* RX-0087.00005 (discussing the DRAM of the integrated device); RDX-0093C.00015. The integrated device also has “a high performance memory controller that directly controls DRAM.” RX-0382C.000040 at Q154; RX-0087.00026; RDX-0093C.00015. The DRAM is referred to as “local memory” of the integrated device. RX-0382C.000040 at Q154; RX-0087.00019-20; RDX.0093.00019-20. The CPU “can directly access multi-byte quantities in Eagle and its memory,” showing that the CPU is operably coupled to the memory. RX-0382C.000040 at Q154; RX-0087.00005; RDX-0093C.00016. Moreover, the CPU is capable of writing pixels to “local memory.” RX-0382C.000040 at Q154; RX-0087.00023; RDX-0093C.00020.

Resps. Br. at 247-48.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 119 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Eagle discloses a circuit including the processor described in limitation [C]. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 154 (and the evidence cited in the answer, except for RDX-0093); RX-0087 (Eagle) at 5, 19-20, 23. Accordingly, the administrative law judge has determined that Eagle discloses subject matter that satisfies this limitation.

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- d) *Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,*

(1) Analysis of Respondents' Argument

Respondents argue, in part:

Eagle performs alpha blending of graphics images and external video and of graphics images themselves. RX-0382C.000036 at Q144. Eagle provides a "very clear and unambiguous description of the alpha blending of two images." Tr. (Medoff) at 700:17-18; *see id.* at 699:5-700:18. Eagle discloses a blitter, which performs operations on arrays of pixels, including alpha blending. RX-0382C.000036 at Q142-44; RX-0087.00019-20; Tr. (Medoff) at 699:5-700:18; 703:23-704:11. The term "blitter" derives from "Bit BLT," an acronym for the "bit block transfer" function implemented in software and microcode. Eagle discloses that the blitter blends together graphics images using a "weighted sum based on an alpha factor." RX-0382C.000036-37 at Q143-45; RX-0087.00020; Tr. (Medoff) at 699:5-700:18; 703:23-704:11. Specifically, the weighted sum is determined by:

$$\text{result_pixel} = \text{source1_pixel} * \text{blit_alpha} + \text{source2_pixel} * (1 - \text{blit_alpha})$$

Eagle also discloses blending graphics images through a method called "alpha blending on write from CPU." RX-0382C.000037 at Q146-47; RX-0087.00022. Through this method, the CPU can write RGB pixel values to any local memory location with independent alpha values for each pixel. RX-0382C.000037 at Q146-47; RX-0087.00023. The method performs alpha blending using a nearly identical equation as used by the blitter to blend graphics images from different memory locations:

$$\text{result_pixel} = \text{CPU_pixel} * \text{CPU_alpha} + \text{destination_pixel} * (1 - \text{CPU_alpha})$$

Eagle also discloses blending graphics images with external video through its "overlay" capability. RX-0382C.000038 at Q148-49; RX-0087.00009-10. Like the blending performed between

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graphics images, Eagle blends graphics images with external video using a nearly identical equation:

$$\text{output_value} = \text{alpha} * \text{graphics_value} + (1 - \text{alpha}) * \text{ext_video_value}.$$

Resps. Br. at 245-46.

Broadcom argues:

Eagle fails to teach blending “a plurality of graphics images” and fails to disclose blending “of graphics images using a *plurality* of alpha values associated with the graphics *images*” as required by claim 1 of the ‘104 Patent. *Id.* at Q/A 101. Eagle discloses three processes that may be used for alpha blending. *Id.* The equation disclosed on page 10, for example, is for blending a graphics image with an external video image. It does not disclose or relate to blending a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in memory as required by claim 1 of the ‘104 Patent. *Id.* At page 22, Eagle reveals the blitter alpha blending equation. Dr. Medoff then assumes that the source1_pixel and source2_pixel could be pixels from two graphics images, and if true, this equation implies that the Eagle blitter can be used to blend two graphics images by the traditional “one step” method. See CX-578C (Havlicek WS) at Q/A 102.

...

... [the equation on page 22 of Eagle] shows only one alpha value blit_alpha; it is a single 8-bit value that must be used for the entire blit operation, *i.e.*, the same value blit_alpha must be used for all pixels. *Id.* Thus, the blitter in Eagle is not capable of blending a plurality of graphics together using a *plurality* of alpha values associated with the graphics images.

Finally, the third and final alpha blending operation page 23 merely discloses traditional one-step blending process, and does not disclose blending the graphics images using a plurality of alpha values associated with the graphics images as required by claim 1 of the ‘104 Patent.

Broadcom Br. at 120 (emphasis in original).

Respondents reply, in part:

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Broadcom's assertion that Eagle does not disclose blending graphics (*see* CPostHg. Br. 119-20) is incorrect. Eagle discloses a blitter that alpha blends a plurality of graphics images together to create a blended graphics image. RX-0382C (Medoff) Q142-44; RX-0087.00019-20; Tr. (Medoff) at 699:5-700:18; 703:23-704:11; *see* RPostHg. Br. at 244-54. As Dr. Medoff testified, Eagle provides a "very clear and unambiguous description of the alpha blending of two images." Tr. (Medoff) at 700:17-18. Eagle also discloses that alpha blending of graphics images can be performed by the Eagle CPU using an identical equation. RX-0382C.000035-37, 41; RPostHg. Br. at 244-46, 248-51.

Resps. Reply at 95.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Eagle discloses a processor that is operable to "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory." As an initial matter, the evidence that respondents cite does not establish that Eagle discloses blending a plurality (*i.e.*, two or more) graphics images. In particular, Dr. Medoff's testimony that "Eagle also includes some acceleration features that support 'an unrestricted number of sprites and layers,' which one of ordinary skill in the art would understand refers to graphics images" is unsupported; no extra references or evidence is cited to explain the meaning of the term, show that the concept was inherent, or demonstrate enablement.²⁵ Additionally, respondents have not shown that Eagle teaches alpha blending "using a plurality of alpha values associated with the graphics images." With regard to Eagle's three blending formulas:

²⁵ *See* THE MANUAL OF PATENT EXAMINING PROCEDURE, § 2131.01 (9th Ed., Rev. 08.2017, last revised January 2018) (discussing instances when it is appropriate to use multiple references in an anticipation rejection).

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- The first formula²⁶ (on page 10 of Eagle) does not clearly disclose blending two or more graphics images using a plurality of alpha values associated with the graphics images. *See* CX-0578C (Havlicek RWS) at Q/A 101.
- The second formula²⁷ (on page 22 of Eagle) does not clearly disclose blending two or more graphics images using a plurality of alpha values associated with the graphics images. *See* CX-0578C (Havlicek RWS) at Q/A 102 (“the same value blit_alpha must be used for all pixels.”).
- The third formula²⁸ (on page 23 of Eagle) does not clearly disclose blending two or more graphics images using a plurality of alpha values associated with the graphics images. *See* CX-0578C (Havlicek RWS) at Q/A 103.

See also CX-0587C (Havlicek RWS) at Q/A 98, 100-104, 107.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Eagle discloses subject matter that satisfies this limitation.

(2) Analysis of Broadcom’s Argument²⁹

As discussed above with respect to claim construction, respondents’ proposed construction of the term “a blended graphics image” is identical to Broadcom’s alternative construction, and was adopted by the administrative law judge.³⁰ Respondents argue that even if Broadcom’s primary argument were adopted, and no separate construction for the term “a

²⁶ The first formula is: $\text{output_value} = \alpha * \text{graphics_value} + (1 - \alpha) * \text{ext_video_value}$

²⁷ The second formula is: $\text{result_pixel} = \text{CPU_pixel} * \text{CPU_alpha} + \text{destination_pixel} * (1 - \text{CPU_alpha})$

²⁸ The third formula is: $\text{result_pixel} = \text{source1_pixel} * \text{blit_alpha} + \text{source2_pixel} * (1 - \text{blit_alpha})$.

²⁹ The administrative law judge provides analysis under Broadcom’s construction because respondents’ brief presents arguments under both respondents’ and complainant’s constructions.

³⁰ Broadcom has argued that a “separate construction is not necessary” for the terms “blended graphics image,” “a blended graphics image,” and “the blended graphics image.” Broadcom Br. at 22-23.

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blended graphics image” is necessary, Eagle still satisfied this claim element. Respondents’ entire argument is:

Complainant’s Construction: Dr. Medoff testified during the hearing that “[u]nder Broadcom’s construction, [his] opinion is that Eagle anticipates claim 1.” Tr. (Medoff) at 685:5-7. For similar reasons as under Respondents’ construction, the array of “result_pixel” in Eagle, alone or modified by the disclosures of Porter & Duff, also satisfies Complaint’s construction—plain and ordinary meaning—or Complainant’s alternative construction—“data representing a single view of a mixture of at least two graphics images.”

Resps. Br. at 251 (emphasis in original).

The administrative law judge previously determined that respondents have not shown, through clear and convincing evidence, that Eagle discloses subject matter that satisfies this limitation. *See* § IV(F)(1)(d)(1), *supra*. In particular, as discussed above, respondents have not shown, through clear and convincing evidence, that Eagle discloses blending a plurality (*i.e.*, two or more) graphics images or that Eagle teaches alpha blending “using a plurality of alpha values associated with the graphics images.” The cited portion of Dr. Medoff’s testimony from the hearing does not change the administrative law judge’s conclusion from § IV(F)(1)(d)(1), *supra*.³¹

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Eagle discloses subject matter that satisfies this limitation.

³¹ Dr. Medoff testified that “Under Broadcom’s construction, my opinion is that the Eagle reference anticipates claim 1.” Medoff Tr. 685. *See also* RX-0382C (Medoff WS) at Q/A 157 (“Overall, the different constructions did not impact my analysis of this limitation. As I will explain, Eagle (RX-0087) discloses this limitation under either proposed construction.”).

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- e) *Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and*

Respondents' entire argument is:

Eagle discloses "process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image." RX-0382C.0042 at Q159-61; RDX-0093C.0049-52.

Broadcom's expert agreed that this limitation "means [] that the format of the video and the graphics must match" when the video and graphics reach the "blending circuit." Tr. (Havlicek) 341:9-342:3. The array of "result_pixel" after all alpha blending is completed is "data representing a single view of a mixture of all graphics images to be blended." As discussed above with respect to [limitation 1[D]], the resultant pixels stored in the "destination address" may be used as a source array in a subsequent blending operation, thereby blending multiple graphics images together (as the array at the destination address is the combination of at least two graphics images). RX-0382C.0041 at Q158; RDX-0093C.23-25. Therefore, after all graphics images are alpha blended, the final array of "result_pixel" represents a single view of all the graphics images meant to be blended. Eagle converts the blended graphics image into the YCbCr domain prior to overlaying the graphics on video. See RX-0382C Q161; RX-0087.8-10. Eagle's internal color space converter converts the stored blended graphics image into the YCbCr domain so that it is suitable for blending with video because this is "the natural domain of the external video." RX-0087.00010; see RX-0382C.000042 at Q161. The Display Controller further provides for displaying output video in one of two color spaces: RGB 16 or CLUT 8, as discussed on pages 7-8 of Eagle (RX-0087). A digital encoder (DENC) or digital-to-analog converter (DAC) converts the final output from the Display Controller as illustrated in Figure 4 of Eagle (RX-0087.7). Because the result_pixel and the video are blended together, they must be in the same format when they reach the Display Controller—as Dr. Havlicek asserted the claims require. Tr. (Havlicek) 341:9-342:3. Therefore, Eagle (RX-0087) discloses "process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image."

Resps. Br. at 251-52.

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Broadcom does not clearly rebut this argument. *See generally* Broadcom Br., Section IV(B)(7)(c)(i) (the limitation is not contested); Broadcom Reply, Section II(E) (the limitation is not contested).³² Indeed, although Broadcom's expert, Dr. Havlicek, testified that this limitation was not met, Broadcom did not cite this testimony. *See, e.g.*, CX-0578C (Havlicek RWS) at Q/A 121-22.

The evidence and argument cited in respondents' brief shows that Eagle discloses a processor that is operable to process graphics images into a format suitable for blending with a video image. *See* RX-0087 (Eagle) at 10; RX-0382C (Medoff WS) at Q/A 159-61; Havlicek Tr. 341-342. In particular, Eagle discloses: "Compositing of graphics and video is implemented in the YCbCr domain, which is the natural domain of the external video. The graphics display values are converted to YCbCr by an internal color space converter." RX-0087 at 10. Accordingly, the administrative law judge has determined that Eagle discloses subject matter that satisfies this limitation.

f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

(1) Analysis of Respondents' Argument³³

With respect to the Eagle reference only, respondents argue:

To the extent that [limitation [F]] is construed as a two-step blending process in which graphics are blended together before they are blended with video, Eagle (RX-0087) discloses on pages

³² Broadcom's argument for limitation [E] is dependent on its argument for limitation [D]. *See* Broadcom Br. at 119 ("Eagle also does not disclose claim elements [E] and [F] above because it does not disclose "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.").

³³ Respondents' proposed construction is: "blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image." Resps. Br. at 252.

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9-10 two types of overlays utilizing alpha blending, based on the particular pixel mode used: (1) alpha plane mode or (2) alpha-CLUT mode. Tr. (Medoff) at 704:2-11. In either mode, “a translucent pixel is multiplied by the alpha value while the corresponding pixel in the video background is multiplied by (1-alpha) and the two are summed to produce the output value.” RX-0087.00010.

Resps. Br. at 254.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 119 (Broadcom presents an unsupported, conclusory argument that dovetails with its arguments about limitation [D]); Broadcom Reply, Section II(E) (same).³⁴ Indeed, although Broadcom’s expert, Dr. Havlicek, testified that this limitation was not met, *see, e.g.*, CX-0578C (Havlicek RWS) at Q/A 123, 127, Broadcom did not cite this testimony.

If limitation [D] is satisfied, the evidence and argument cited in respondents’ brief shows that Eagle discloses a processor that is operable to “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” *See* RX-0087 (Eagle) at 7, 9-10; RX-0382C (Medoff WS) at Q/A 171; Medoff Tr. 704. The administrative law judge, however, previously determined that Eagle did not disclose subject matter showing that limitation [D] was known. *See* § IV(F)(1)(d), *supra*.

(2) Analysis of Broadcom’s Argument

Respondents’ entire argument is:

Complainant’s Construction: For these reasons, Eagle, alone or modified by Porter & Duff, also satisfies Complaint’s construction of plain and ordinary meaning. As discussed above, Dr. Medoff

³⁴ Broadcom’s argument for limitation [F] is dependent on its argument for limitation [D]. *See* Broadcom Br. at 119 (“Eagle also does not disclose claim elements [E] and [F] above because it does not disclose ‘blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.’”).

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analyzed the claims under both Complainant's [and respondents'] construction of the term. Tr. (Medoff) at 684:25:685:7.

Resps. Br. at 254 (emphasis in original).

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br., Section IV(B)(7)(c)(i) (the limitation is not contested); Broadcom Reply, Section II(E) (Broadcom presents an unsupported, conclusory argument that dovetails with its arguments about limitation [C]). Indeed, although Broadcom's expert, Dr. Havlicek, testified that this limitation was not met, Broadcom did not cite this testimony. *See, e.g.*, CX-0578C (Havlicek RWS) at Q/A 123, 127.

The administrative law judge has determined that Eagle discloses subject matter that satisfies this limitation under Broadcom's constructions for the same reasons it satisfies this limitation under respondents' constructions. Thus, if limitation [D] is satisfied, the evidence and argument cited in respondents' brief shows that Eagle discloses a processor that is operable to "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values." *See* RX-0087 (Eagle) at 7, 9-10; RX-0382C (Medoff WS) at Q/A 171; Medoff Tr. 704. The administrative law judge, however, previously determined that Eagle did not disclose subject matter showing that limitation [D] was known. *See* § IV(F)(1)(d), *supra*.

2. Claim 10

Respondents argue:

Eagle discloses the one or more circuits of claim 1, "wherein the at least one processor is operable to convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format." RX-0382C.0047 at Q179-80; RDX-0093C.00124-36.

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Eagle discloses that the graphics images which are blended during alpha blending in the blitter must have a consistent format. RX-0382C.000047 at Q180; RDX-0093C.00126; RX-0087.00020. Specifically, although graphics images may be generated in either RGB16 or CLUT8 format, RGB16 must be used for all graphics image being alpha blended by the blitter. RX-0382C.000047 at Q180; RX-0087.00020; RDX-0093C.00126-27. That is, the graphics images must be converted into RGB format for alpha blending. RX-0382C.000047 at Q180; RDX-0093C.00126-27; RX-0087.00022 (“Alpha blending can only be performed on RGB pixels because the arithmetic operations do not have a meaningful interpretation for the index values used in CLUT color spaces.”). The same is true for blending graphics images through the alpha blend on write from CPU capability. RX-0382C.000047 at Q180; RDX-0093C.00127-30; RX-0087.00022-23. As described in Eagle, the RGB values written by the CPU “can be specified as 24-bit values,” and is converted (through dithering) to a 16-bit value (*i.e.*, RGB16 format). RX-0382C.000047 at Q180; RDX-0093C.00130; RX-0087.00023.

Resps. Br. at 254-55.

Broadcom argues that Eagle does not anticipate claim 10 based on its dependency from claim 1 and because Dr. Medoff did not provide “detailed analysis . . . show[ing] where that limitation is disclosed.” Broadcom Br. at 121 (citing CX-0578C (Havlicek RWS) at Q/A 156).

The administrative law judge has determined that Eagle anticipates claim 10, provided it also anticipates claim 1. Dr. Medoff explained that Eagle discloses placing graphics images in RGB16 format prior to blending. RX-0382C (Medoff WS) at Q/A 180. Page 20 of Eagle states:

Color Space

Either RGB16 or CLUT8 color space can be used, however, the color space must be consistent for the source and destination. Alpha blending is supported only for RGB16 pixels.

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RX-0087 at 20. While Dr. Havlicek faults Dr. Medoff for not providing any analysis, he does not substantively analyze the points Dr. Medoff has made. *See* CX-0578C (Havlicek RWS) at Q/A 156.

3. Claims 11, 16, 17 and 22

Respondents and Broadcom have not presented separate arguments for claims 11, 16, 17, and 22. *See* Resps. Br. at 255 (respondents simply refer to prior arguments); Broadcom Br. at 119 (same).

Accordingly, the administrative law judge has determined that respondents have not shown that claims 11, 16, 17, and 22 are anticipated based upon the same rationale provided with respect to claim 1.

4. Claims 2-6, 9, 12-15, 18-21

Respondents' introduction of Eagle vaguely argues, *i.e.*, without explaining whether respondents are making an anticipation or obviousness argument, that: "Eagle discloses, alone or in combination, discloses claims 1-6 and 9-22 of the '104 Patent under all proposed constructions." Resps. Br. at 244. Respondents later argue that claims 2-6, 9, 12-15, 18-21 would have been obvious:

Eagle, alone or in view of Oakley (RX-0149), renders obvious claims 2-6, 9, 12-15, and 18-21 (the "dependent claims"). RX-0382C.000049 at Q191-203; RDX-0093C.00087-124, 00214-218. Moreover, Eagle, alone or in view of West (RX-0150) renders obvious claims 2, 4-6, 9, 12, 13, 18, and 19. RX-0382C.000049 at Q191-203; RDX-0093C.00087-124, 00214-218.

Resps. Br. at 255.

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Accordingly, the administrative law judge has determined that respondents have not shown that Eagle anticipates claims 2-6, 9, 12-15, and 18-21. Respondents' obviousness arguments are addressed in § IV(L), *infra*.

G. Anticipation – Gloudemans

In general, respondents argue that U.S. Patent No. 6,266,100 ("Gloudemans") "anticipates claims 1, 11, and 17 of the '104 Patent under Broadcom's constructions." Resps. Br. at 256. Respondents argue that Gloudemans is prior art under 35 U.S.C. § 102(e) "because [it] was filed before November 9, 1998 (the earliest priority date of the '104 Patent, *see* RX-0683)." *Id.* at 241. Respondents note that Gloudemans is "listed on the face of the '104 Patent." *Id.*

Broadcom argues, in part, that:

Gloudemans does not disclose "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory," as recited in claim 1. CX-578C (Havlicek WS) at Q/A 301-302, 360-361, and 376-377. Gloudemans also does not disclose claim elements [E] and [F] above because it does not disclose "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image." *Id.*

Broadcom Br. at 135.

1. Claim 1

- a) ***Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:***

Respondents' entire argument is:

Gloudemans (RX-0073) discloses "One or more circuits for processing graphics and video images to produce a blended image." RX-0382C Q256; RX-0073 at Figs. 1 and 2, 4:28-60, 5:4-22, 7:26-65; RDX-0089.2-5. Broadcom does not dispute that Gloudemans discloses this element. CX-0578C (Havlicek) Q297-391. Gloudemans "can be used to enhance a video representation

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of the football stadium” by blending graphics with video, where “video means an analog or digital signal depicting (or used to produce) moving images.” RX-0382C Q256; RX-0073 at 4:31-32; RDX-0089.2-5. Gloudemans’ PC concentrator 82 sends camera view data to a computer 94, which works with computer 96 to create graphics and alpha signals, which in turn are sent to keyer 98 for blending with a video signal from frame delay 100. *Id.*; RX-0073 at 7:26-65. This meets limitation 1[pre].

Resps. Br. at. 258.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 135 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Gloudemans discloses a circuit as described in the preamble. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 256 (and the evidence cited in the answer, except for RDX-0089); RX-0073 (Gloudemans) at Figs. 1 and 2, 4:28-60, 5:4-22, 7:26-65. Accordingly, the administrative law judge has determined that Gloudemans discloses subject matter that satisfies the preamble.

b) Limitation [B]: at least one interface operable to receive one or both of video and audio; and

Respondents’ entire argument is:

Gloudemans discloses “at least one interface operable to receive one or both of video and audio.” RX-0382C Q257; RX-0073 at Fig.2, 6:38-58, 7:26-27, 7:40-46, 8:32-42; RDX-0089.0006-08. Broadcom does not dispute that Gloudemans discloses this element. CX-0578C (Havlicek) Q297-391. Video outputs of cameras 60, 62, and 64 are sent to multiviewer 90, which combines them into one signal. Thus, multiviewer 90 meets this limitation. RX-0382C Q257; RX-0073 at Fig.2, 6:38-58; RDX-0089.0006-08.

Resps. Br. at 258.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 135 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

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The evidence and argument cited in respondents' brief shows that Gloudemans discloses a circuit including an interface that can receive video and audio. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 257 (and the evidence cited in the answer, except for RDX-0089); RX-0073 (Gloudemans) at Fig.2, 6:38-58, 7:26-27, 7:40-46, 8:32-42. Accordingly, the administrative law judge has determined that Gloudemans discloses subject matter that satisfies this limitation.

- c) ***Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:***

Respondents' entire argument is:

Gloudemans discloses "at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits." RX-0382C Q258; RX-0073 at Fig. 2, 7:50-52, 8:32-42; RDX-0089.8-9. Broadcom does not dispute that Gloudemans discloses this element. CX-0578C (Havlicek) Q297-391. Computer 94 and tally detector 88 are "O2 workstations," and computer 96 is an "Indigo 2 Impact" computer. RX-0382C Q258; RX-0073 at 8:3-42; RDX-0089.8-9. Such computers "include processors, memory, [and] disk drives." Tally detector 88, computer 94, and computer 96 are operably coupled to the multiviewer 90. *Id.*; RX-0073 at Fig. 2. Because computers 94 and 96 and tally detector 88 are operably coupled to the multiviewer 90 (the "at least one interface") as well as to "memory" that is part of each of the computers 94 and 96 and tally detector 88, multiviewer 90 is the claimed "at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits."

Resps. Br. at 258-59.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 135 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Gloudemans discloses a processor as described in claim 1. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 258 (and the

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evidence cited in the answer, except for RDX-0089); RX-0073 (Gloudemans) at Fig. 2, 7:50-52, 8:32-42. Accordingly, the administrative law judge has determined that Gloudemans discloses subject matter that satisfies this limitation.

- d) *Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,***

Respondents argue, in part:

Gloudemans discloses this limitation under Respondents' construction of "a blended graphics image," as well as Complainant's construction of "blended graphics image" (same). RX-0382C Q259-63; RX-0424.0006; RDX-0078.0010-34. Gloudemans discusses "combining *at least a first image or video* with *at least a second image or video* such that the result includes all or part of the image or video and all or part of the second image or video." *Id.*; RX-0073 at 4:32-35. Computers 94 and 96 work together to create a graphic and a set of associated alpha signals, such as highlighting "trouble spots" on a golf course and first down lines in football games, RX-0073 at 1:51-2:2, 5:4-22; RX-0382C Q259; RDX-0089.0010-17. Gloudemans explains that "*any other graphic* can be *added to* or *deleted from* any suitable surface or portion of the stadium (including the field)," using a variety of operations including "blending two images," "editing an image, adding an image, replacing an image with another image, highlighting an image using any appropriate method of highlighting" or "other suitable graphical enhancements to the video." RX-0073 at 5:12-22; RX-0382C Q259; RDX-0089.10-17. Figure 1 shows multiple graphics composited with one another and with the video of the football field (*e.g.*, yard line 8, logo 12, and logo 14), each of which can be "added to the video at the right location." RX-0073 at 4:28-65, Fig. 1; RX-0382C Q259; RDX-0089.10-16. This blending of graphic images discloses the claimed "blend a plurality of graphics images" and "generate a blended graphics image." These images can be blended together using an "alpha signal" that indicates "how to blend one image or video with a second image or video." RX-0073 at 34:38-40, Fig. 24; RX-0382C Q259; RDX-0089.16. Gloudemans explains that computers 94 and/or 96 determine alphas for various pixels and use those determined alphas for blending a graphic using keyer 98 or a computer. RX-0073 at Fig. 24, 8:50-52, 34:16-46; RX-0382C Q259; RDX-0089.16. Thus, Gloudemans discloses this limitation.

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Resps. Br. at 259-60.

Broadcom argues:

Gloudemans (RX-0073) discloses a one-step process for blending a graphics image onto a video signal. CX-578C (Havlicek WS) at Q/A 302. In particular, Gloudemans discloses a process wherein a single graphics image is created and blended onto a video signal in a single blending step. *Id.*; RX-0073, col. 7:38-53. Gloudemans does not disclose blending a plurality of graphics images using a plurality of alpha values to generate a blended graphics image. CX-578C (Havlicek WS) at Q/A 302.

In Gloudemans, a graphic is drawn and sent to a keyer to be blended with a video signal. *Id.*; RX-0073 at col. 33:21-26. Gloudemans renders a single graphics image and then blends that single graphics image with video. CX-578C (Havlicek WS) at Q/A 302, 303. Gloudemans does not disclose blending a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image. *Id.* at Q/A 303.

As disclosed in Gloudemans, a graphic can also be a logo such as an advertisement, emblem, etc. *Id.*; RX-0073 at col. 34:10-15. The basic procedure for using a logo is the same as already discussed: parameters are received, preliminary computations are performed, and then the graphic is drawn (rendered in pixels) as a single graphics image. CX-578C (Havlicek WS) at Q/A 303. This single graphics image is then sent to the keyer (or a computer) for blending with video in a one-step blending process. *Id.*

Broadcom Br. at 135-36.

Broadcom replies, in part:

... Dr. Medoff mischaracterizes column 7, lines 54-64 of Gloudemans as disclosing a system for blending a plurality of graphics images by stating that Gloudemans “blends a ‘foreground’ image with a ‘background’ image.” *Id.* at Q/A 254. However, Gloudemans refers to a graphic as the foreground and the video signal as the background, not two graphics images. CX-578C (Havlicek WS) at Q/A 304. None of Dr. Medoff’s citations to Gloudemans disclose blending a plurality of graphics images together as required by claim 1 of the ‘104 Patent. *Id.*

Broadcom Reply at 28.

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The evidence shows that Gloudemans discloses a processor that is operable to “blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory” under respondents’ constructions. Gloudemans discloses blending a plurality of graphics images on a screen. For example, Gloudemans discusses adding a first-down line and a logo on the same screen:

A first down line can be depicted by drawing a line across the field. This line can be a black or white line, or any other suitable color (*e.g.* red). The line can be bold, thin, thick, shaded, blinking, dotted, dashed, tapered, etc. In one embodiment, the line or other graphic is displayed to show a certain significance such as having a first down line blink on third down or change color when the offense is near the goal line. The enhancement need not even be a line. The graphic may be another shape or form that is appropriate. In addition to blending two images, the enhancement can be made by editing an image, adding an image, replacing an image with another image, highlighting an image using any appropriate method of highlighting, other suitable graphical enhancements to the video, etc. Furthermore, the enhancements are not restricted to showing first down lines and logos. Any other graphic can be added to or deleted from any suitable surface or portion of the stadium (including the field). For example, a graphic could be added to show more people in the stands.

RX-0073 at FIG. 1, 4:32-35, 5:4-22; RX-0382C (Medoff WS) at Q/A 259. Although Dr. Havlicek (Broadcom’s expert) disagrees with Dr. Medoff, Dr. Havlicek’s disagreement is based on a requirement that all blended graphics must be contiguous. *See* CX-0578C (Havlicek RWS) at Q/A 306 (“it is clear from the figure that yard line 8, logo 12, and logo 14 are all disjoint graphics that are not blended with one another”).

Gloudemans also teaches blending images with a plurality of alpha values. *See* RX-0073 at 34:16-46; RX-0382C (Medoff WS) at Q/A 259. For example, Gloudemans discusses using different alpha values for boundary points, center points, and edge points. *Id.* The alpha values can be determined for each point in a graphic. RX-0073 at 34:35-46.

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The evidence does not show, however, that Gloudemans discloses storing an image “in the at least one memory.” In particular, Dr. Medoff testified that “One of ordinary skill would understand that before sending this blended graphic to keyer 98, the graphic could be stored, at least temporarily, in the memory of one of computer 94 or computer 96, in order to perform that sending.” RX-0382C (Medoff WS) at Q/A 259. This testimony is insufficient to show that Gloudemans clearly and convincingly discloses a memory.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Gloudemans discloses subject matter that satisfies this limitation.

- e) ***Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and***

Respondents’ entire argument is:

Gloudemans discloses “process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image.” RX-0382C Q264; RX-0073 at Figs. 1, 2, 3, 24, 6:21-23, 7:43-45, 9:4-27, 14:65-67, 32:25-47, 33:10-13, 34:16-46; RDX-0089.0034-40. Broadcom’s primary dispute as to this claim element is whether Gloudemans discloses blending a plurality of graphics images—limitation 1[c]. CPreHg. Br. at 171. Broadcom’s expert agreed that this limitation “means that the format of the video and the graphics must match” when the video and graphics reach the “blending circuit.” Tr. (Havlicek) 341:9-342:3. Broadcom’s expert also agreed that “Gloudemans establishes that the format suitable for blending with video is determined by the specification of the keyer.” CPreHg. Br. at 171 (citing CX-0578C at Q316). In fact, Gloudemans discloses that the graphic signal can be sent as a YUV, RGB, or YCbCr signal or other appropriate signal “according to the specification of the keyer,” which also receives a video signal. RX-0073 at 7:40-46. Broadcom’s complaint is that Gloudemans does not disclose “how a graphics image not in the suitable format for blending with video can be processed to place it in the suitable format for blending with video.” CPreHg. Br. at 171 (citing CX-0578C at Q316). But the fact, recognized by

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Broadcom, that Gloudemans discloses that the graphics image is in a format suitable for blending with video means that Gloudemans discloses that the graphics are processed to place them in this form. Gloudemans' graphics signals may be sent in a variety of different formats "according to the specification of the keyer," which is configured to receive video signal from frame delay 100 and blend it with the graphic signal. RX-0382C Q256, 264; RX-0073 at Fig. 2, 7:26-65; RDX-0089.0034-40. Because the graphics and video are blended together, and because the graphics are tailored "according to the specification of the keyer," they are in the same format when they reach the keyer for blending—as Dr. Havlicek asserts the claims require. Tr. (Havlicek) 341:9-342:3. Thus, Gloudemans discloses element 1[d]. RX-0382C Q264; RX-0073 at Fig. 2, 7:43-45, 9:4-27, 14:65-67, 32:25-47, 33:10-13, 34:16-46; RDX-0089.0034-40.

Resps. Br. at 262-63.

Broadcom argues, in part:

With respect to Element [E], Gloudemans also does not disclose processing even single (non-blended) graphics images to place them in a format suitable for blending with video. [CX-0578C (Havlicek RWS)] at Q/A 316. Gloudemans establishes that the format suitable for blending with video is determined by the specification of the keyer, it fails to teach how a graphics image not in the suitable format for blending with video can be processed to place it in the suitable format for blending with video. *Id.*

Broadcom Br. at 137-38. Broadcom then argues that Gloudemans does not disclose this limitation because it "teaches away from blending graphics with a video signal that originated outside of the invention." *Id.* at 138.

The evidence shows that Gloudemans discloses a processor that is operable to process graphics images into a format suitable for blending with a video image. *See* RX-0073 at Fig. 2, 7:38-53, 34:16-46; *see also* RX-0382C (Medoff WS) at Q/A 264. In particular, Gloudemans explains that a "graphic signal can be sent as a YUV signal RGB signal, YCbCr signal or other appropriate signal according to the specifications of the keyer." RX-0073

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at 7:43-45. Accordingly, the administrative law judge has determined that Gloudemans discloses subject matter that satisfies this limitation.

f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

(1) Analysis of Respondents' Argument³⁵

Respondents' entire argument under their construction follows:

Respondents' Construction: Respondents' construction—"blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image"—incorporates the second part of the formula in the '104 Patent (*i.e.*, $AR(i) = AR(i-1) * (1 - A(i))$), is consistent with Broadcom's position in the *SiRF* litigation, and is consistent with the proper meaning that one of ordinary skill would give to this term. RX-0382C Q265; JX-0003 at 45:50-57; RX-0313.00017-19; *see also supra* Section VI.B.2.

Under this construction, Gloudemans in view of Porter & Duff (RX-0244) renders obvious limitation 1[e]. Porter & Duff discusses the "over" operator that blends two pictures (A and B) together using fractions F_A and F_B ; here, "1" and " $1 - \alpha_A$ " (α_A being the alpha value for picture A). RX-0244 at 256-58; RX-0382C Q269; RDX-0089.0052-54. Each blending operation uses two alpha values, and the blending results in a blended translucent image having a composite alpha that has been computed from the alpha values of all images that have been blended and where "each of the input colors is premultiplied by its alpha." *Id.* and Section VI.E.1.a. Because each use of the "over" operator uses the " $1 - \alpha_A$ " fraction in the calculation of the component-by-component blending operation, Gloudemans in view of Porter & Duff discloses this element under Respondents' construction. *Id.*

Resps. Br. at 264-65 (emphasis in original).

In Q/A 265, Dr. Medoff (respondents' expert) testified:

³⁵ Respondents' proposed construction is: "blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image." Resps. Br. at 252.

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Q265. For element 1[e], “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” do you have an opinion with respect to Gloudemans (RX-0073)?

A. Yes. As I discussed earlier, Respondents have offered a construction for element 1[e]: “blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” In the alternative, Respondents contend that this phrase renders the claim invalid under 35 U.S.C. section 112, second paragraph.

Broadcom asserts that this element is to be construed with its plain and ordinary meaning, but did not offer a particular construction for this phrase. And as I discussed earlier, it is my opinion that Respondents’ proposed construction which incorporates the second part of the “formula” in 45:50-57 of the ‘104 Patent, JX-0003, is consistent with the proper meaning that a person of ordinary skill in the relevant technological field would give to this term. Additionally, as I discussed earlier, Respondents and Broadcom have offered different constructions for the terms “a blended graphics image,” “the blended graphics image,” and “blended graphics image;” my opinions about element 1[e] with respect to Gloudemans are the same under any of those constructions.

RX-0382C (Medoff WS) at Q/A 265.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Gloudemans discloses subject matter that satisfies this limitation. Indeed, respondents’ brief presents an obviousness argument, and the testimony that it relies upon discusses claim construction. Further, under respondents’ constructions, respondents have not shown that Gloudemans discloses the two-step process of “blend[ing] the blended graphics image.” Gloudemans is vague as to when the blending occurs to disclose this element, nor is it clear that Gloudemans discloses the formula respondents contend should be included in the construction.

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Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Gloudemans discloses subject matter that satisfies this limitation under respondents' construction.

(2) Analysis of Broadcom's Argument

Respondents' entire argument is:

Complainant's construction/non-"two-step:" To the extent that limitation 1[e] is construed to cover a blending process other than the two-step blending process of Respondents' construction, one in which not all graphics are blended before blending with video, Gloudemans (RX-0073) discloses this limitation. Gloudemans explains that computer 94 works with computer 96 to create a graphic and a set of associated alpha signals; computer 96 can then send that created graphic, the "foreground," to keyer 98, which receives a video signal from frame delay 100, known as the "background." RX-0382C Q266; RX-0073 at 7:38-40, 7:54-63; RDX-0089.0041-45. Keyer 98 blends a foreground with a background "based on the level of the *alpha* or key from computer 96" on a "pixel by pixel basis," for both foreground and background. RX-0382C Q266; RX-0073 at 7:56-63; RDX-0089.0041-45. Gloudemans thus discloses this limitation under this construction. *See* RX-0424.0007.

"Two-step:" To the extent element 1[e] is construed to as a two-step blending process in which all graphics images are blended together before they are blended with video consistent with Respondents' construction, Gloudemans renders this limitation obvious. RDX-0382C Q267; RX-0073 at 7:38-65; RDX-0089.0044-45. Dr. Medoff explained that there are numerous operations to blend graphics with video, including 1) serially blending each graphic with video and 2) the "two-step" process of blending all graphics first before blending the result with video. RDX-0382C Q267. To the extent Gloudemans does not disclose the latter, one of ordinary skill would have been motivated to adopt it because it simplifies the blending of graphics and video and is merely a matter of design choice. RDX-0382C Q267; RX-0073 at 7:38-65; RDX-0089.0044-45.

Resps. Br. at 264 (emphasis in original).

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Broadcom argues that Gloudemans does not disclose the two-step blending process. *See* Broadcom Br. at 134, 138. Broadcom also argues that the system Gloudemans discloses requires knowledge for the “complete geometry of the camera[s]” in order to function. *Id.* at 138.

Respondents reply that camera geometry is “is irrelevant because the claims do not recite where the video signal must come from.” Resps. Reply at 96.

The evidence shows that, under Broadcom’s constructions, Gloudemans discloses subject matter that satisfies this limitation. For example, FIG. 2 of Gloudemans shows multiple graphics images have been blended with a video image, and the specification discloses that the graphics images have been blended using different alpha values. RX-0382C (Medoff WS) at Q/A 266. Indeed, this basic theory tracks Broadcom’s infringement and domestic-industry-technical-prong allegations. Further, having knowledge of the camera geometry is not relevant to an anticipation analysis, as camera positioning is not recited in the claims.

Accordingly, the administrative law judge has determined that Gloudemans, under Broadcom’s constructions, discloses subject matter that satisfies this limitation.

2. Claims 11 and 17

For claims 11 and 17, respondents simply refer to their arguments for claim 1; no new evidence or argument is presented. *See* Resps. Br. at 265-66.

For claims 11 and 17, Broadcom argues:

Respondents have not proven by clear and convincing evidence that independent claims 1, 11, and 17 of the ‘104 Patent are invalid in view of Gloudemans alone or in combination with Porter & Duff. CX-0578C (Havlicek WS) at Q/A 299-300. The following elements of Claim 1 are not disclosed or suggested by Gloudemans:

[D] blend a plurality of graphics images using a plurality of alpha values associated with the graphics

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images to generate a blended graphics image for storage in the at least one memory,

[E] process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

[F] blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

The same or similar three claim elements are also recited in claims 11 and 17. For the reasons discussed below, claims 1, 11 and 17 remain valid in view of Gloudemans and in view of Gloudemans combined with Porter & Duff.

Broadcom Br. at 135.

The administrative law judge previously determined that Gloudemans does not anticipate claim 1. Based upon the reasoning presented with respect to claim 1, and the parties' arguments that simply refer to claim 1, the administrative law judge has determined that Gloudemans does not anticipate claims 11 and 17.

3. Claim 10

Respondents argue:

Gloudemans alone or in combination with Porter & Duff discloses claim 10. RX-0073 at 7:38-45, Fig. 2; RX-0382C Q273; RDX-0089.0093-94. Gloudemans discloses that the graphics signal generated when computer 94 and computer 96 work together is sent as a "YUV signal, RGB signal, YCbCr signal or other appropriate signal." *Id.* For multiple graphics sent to keyer 98 to have been blended together, they would have been processed to have a common graphics data format. *Id.*; Tr. (Havlicek) 341:9-342:3.

Resps. Br. at 265.

For claims 10, 16, and 22, Broadcom argues:

Because Gloudemans (RX-0073) does not anticipate or render obvious independent claims 1, 11, and 17, then Gloudemans

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(RX-0073) also do not anticipate or render obvious claims 10, 16 and 22. CX-578C (Havlicek WS) at Q/A 261.

Broadcom Br. at 139-40.³⁶

Respondents cite the following portion of Gloudemans:

Computer 94 and computer 96 work together to create the graphic and a set of associated alpha signals. Both the graphic and alpha signals are sent to keyer 98. An alpha signal that is sent to keyer 98 is also called a key signal. Each pixel has its own key or alpha value. The graphic signal can be sent as a YUV signal RGB signal, YCbCr signal or other appropriate signal according to the specifications of the keyer.

RX-0073 at 7:38-45.

Dr. Medoff testified as follows:

Q273. What is your opinion with respect to claim 10 and Gloudemans (RX-0073)?

A As discussed earlier, Gloudemans (RX-0073), alone or in combination with Porter & Duff (RX-0244), discloses the limitations of claim 1. As shown on pages 92-93 of my claim chart, RDX-0089, Gloudemans (RX-0073) discloses that the graphic signal generated when computer 94 and computer 96 work together is sent as a “YUV signal, RGB signal, YCbCr signal or other appropriate signal.” In my opinion, for the graphics that make up the ultimately sent to the keyer 98 to be blended together, one of ordinary skill would understand that they would have a common graphics data format. In my opinion, Gloudemans (RX-0073) discloses the additional elements in claim 10[.]

RX-0382C (Medoff WS) at Q/A 273.

In response, Dr. Havlicek testified as follows:

Q357. Do you have an opinion concerning whether claim 10 is anticipated by Gloudemans (RX-0073)?

A Yes. It is my opinion that claim 10 is not anticipated by Gloudemans (RX-0073).

³⁶ CX-0578C (Havlicek RWS) at Q/A 261 pertains to Video Toaster.

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Q358. Can you please explain why?

A. Claim 10 is a dependent claim of independent claim 1. Gloudemans (RX-0073) does not anticipate or render obvious claim 10 because it does not anticipate or render obvious claim 1 for the reasons I have discussed above.

In addition, Gloudemans (RX-0073) does not disclose the element of claim 10 and Dr. Medoff's reliance in his answer to Question 231 on certain excerpts of Gloudemans (RX-0073) are inapposite. Gloudemans (RX-0073) does not disclose or suggest at least one processor operable to "convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format" as recited in claim 10.

CX-0578C (Havlicek RWS) at Q/A 357-58.

The administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Gloudemans discloses subject matter that satisfies the limitations particular to claim 10. Dr. Medoff's testimony explains that one of ordinary skill in the art would understand that graphics sent to the keyer would have a common graphics data.

RX-0382C (Medoff WS) at Q/A 273. While Dr. Havlicek believes the passage Dr. Medoff relies on is inapposite, he has not explained why the passage is inapposite or why Dr. Medoff is wrong. *See* CX-0578C (Havlicek RWS) at Q/A 357-58. Accordingly, if claim 1 is found anticipated, the administrative law judge would also find dependent claim 10 anticipated.

4. Claim 16 and 22

For claim 16, respondents' entire argument is:

See claim 10. RX-0382C Q273, 279; RDX-0089.0093-94, .0102; RX-0244 at 256-58.

Id. at 266. For claim 22, respondents' entire argument is:

See claim 16. RX-0382C Q273, 279, 280-81, 278; RDX-0089.0106.

Id.

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For claims 10, 16, and 22, Broadcom argues:

Because Gloudemans (RX-0073) does not anticipate or render obvious independent claims 1, 11, and 17, then Gloudemans (RX-0073) also do not anticipate or render obvious claims 10, 16 and 22. CX-578C (Havlicek WS) at Q/A 261.

Broadcom Br. at 139-40.

The administrative law judge previously determined claim 10 would be anticipated if claim 1 is found to be anticipated. Based on the parties' arguments, the administrative law judge would also find claims 16 and 22 are anticipated if claims 1 and 10 are found anticipated.

H. Anticipation – Myhrvold

In general, respondents argue that U.S. Patent No. 5,867,166 (“Myhrvold”) “anticipates claims 1, 11, and 17 of the ‘104 Patent under Broadcom’s constructions.” Resps. Br. at 267. Respondents argue that Myhrvold is prior art under 35 U.S.C. § 102(e) “because [it] was filed before November 9, 1998 (the earliest priority date of the ‘104 Patent, *see* RX-0683).” *Id.* at 241. Respondents note that Myhrvold is “listed on the face of the ‘104 Patent.” *Id.*

Broadcom argues, in part, that:

Myhrvold (RX-0083) does not anticipate or render obvious the claims of the ‘104 Patent. CX-578C (Havlicek WS) at Q/A 394. Myhrvold was considered by the Examiner during prosecution of the application that became the ‘104 Patent. *Id.* at Q/A 393; JX-0006.0393 (‘104 FH). The Examiner correctly determined that the claims of the ‘104 Patent were allowable over all cited prior art references, including Myhrvold, and allowed the claims. CX-578C (Havlicek WS) at Q/A 393; JX-0006.0386 (‘104 FH).

Myhrvold (RX-0073) is a Class A reference, and similar to the references (in that it discloses the traditional one-step approach to blending a graphics image with a graphics image) that were before the USPTO during related prosecution of ‘104 Patent, and the claims of the ‘104 Patent remain valid over Myhrvold. CX-578C (Havlicek WS) at Q/A 394. Myhrvold discloses a one-step process for blending gsprites one under another, and does not disclose the claimed two-step alpha blending process of the 104 Patent. *Id.*

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Therefore, Myhrvold does not anticipate or render obvious claim 1.
Id.

Broadcom Br. at 141-42.

1. Claim 1

- a) ***Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:***

Respondents' entire argument is:

Myhrvold discloses "One or more circuits for processing graphics and video images to produce a blended image." RX-0083 at Abstract, Fig. 4A, 6:50-7:4, 12:38-13:27; RX-0382C Q298; RDX-0090.0002-05. Broadcom does not dispute that Myhrvold discloses this element. CX-0578C (Havlicek) Q392-474. Myhrvold can "combine video and graphics" such as by applying "video to graphical objects" or by adding graphical objects to video data." RX-0083 at Abstract, 6:50-7:4; RX-0382C Q298; RDX-0090.2-5. Figure 4A illustrates an image processing board 174, which communicates with the host computer through bus 146, and includes DSP 176, tiler 200, shared memory 216, the gsprite engine 204, compositing buffer 210, and a digital-to-analog converter (DAC) 212.

Resps. Br. at. 269.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 142 (contesting limitations [E] and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Myhrvold discloses a circuit as described in the preamble. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 298 (and the evidence cited in the answer, except for RDX-0090); RX-0083 (Myhrvold) at Abstract, Fig. 4A, 6:50-7:4, 12:38-13:27. Accordingly, the administrative law judge has determined that Myhrvold discloses subject matter that satisfies the preamble.

- b) ***Limitation [B]: at least one interface operable to receive one or both of video and audio; and***

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Respondents' entire argument is:

Myhrvold discloses "at least one interface operable to receive one or both of video and audio." RX-0083 at Figs. 2, 4A, 10:48-56, 11:13-20 and 35-44, 12:38-13:27; RX-0382C Q299; RDX-0090.0005-09. Broadcom does not dispute that Myhrvold discloses this element. CX-0578C (Havlicek) Q392-474. Image processing board 174 communicates with the host computer and includes hardware and a PCI BUS. RX-0083 at Figs. 2, 4A, 10:48-66, 12:9-67-13:27; RX-0382C Q299; RDX-0090.0005-09. The PCI BUS transfers commands and data between the host and DSP 176 and renders images and transfers display images to display device 142 through DAC 212. *Id.* Myhrvold's PCI BUS meets [limitation [B]].

Resps. Br. at 258.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 142 (contesting limitations [E] and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Myhrvold discloses a circuit including an interface that can receive video and audio. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 298 (and the evidence cited in the answer, except for RDX-0090); RX-0083 (Myhrvold) at Abstract, Fig. 4A, 6:50-7:4, 12:38-13:27. Accordingly, the administrative law judge has determined that Myhrvold discloses subject matter that satisfies this limitation.

- c) ***Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:***

Respondents' entire argument is:

Myhrvold discloses "at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits." RX-0382C Q300; RX-0073 at Figs. 1, 4A, 13, 7:9-22, 12:39-56, 13:17-23, 29:4-8; RDX-0090.0009-13. Broadcom does not dispute that Myhrvold discloses this element. CX-0578C (Havlicek) Q392-474. Myhrvold shows image processor 106 in Figure 1, which includes tiler 200, gsprite engine 204, compositing buffer 210, and DAC

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212. RX-0382C Q300; RX-0073 at Figs. 1, 4A, 7:9-22, 12:39-56; RDX-0090.0009-13. Image processing board 174 is operably coupled to the PCI BUS and includes shared memory 216. *Id.* Myhrvold's image processor thus discloses [limitation [C]].

Resps. Br. at 270.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 142 (contesting limitations [E] and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Myhrvold discloses a processor as described in claim 1. *See, e.g.,* RX-0382C (Medoff WS) at Q/A 300 (and the evidence cited in the answer, except for RDX-0090); RX-0083 at FIGS. 1, 4A, 13, 7:9-22, 12:39-56, 13:17-23, 29:4-8. Accordingly, the administrative law judge has determined that Myhrvold discloses subject matter that satisfies this limitation.

d) *Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,*

Respondents argue, in part:

Myhrvold discloses this element under Respondents' construction of "a blended graphics image" ("data representing a single view of a mixture of at least two graphics images") as well as Complainant's construction of "blended graphics image" (same construction). RX-0382C Q301-05; RX-0424.0006; RDX-0090.0013-40. Myhrvold explains that "pixels in [each] gsprite have color and alpha (opacity) information associated with them, so that multiple gsprites can be composited together to create the overall scene." *Id.*; RX-0382C Q301; RX-0083 at 7:58-62. Myhrvold thus discloses blending a plurality of graphics images. More specifically, image processor 106 "composites the resulting pixel data," which "includes computing the color and alpha for pixels in output device coordinates based on the gsprite transforms," transforming "the pixel data for gsprites in the display list," and compositing "the transformed pixel data." RX-0382C Q301; RX-0083 at Fig. 1, 16:46-54; RDX-0090.0013-40. "The process involves determining the color and alpha at a pixel location based on the contribution of one or more pixel values from gsprites

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that cover that pixel location.” *Id.* Myhrvold explains that the compositing buffer stores the resulting blended gsprites; “the gsprite engine 204 . . . perform[s] the necessary image processing for general affine transformations (which include scaling, translation with subpixel accuracy, rotation, reflection and shearing)” and that “after filtering, the resulting pixels (with alpha) are sent to the compositing buffers where display pixel data is calculated.” RX-0382C Q301; RX-0083 at 13:9-15; RDX-0090.0013-40. Myhrvold discusses sample equations for computing alpha and color during the blending process, computing alpha as $A_{new} = A_{old} - (A_{old} * A_{in})$ and color as $C_{new} = C_{old} + (C_{in} * (A_{old} * A_{in}))$ (front-to-back blending), and alpha as $A_{new} = A_{in} + ((1 - A_{in}) * A_{old})$ and color as $C_{new} = (C_{in} * A_{in}) + ((1 - A_{in}) * C_{old})$ (back-to-front blending). RX-0382C Q301; RX-0083 at 71:29-72:35; RDX-0090.0013-40. To the extent Broadcom argues that the use of a single “alpha signal” is insufficient to disclose the “plurality of alpha values associated with the graphics images,” Dr. Havlicek testified that a single or fixed alpha value can be “associated with” a graphics image if it describes and specifies the opacity of the pixels in the image. Tr. (Havlicek) 351:17-352:20. See Section VI.E.1.c.i (explaining that a single alpha value associated with a plurality of images meets the claim language). Because the pixels of each gsprite have alpha values associated with them, and blending them together causes the blended gsprite to be stored in a compositing buffer, RX-0382C at Q301, Myhrvold discloses element 1[c].

Resps. Br. at 270-71.

Broadcom does not clearly rebut this argument. See generally Broadcom Br. at 142 (contesting limitations [E] and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Myhrvold discloses a processor that can blend a plurality of graphics images using a plurality of alpha values, as described in claim 1. See, e.g., RX-0382C (Medoff WS) at Q/A 301 (and the evidence cited in the answer, except for RDX-0090).

- e) ***Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and***

Respondents’ entire argument is:

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Myhrvold discloses “process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image.” RX-0382C Q306; RX-0083 at Fig. 12A, 7:63-66, 13:9-15, 19:60-20:8, 27:3-11, 43:51-44:6, 60:66-61:23; RDX-0090.0040-44. Broadcom’s expert agreed that this limitation “means [] that the format of the video and the graphics must match” when the video and graphics reach the “blending circuit.” Tr. (Havlicek) 341:9-342:3. Myhrvold (RX-0083) explains that the gsprite engine can perform image processing for general transformations (e.g., scaling and translation) to mimic motion and to match the priorities of a “scene” such as a background video image. RX-0382C Q306; RX-0083 at Fig. 12A, 7:63-66, 8:12-17, 13:9-15, 27:3-11, 61:11-23; RDX-0090.0040-44. Gsprite engine 204 can also transform gsprite data in AYUV format to ARGB format before sending it to the compositing buffer. *Id.* Because the graphic and video are blended together, using image processing to match the “priorities” of a “scene” such as a background video image, the gsprite and scene must be in the same format when they reach the compositing buffer—as Dr. Havlicek asserted the claims require. Tr. (Havlicek) 341:9-342:3. Thus, Myhrvold discloses element 1[d]. RX-0382C Q306; RX-0083 at Fig. 12A, 7:63-66, 13:9-15, 19:60-20:8, 27:3-11, 60:66-61:23, 43:51-44:6; RDX-0090.0040-44.

Resps. Br. at 272-73.

Broadcom argues:

Myhrvold (RX-0083) does not disclose Element [E] or [F] as listed above because Myhrvold does not disclose blending a graphics image with a video image. *Id.* at Q/A 396, 406, 443-444, 459-460. The invention disclosed in Myhrvold (RX-0083) represents graphics images as objects called “generalized sprites” or “gsprites.” *Id.* at Q/A 397; RX-0083 (Myhrvold) at 4:38-40; 7:58-59; 8:20-27; 9:20-21; 27:23-29. “The term ‘gsprite’ refers generally to an image layer that can be composited with other image layers to form a display image.” RX-0083 (Myhrvold) at 4:38-40.

Instead of disclosing the claimed two-step alpha blending process in the ‘104 Patent, Myhrvold discloses a graphics system for rendering an animation by combining gsprites using a one-step blending method. CX-578C (Havlicek WS) at Q/A 398. For example, the system can perform a wide variety of operations on gsprites, including gsprite compositing (blending). RX-0083 (Myhrvold) at 7:63-8:17, 7:58-62, 27:7-11, 62:30-36; CX-578C

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(Havlicek WS) at Q/A 398. But Myhrvold does not disclose a two-step method as claimed in the '104 Patent wherein a plurality of graphics images are first blended together using alpha values and the blended graphics image is then blended with a video image using the alpha values. CX-578C (Havlicek WS) at Q/A 398. It is not taught or suggested anywhere in Myhrvold how a video image could be rendered to a gsprite or represented by a gsprite. *Id.* Further, Myhrvold does not disclose blending of gsprites with objects that are not gsprites. *Id.* Therefore, under Respondents' or Broadcom's claim constructions, Myhrvold (RX-0083) cannot disclose placing "the blended graphics image in a format suitable for blending with a video image." *Id.*

Broadcom Br. at 142-43.

Respondents reply, in part, that "Broadcom ignores numerous portions of Myhrvold, cited by Respondents, that explicitly discuss blending images with video." Resps. Reply at 97 (citing RX-0083 at 6:50-66).

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Myhrvold discloses a processor that processes graphics images into a format suitable for blending.

Respondents rely on, and cite to, Q/A 306 of Dr. Medoff's testimony. *See* Resps. Br. at 272-73 (citing RX-0382 (Medoff WS) at Q/A 306). In Q/A 306, Dr. Medoff testified as follows:

Q306. For element 1[d], "process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image," do you have an opinion with respect to Myhrvold (RX-0083)?

A. . . . In light of these constructions, in my opinion, Myhrvold (RX-0083) at 13:9-15, explains that the gsprite engine on image processing board 174, depicted in detail in Figure 12A, which I have on page 43 of the claim chart attached to my expert report, RDX-0090, and described in part at 27:3-11 of Myhrvold (RX-0083) operates at "video rates," that is, at rates necessary to support blending of gsprites with video, to perform image processing for general transformations such as scaling, translation, rotation, reflection, and shearing, as well as filtering. 61:18-22 notes that this "video rates" processing can be, for example, 75

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hertz (Hz). 7:63-66 of Myhrvold (RX-0083) also discusses operations such as scaling, rotation, subpixel positioning, transformations to mimic motion, and others. 8:12-17 explains that gsprites can be filtered and scaled to an appropriate size to match the priorities of the scene, that is, the background video image. 61:11-23 also discusses the process of display generation, during which the gsprite engine 204 in image processing board 174 can transform the gsprite data in AYUV format by reading it from memory, decompressing it, transforming it, filtering it, and converting it to ARGB format, before sending it to the compositing buffer at video rates.

In my opinion, Myhrvold's disclosure of the gsprite engine performing image processing including color space conversion from AYUV to ARGB, scaling to match the "priorities" of a "scene" such as a background video image, makes clear that Myhrvold (RX-0083) "adjusts the blended graphics image based on a video image to make the format of the blended graphics image compatible for blending," as required by Respondents' construction of [limitation [E]], as well as under Broadcom's construction, which is what they refer to as the "plain and ordinary meaning" of the term. Other portions of Myhrvold (RX-0083) that I discussed in that claim chart, RDX-0090, including 19:60-20:8, 27:3-11, 43:51-44:6, 60:66-61:23, also support my opinion that Gloudemans (RX-0073) discloses this element.

RX-0382 (Medoff WS) at Q/A 306. Dr. Medoff's opinion that a system operating "at video rates" constitutes blending gsprites with video does not actually identify a video image. *See id.*; *see also* CX-0578C (Havlicek RWS) at Q/A 398 ("It is not taught or suggested anywhere in Myhrvold how a video image could be rendered to a gsprite or represented by a gsprite. Furthermore, Myhrvold does not disclose blending of gsprites with objects that are not gsprites."). Accordingly, the administrative law judge has determined that respondents have not shown that Myhrvold discloses subject matter that satisfies this limitation.

f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

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(1) Analysis of Respondents' Argument³⁷

Respondents' entire argument under their construction follows:

Respondents' Construction: Respondents' construction—"blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image"—incorporates the second part of the formula in the '104 Patent (*i.e.*, $AR(i) = AR(i-1) * (1 - A(i))$), agrees with Broadcom's earlier position in the *SiRF* litigation, and is consistent with the proper meaning that one of ordinary skill would give this term. RX-0382C Q307; JX-0003 at 45:50-57; RX-0313.00017-19; *see also* Section VI.B.2.

Under this construction, Myhrvold in view of Porter & Duff renders [limitation [F]] obvious. Myhrvold includes equations for compositing, including when gsprites are sorted in front-to-back order (alpha value for each pixel is $A_{new} = A_{old} - (A_{old} * A_{in})$; color is $C_{new} = C_{old} + (C_{in} * (A_{old} * A_{in}))$) and when gsprites are sorted in back-to-front order (alpha value for each pixel is $A_{new} = A_{in} + ((1 - A_{in}) * A_{old})$; color is $C_{new} = (C_{in} * A_{in}) + ((1 - A_{in}) * C_{old})$). RX-0382C Q309; RX-0083 at 71:29-72:35; RDX-0090.0044-66. Using "Aold" to calculate "Anew" requires computing and maintaining alpha values for each subsample. RX-0083 at 71:29-72:35; RX-0382C Q311. That yields a composite alpha value similar to that in the '104 Patent. RX-0382C Q309; RX-0083 at 71:29-72:35. *Compare* JX-0003 at 45:50-57, 46:6-17 ($AR(i) = AR(i-1) * (1 - A(i))$) with RX-0083 at 62:30-36 ($Alpha(new) = Alpha(dst) * (1 - Alpha(src))$). The formula in Myhrvold meets [limitation [F]]. RX-0382C Q309, 311.

Resps. Br. at 274-75 (emphasis in original).

Broadcom argues:

Myhrvold (RX-0083) does not disclose Element [E] or [F] as listed above because Myhrvold does not disclose blending a graphics image with a video image. *Id.* at Q/A 396, 406, 443-444, 459-460. The invention disclosed in Myhrvold (RX-0083) represents graphics images as objects called "generalized sprites" or "gsprites." *Id.* at Q/A 397; RX-0083 (Myhrvold) at 4:38-40; 7:58-

³⁷ Respondents' proposed construction is: "blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image." Resps. Br. at 252.

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59; 8:20-27; 9:20-21; 27:23-29. “The term ‘gsprite’ refers generally to an image layer that can be composited with other image layers to form a display image.” RX-0083 (Myhrvold) at 4:38-40.

Instead of disclosing the claimed two-step alpha blending process in the ‘104 Patent, Myhrvold discloses a graphics system for rendering an animation by combining gsprites using a one-step blending method. CX-578C (Havlicek WS) at Q/A 398. For example, the system can perform a wide variety of operations on gsprites, including gsprite compositing (blending). RX-0083 (Myhrvold) at 7:63-8:17, 7:58-62, 27:7-11, 62:30-36; CX-578C (Havlicek WS) at Q/A 398. But Myhrvold does not disclose a two-step method as claimed in the ‘104 Patent wherein a plurality of graphics images are first blended together using alpha values and the blended graphics image is then blended with a video image using the alpha values. CX-578C (Havlicek WS) at Q/A 398. It is not taught or suggested anywhere in Myhrvold how a video image could be rendered to a gsprite or represented by a gsprite. *Id.* Further, Myhrvold does not disclose blending of gsprites with objects that are not gsprites. *Id.* Therefore, under Respondents’ or Broadcom’s claim constructions, Myhrvold (RX-0083) cannot disclose placing “the blended graphics image in a format suitable for blending with a video image.” *Id.*

Myhrvold (RX-0083) also does not disclose “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” as recited in claim 1. *Id.* at Q/A 406. Myhrvold (RX-0083) only discloses how to blend gsprites together in a one-step process, and Myhrvold does not disclose how to blend gsprites with video images. *Id.* at Q/A 407 (citing RX-0073 at 7:58-62, 27:7-11, 62:30-36). Accordingly, under either Respondents’ or Broadcom’s claim constructions, Myhrvold does not disclose at least one processor operable to “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” as required by claim 1 of the ‘104 Patent. CX-578C (Havlicek WS) at Q/A 407, 408, 409 (citing RX-0083 at 15:31-32; 15:23-35).

Broadcom Br. at 142-43.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Myhrvold

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discloses a processor that blends a blended graphics image with video. Myhrvold suggests that its system “can be used to apply video to graphical objects, or conversely, can be used to add graphical objects to video data.” However, Myhrvold’s focus lies on 3-D animation. *See* RX-0083 (“Due to the novel architecture and image processing techniques employed in the system, it can produce sophisticated real time 3-D animation at a significant cost savings over present graphics systems.”). Myhrvold does not clearly disclose combining graphics images with video images. *See* CX-0578C (Havlicek RWS) at Q/A 405-410.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Myhrvold discloses subject matter that satisfies this limitation.

(2) Analysis of Broadcom’s Argument

Respondents’ entire argument is:

Complainant’s construction/non-“two-step”/any formula: If [limitation [F]] is construed to cover a blending process in which not all graphics are blended together before being blended with video and/or a process using any formula for blending, Myhrvold discloses this limitation. RX-0382C Q309-11. The compositing buffer in Myhrvold may have two scanline buffers, one of which is used for compositing gsprites (to create a blended graphics image) and one of which is used to generate video data for display by compositing the gsprites with video (to blend the blended graphics image with a video image). *Id.* at Q309. To the extent that “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” is construed with Complainant’s construction of “plain and ordinary meaning,” Myhrvold discloses this element as discussed above.

“Two-step:” If [limitation [F]] is construed to require a two-step blending process in which graphics images are blended together before they are blended with video, Myhrvold (RX-0083) renders this element obvious. Myhrvold is configured for blending images in a particular order, from distance to the viewpoint. RX-0382C Q311; RX-0083 at 15:30-35. Blending all images together first before blending with video reduces delay in the display of the

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video because blending the blended image with the video may be faster than serially blending each image with a video image. For example, during the video games discussed in Myhrvold (RX-0083), certain gsprites may be static compared to other gsprites. RX-0382C Q311; RX-0083 at 34:53-35:26. Reusing relatively static blended gsprites (instead of reblending each time) can save on processing power and would lend itself to the combination with a video image such as a background image. Dr. Medoff explained that there are two options for blending graphics with video, including 1) serially blending each graphic with video and 2) the “two-step” process of blending all graphics first before blending the result with video. RDX-0382C Q311. To the extent Myhrvold does not disclose the latter, one of ordinary skill would have been motivated adopt the two-step process because it simplifies the bending of graphics and video and is merely a simple matter of design choice (being of two different options for blending). *Id.*; RX-0033 at 15:30-35, 71:50-72:8; RDX-0090.0044-66.

Resps. Br. at 273-74 (emphasis in original).

Broadcom argues that Myhrvold does not disclose the two-step blending process. *See* Broadcom Br. at 143. Broadcom also argues that “Myhrvold (RX-0083) only discloses how to blend gsprites together in a one-step process, and Myhrvold does not disclose how to blend gsprites with video images.” *Id.*

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Myhrvold discloses a processor that blends a blended graphics image with video. The same analysis provided with respect to respondents’ constructions, *see* § IV(J)(1)(f)(1), *supra*, applies here.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Myhrvold discloses subject matter that satisfies this limitation.

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2. Claims 11 and 17

For claims 11 and 17, respondents simply refer to their arguments for claim 1; no new evidence or argument is presented. *See* Resps. Br. at 265-66.

Broadcom argues that because Myhrvold does not disclose limitations [E] and [F] from claim 1, it also does not anticipate claims 11 and 17. Broadcom Br. at 142.

The administrative law judge previously determined that Myhrvold does not anticipate claim 1. Based upon the reasoning presented with respect to claim 1, and the parties' arguments that simply refer to claim 1, the administrative law judge has determined that Myhrvold does not anticipate claims 11 and 17.

3. Claim 10

Respondents argue:

Myhrvold alone or in combination with Porter & Duff discloses claim 10. RX-0382C Q317; RX-0083 at Fig. 4A, 12:50-13:8, 61:18-21; RDX.0090.0099-101. Figure 4A of Myhrvold shows tiler 200, which performs color space conversion. RX-0083 at 12:50-13:8; RX-0382C at (Medoff) Q317; RDX-0090.0101. Figure 4A shows that tiler 200 is before the compositor 210 in the image processor pipeline. RX-0083 at Fig. 4A, 12:50-13:8; RX-0382C at (Medoff) Q317; RDX-0090.0101. Both of the color space conversion process in tiler 200 (before blending) and the AYUV-to-ARGB conversion of gsprites (before compositing) discloses the claimed "convert graphics data format of at least one of the plurality of graphics images such that the plurality of graphics images have a common graphics data format." RX-0382C Q317; RX-0083 at Fig. 4A, 12:50-13:8, 61:18-21; RDX-0090.0099-101.

Resps. Br. at 276.

Broadcom's entire argument for claims 10, 16, and 22 is:

Because Myhrvold (RX-0083) does not anticipate or render obvious independent claims 1, 11, and 17, then Myhrvold (RX-0083) also do not anticipate or render obvious claims 10, 16 and 22. CX-578C (Havlicek WS) at Q/A 441, 458, 474.

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Broadcom Br. at 143-44.

Dr. Medoff's testimony explains that Myhrvold (RX-0083 at 12:50-13:8, 61:18-21, and Figure 4A) alone discloses subject matter that teaches converting graphics data prior to blending graphics images, as claim 10 requires. *See* RX-0382C (Medoff WS) at Q/A 317. Dr. Havlicek does not address these portions of Myhrvold; his testimony only refers to claim 1. *See* CX-0578C (Havlicek WS) at Q/A 441 ("Myhrvold (RX-0083) does not anticipate or render obvious claim 10 because it does not anticipate or render obvious claim 1 for the reasons I have discussed above.").

The administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Myhrvold discloses subject matter that satisfies claim 10. Dr. Medoff's testimony explains that the color space conversion process and gsprite conversion teaches claim 10. RX-0382C (Medoff WS) at Q/A 317. Dr. Havlicek has not rebutted Dr. Medoff's testimony. *See* CX-0578C (Havlicek RWS) at Q/A 441. Accordingly, if claim 1 is found anticipated, the administrative law judge would also find dependent claim 10 anticipated.

4. Claims 16 and 22

For claims 16 and 22, respondents simply refer to claims 10 and 16, respectively. Resps. Br. at 276-77. Broadcom does not present a separate argument for claims 16 and 22. Broadcom Br. at 143-44.

The administrative law judge previously determined claim 10 would be anticipated if claim 1 is found to be anticipated. Based on the parties' arguments, the administrative law judge would also find claims 16 and 22 are anticipated if claims 1 and 10 are found anticipated.

I. Anticipation – Video Toaster

Respondents argue:

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The Video Toaster System has three components: 1) the Commodore Amiga 4000, which is a multimedia computer that has a general-purpose Motorola 68040 processor and a custom graphics chipset; 2) a Video Toaster 4000, which is a video and graphics processor containing several chips for processing video and graphics; and 3) the Video Toaster Flyer, which is a video, graphics, and audio storage system. RX-0382C at Q207-208.

Resps. Br. at 278. Respondents cite five exhibits—RX-0410, RX-0411, RX-0412, RX-0413, RX-0414—in discussing the system. *Id.* at 278-290.

In general, Broadcom argues that Video Toaster is non-analogous art. Broadcom Br. at 125. Broadcom further argues that Video Toaster does not disclose limitations [D], [E], or [F] of claim 1. *Id.* at 127.

1. Claim 1

- a) Limitation [A]: One or more circuits for processing graphics and video images to produce a blended image, the one or more circuits comprising:*

Respondents' entire argument is:

The Video Toaster System discloses [limitation [A]]. RX-0382C at Q218. The Commodore Amiga 4000 includes an AGA custom graphics chipset, which comprises a circuit for processing graphics and video images to produce a blended image. RX-0382C at Q218; RX-0411.00002 (Commodore Amiga 4000). The NewTek Video Toaster 4000 is a video and graphics processor sub-system that includes several chips for processing video and graphics. RX-0382C at Q218; RX-0412.11-12 (Developer's Handbook). The ToasterPaint program can be used to load, edit, and save 2-bit, 4-bit, or 8-bit alpha graphics images to and from the framestore or disk. RX-0382C at Q218; RX-0413.00224-25 (Video Toaster 4000 Manual). The Toaster can continuously digitize, store, 'undigitize' and replay an incoming NTSC video signal. RX-0382C at Q218; *See* Figure 1, top portion, and note the digital video frame stores (RAM0, RAM1) and the digital video flow pathway (ADC, FIFO, RAM0/I, DAC0/I). "When the Toaster is in 'digital' mode, the two frame stores (which are shown as highlighted buttons on the Switcher screen in digital mode) contain digitized versions of whatever video source is incoming on the

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MAIN Toaster bus.” RX-0382C at Q218; RX-0412.00043 (Developer’s Handbook).

The Transparency and Warping Panel provides “tremendous power to blend graphics seamlessly.” RX-0382C at Q218; RX-0413.00252 (Video Toaster 4000 Manual). Graphics can be blended in ToasterPaint using, *e.g.*, the MergePicture function, where “the whole back picture is the paint that can act on the front picture” using features such as transparency control. RX-0382C at Q218; RX-0413.00260. Graphics objects can be loaded into LightWave3D or rendered within the program as background images or foreground images and blended with other graphics objects. RX-0382C at Q218; RX-0413.00332, 397. The FG Alpha Image button allows the user to perform alpha channel image compositing of an entire scene (*e.g.*, the rendered image of the scene as set up in Layout, and the loaded image selected as Foreground Image) or just two images together (the Foreground Image with a selected Background Image). RX-0382C at Q218; RX-0413.00397. Graphics objects from ToasterPaint or LightWave3D can be stored in the Toaster’s framestores, and the inputs to the framestores (*e.g.*, the digital video) can be blended together with the blended graphics image. RX-0382C at Q218; RX-0412.00011-12, 43 at Fig. 1.

Resps. Br. at. 280-81.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 127 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents’ brief shows that Video Toaster discloses a circuit as described in the preamble. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 218 (and the evidence discussed in the answer, except for RDX-0092). Accordingly, the administrative law judge has determined that Video Toaster discloses subject matter that satisfies the preamble.

b) Limitation [B]: at least one interface operable to receive one or both of video and audio; and

Respondents’ entire argument is:

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The Video Toaster System discloses [limitation [B]]. RX-0382C at Q219. The Video Toaster System, may receive video signals from any of four video inputs or from either of two digital framestores. *Id.* These may be routed to the AMUX or BMUX and then through the A/B FADER. *Id.*; RX-0412.00011-12, 43 (Developer's Handbook) at Fig. 1; RDX-0092.8. The Developer's Handbook lists signals that may be routed through the A and B multiplexers: VID 1, VID 2, VID 3, and VID 4 (video inputs to the Toaster); DAC 0 and DAC 1 (inputs from the Toaster's digital video banks); ENCODER (allows RGB graphics stored on the Amiga to be input to the Toaster); and MONOCHROME (allows monochrome and luminance keying settings from any of the aforementioned signals to be input to the Toaster). RX-0382C at Q219; RX-0412.00014.

Resps. Br. at 258.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 127 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Video Toaster discloses a circuit including an interface that can receive video and audio. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 219 (and the evidence discussed in the answer, except for RDX-0092). Accordingly, the administrative law judge has determined that Video Toaster discloses subject matter that satisfies this limitation.

- c) ***Limitation [C]: at least one processor operably coupled to the at least one interface and to at least one memory located within or external to the one or more circuits, the at least one processor operable to:***

Respondents' entire argument is:

The Video Toaster System discloses [limitation [C]]. RX-0382C at Q220. It includes a video and graphics processor and circuits coupled to the interfaces. *Id.* The A/B FADER is a circuit coupled to the AMUX and BMUX circuits, which are coupled to the four video input sources, the two digital framestores, the ENCODER (RGB graphics) input, and the MONOCHROME (monochrome and luminance keying). *Id.*; RX-0412.00014 at Fig. 1. The Video Toaster System is coupled to memory, as the framestores, labeled

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RAM0 and RAM1 in the block diagram of Fig. 1 of the Developer's Handbook, are memory. RX-0382C at Q220; RX-0412.00043, Fig. 1. The Amiga 4000 is a computer including a multimedia processor and a hard disk drive and DRAM memory. RX-0382C at Q220; RX-0410.00010 (A4000).

Resps. Br. at 281.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 127 (contesting limitations [D], [E], and [F] only); Broadcom Reply, Section II(E).

The evidence and argument cited in respondents' brief shows that Video Toaster discloses a processor as described in claim 1. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 300 (and the evidence discussed in the answer, except for RDX-0092). Accordingly, the administrative law judge has determined that Video Toaster discloses subject matter that satisfies this limitation.

- d) *Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,***

Respondents argue, in part:

The Video Toaster System discloses and/or renders obvious [limitation [D]]. RX-0382C at Q221. The Video Toaster System includes software programs that use components of the Amiga 4000 and the Toaster sub-system. RX-0382C at Q221. These software programs include the ToasterPaint and the LightWave3D programs, each of which is capable of blending graphics images using an alpha channel to generate a blended graphics image, which can be stored in memory. *Id.*

The ToasterPaint program can be used to load, edit, and save 2-bit, 4-bit, or 8-bit alpha graphics images to and from the framestore or disk RX-0382C at Q221; RX-0413.00224-25. This allows the transparency of an image (or parts of an image) to be adjusted by changing the alpha value of the image. RX-0382C at Q221; RX-0413.00231....

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The Video Toaster System also includes a program called LightWave3D, described in the Video Toaster 4000 Manual. RX-0382C at Q221; RX-0413.00332-435. A user may use LightWave3D to render and model three-dimensional graphics, which may then be stored and used as objects. RX-0382C at Q221. . . . The graphics, objects, scenes, and animations rendered in LightWave can be stored individually or in combination on the Video Toaster System (including the framestore of the Toaster or the hard disk of the Amiga). RX-0382C at Q221; RX-0413.00334-35, 359, 379-80, 391, 400-402.

Resps. Br. at 281-82.

Broadcom argues that Video Toaster does not blend a plurality of graphics images using alpha values. Broadcom Br. at 128-29 (“The Video Toaster does not teach, and Dr. Medoff has not shown, that the NewTek hardware card is capable of blending the prestored LightWave graphics image with another graphics image.”).

Respondents’ reply argues that “there are two subsystems, ToasterPaint and LightWave 3D, that can blend a plurality of graphics images to create a blended graphics image.” Resps. Reply at 97.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Video Toaster discloses a processor that blends graphics images. *See* CX-0578C (Havlicek RWS) at Q/A 205-06 (providing background on how a user must create the blended images in the Video Toaster system).

As an initial point, Dr. Medoff’s testimony opines on what Video Toaster “can” do rather than providing a firm description of how the system operates. *See* RX-0382C (Medoff WS) at Q/A 221. Dr. Medoff cites to various portions of the Video Toaster Manual (RX-0413) that provide a user with directions on how to use the system—the system does not operate autonomously. *Id.* For example, in opining that Video Toaster discloses blending graphics, Dr.

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Medoff cites to page 260 and states that “Graphics can be blended in ToasterPaint, for example, using the MergePicture function, where ‘the whole back picture is the paint that can act on the front picture’ using features such as transparency control.” *Id.* This is the section of page 260 that Dr. Medoff relies on:

Merging Pictures

Remember, with Merge Picture, the whole back picture is the paint that can act on the front picture with any of the Mode menu features. Try bringing a picture into the front using Transparency controls for a "soft-focus" effect.

RX-0413 at 260. The entirety of page 260, however, is directed to “Miscellaneous Tips” that provide guidance to a human user. For example, the “Miscellaneous Tips” provide the user with guidance on what to do when he or she receives unexpected results:

Unexpected Results

If you're not getting what you expect when you draw, check to see what Drawing mode you're in, or see if you've left the Transparency controls on. Usually, unexpected results are caused by a control from another panel that has been "left on."

Press the Tab key to return ToasterPaint to its default settings and try again.

Id. The same page of the manual also provides guidance on how a user can open a file faster:

Loading Files Faster

Files can be opened by double-clicking on the file name.

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Id. Video Toaster clearly does not disclose a processor that is operable to blend a plurality of graphics images, as limitation [D] requires. *See* CX-0578C (Havlicek RWS) at Q/A 199 (“Toaster Paint provides a human user with the capability to draw or import graphics images, edit and save graphics images, and alpha blend graphics images, all manually using keyboard and mouse commands.”).

Dr. Medoff’s testimony about using alpha blending is similarly deficient. For example, Dr. Medoff opines that using an alpha channel satisfies the “plurality of alpha values” aspect of limitation [D]. *See* RX-0382C (Medoff WS) at Q/A 221 (citing RX-0413 at 231, 397). The descriptions provided in RX-0413 at 231, 397 (as well as Dr. Medoff’s testimony), however, are too superficial to find that the Video Toaster system performs alpha blending.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Video Toaster discloses subject matter that satisfies this limitation.

- e) ***Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and***

Respondents’ entire argument is:

The Video Toaster System discloses [limitation [E]]. RX-0382C.61. As discussed above with respect to [limitation [D]], the ToasterPaint and the LightWave3D programs can generate a blended graphics image, and the blended graphics image can be stored in the Amiga 4000’s hard drive or the Video Toaster’s framestore. *Id.* The ToasterPaint and LightWave3D program process images in RGB format. *Id.* When an image is ready for transfer to the Video Toaster 4000, the image is converted from RGB format to digital NTSC format through a process described in the Developer’s Handbook at RX-0412.5. *Id.* The images in the framestores, labeled RAM0 or RAM1 in Fig. 1 of the Developer’s Handbook, may be blended with video in NTSC format by the A/B FADER circuit. *Id.*; *see also* RX-0412.12-14, Fig. 1. The digital image in framebuffers RAM0

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or RAM1 is converted from digital NTSC format in RAM0 or RAM1 to analog NTSC format by DAC0 or DAC1 so that it is in a format suitable for blending with a video image. RX-0382C.61; *see also* RX-0412.12, Fig. 1.

The Developer's Handbook describes these functions: "DAC0 – video from the Toaster's #1 Digital Video Bank (DVI), after being converted into NTSC analog video by the Toaster's Digital to Analog converter (DAC) #0" and "DAC1 – video from the Toaster's #2 Digital Video Bank (DV2), after being converted into NTSC analog video by the Toaster's Digital to Analog converter (DAC) #1." RX-0382C.000061; RX-0412.00014. Accordingly, the blended graphics image output from ToasterPaint or LightWave3D, which is in RGB color space, is converted to an NTSC signal for blending with video. RX-0382C.000061. Because the images and video are both in NTSC format when blended, they are in the same format when they reach the A/B FADER for blending—as Dr. Havlicek asserts the claims require. Tr. (Havlicek) 341:9-342:3; *supra* Section VI.E.1.c.i. Thus, the Video Toaster System discloses [limitation [E]].

Resps. Br. at 285-86.

Broadcom argues:

... Video Toaster also does not disclose claim elements [E] above because it does not disclose "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image."

Broadcom Br. at 128.

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Video Toaster discloses a processor that processes graphics images into a format suitable for blending. Dr. Havlicek, Broadcom's expert, testified as follows:

Q213. What other element of claim 1 is not disclosed by Video Toaster System (RX-0411 through RX-0414)?

A. Video Toaster System (RX-0411 through RX-0414) does not disclose "process the graphics images and/or the blended graphics

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image to place the blended graphics image in a format suitable for blending with a video image,” as recited in claim 1.

Q214. Can you please explain the bases of your opinion?

A. Yes. For the reasons provided earlier, Video Toaster System (RX-0411 through RX-0414) does not disclose “blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.” Therefore, Video Toaster System (RX-0411 through RX-0414) cannot disclose placing “the blended graphics image in a format suitable for blending with a video image.”

CX-0578C (Havlicek RWS) at Q/A 213-14.

The administrative law judge previously determined that respondents have not shown that Video Toaster disclosed limitation [D]. The administrative law judge has determined that Video Toaster does not disclose placing “the blended graphics image in a format suitable for blending with a video image.” *See* CX-0578C (Havlicek RWS) at Q/A 213-14. Accordingly, the administrative law judge has determined that respondents have not shown that Video Toaster discloses subject matter that satisfies this limitation.

f) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

(1) Analysis of Broadcom’s Argument

Respondents’ entire anticipation argument for this limitation, with respect to Video Toaster, follows:

The Video Toaster System discloses [limitation [F]], especially if it is construed to cover a blending process other than a two-step blending process. RX-0382C.000061. As discussed with respect to [limitation [D]], the Video Toaster System can generate a blended graphics image through the ToasterPaint or LightWave3D programs and can save the blended graphics image in the Amiga’s memory or in the Toaster’s framestores. *Id.* The Toaster can take the contents of the framestores and convert the blended graphics image stored therein into analog NTSC via DAC0 and DAC1,

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respectively, as discussed with respect to [limitation [E]]. *Id.* at 000061-62. The NTSC output from DAC0 or DAC1 can be input to AMUX or BMUX, and an NTSC video signal can be input to AMUX or BMUX via a VID1 – VID4 input, and the output signals from AMUX and BMUX is fed to the A/B FADER along with an 8-bit binary control signal. *Id.* at 000062; RX-0412.00011-12, Fig. 1. The 8-bit binary control signal is an alpha channel that can be taken from one of the eight inputs on MUX D of Fig. 1. RX-0382C.000062; RX-0412.00012. “[A]ny of [the] 8 inputs to the FCMUX can be selected to govern the 256-level (8-bit) fader control value.” RX-0382C.000062. One of those inputs is RGQUAD, which are “8 bits derived from the high bits of RED and GREEN Amiga color values of four neighboring pixels (a ‘QUAD’ of pixels) on the Amiga’s display (*see* DIGBR, below).” *Id.*; RX-0412.00013. The Amiga display image may be an alpha channel image, thereby enabling alpha values derived from alpha values associated with graphics images in the LightWave 3D application to control the alpha blending on the Video Toaster. RX-0382C.62. Thus, the A/B FADER completes the blending of the blended graphics image with the video, controlled by the alpha channel or values derived therefrom. RX-0382C.62.

Resps. Br. at 286.

Broadcom argues, in part:

Respondents have not proven that the Video Toaster System (RX-0410 to RX-0414) discloses “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” as recited in Claim 1. CX-578C (Havlicek WS) at Q/A 222. This same or similar claim element is also recited in independent claims 11 and 17. For the reasons discussed above, the Video Toaster System (RX-0410 to RX-0414) does not disclose “blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.” *Id.* at Q/A 223. Therefore, under either Respondents’ or Broadcom’s claim constructions, Video Toaster System (RX-0410 to RX-0414) cannot disclose “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” *Id.* Further, the Video Toaster System is incapable of blending any graphics image with a video image.

Broadcom Br. at 143. Dr. Havlicek, Broadcom’s expert, testified as follows:

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Q222. What other element of claim 1 is not disclosed by Video Toaster System (RX-0411 through RX-0414)?

A. Video Toaster System (RX-0411 through RX-0414) does not disclose “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values,” as recited in claim 1.

Q223. Can you please explain the bases of your opinion?

A. Yes. For the reasons I provided earlier, Video Toaster System (RX-0411 through RX-0414) does not disclose “blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.” Therefore, Video Toaster System (RX-0411 through RX-0414) cannot disclose “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.”

CX-0578C (Havlicek RWS) at Q/A 222-23.

The administrative law judge previously determined that respondents have not shown that Video Toaster disclosed limitation [D]. The administrative law judge has determined that Video Toaster does not disclose “blend[ing] the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” *See* CX-0578C (Havlicek RWS) at Q/A 222-23.

Accordingly, the administrative law judge has determined that respondents have not shown that Video Toaster discloses subject matter that satisfies this limitation.

(2) Analysis of Respondents’ Argument

Respondents’ entire anticipation argument for this limitation, with respect to Video Toaster, is reproduced above. *See* Resps. Br. at 286-87.

Respondents have not clearly argued that Video Toaster satisfies limitation [F] under their proposed construction. *See id.* (“The Video Toaster System discloses [limitation [F]],

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especially if it is construed to cover a blending process other than a two-step blending process. . . .”); *see also* Resps. Reply at 97-98.

Accordingly, the administrative law judge has determined that respondents have not shown that Video Toaster discloses subject matter that satisfies this limitation.

2. Claim 11 and 17

For claims 11 and 17, respondents simply refer to their arguments for claim 1; no new evidence or argument is presented. *See* Resps. Br. at 289.

Broadcom argues that because Video Toaster does not disclose limitations [D], [E], and [F] from claim 1, it also does not anticipate claims 11 and 17. Broadcom Br. at 127.

The administrative law judge previously determined that Video Toaster does not anticipate claim 1. Based upon the reasoning presented with respect to claim 1, and the parties’ arguments that simply refer to claim 1, the administrative law judge has determined that Video Toaster does not anticipate claims 11 and 17.

3. Claim 10

Respondents argue:

Claim 10 depends from claim 1. RX-0382C.000064. As discussed for claim 1, ToasterPaint and LightWave generate a blended graphics image in RGB color space. RX-0382C.000064; RX-0413.00379. The LightWave application accepts input graphics images in a variety of formats including: framestore files saved by the Video Toaster applications (*e.g.*, Switcher or LightWave) in digital NTSC format and RGB files and brushes saved by ToasterPaint. *Id.*; RX-0382C.000064. Blending of images from these different formats necessarily requires a common format. *Id.* The Video Toaster System performs the format conversion of at least one image in order to perform the blending. *Id.*

Resps. Br. at 288.

Broadcom argues:

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In addition, Video Toaster System (RX-0410 to RX-0414) does not disclose the element of claims 10, 16, and 22, and Dr. Medoff's reliance in his answer to Question 231 on certain excerpts of Video Toaster System (RX-0410 to RX-0414) are inapposite. [CX-0578C (Havlicek WS)] at Q/A 156, 260, 261, 279, 280, 295, 296. The Video Toaster System (RX-0410 to RX-0414) does not disclose or suggest at least one processor operable to "convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format" as recited in claims 10, 16 and 22. *Id.* at Q/A 260, 261, 279, 280, 295, 296. Accordingly, the Video Toaster System does not anticipate or render obvious claims 10, 16 and 22.

Broadcom Br. at 132.

Dr. Havlicek testified as follows:

Q260. Do you have an opinion concerning whether claim 10 is anticipated by Video Toaster System (RX-0411 through RX-0414)?

A Yes. It is my opinion that claim 10 is not anticipated by Video Toaster System (RX-0411 through RX-0414).

Q261. Can you please explain why?

A Claim 10 is a dependent claim of independent claim 1. I understand that if Video Toaster System (RX-0411 through RX-0414) (RX-0087) does not anticipate or render obvious claim 1, then Video Toaster System (RX-0411 through RX-0414) also do not anticipate or render obvious claim 10. Video Toaster System (RX-0411 through RX-0414) does not anticipate or render obvious claim 10 because it does not anticipate or render obvious claim 1 for the reasons I have discussed above. In addition, Video Toaster System (RX-0411 through RX-0414) does not disclose the element of claim 10 and Dr. Medoff's reliance in his answer to Question 231 on certain excerpts of Video Toaster System (RX-0411 through RX-0414) are inapposite. Video Toaster System (RX-0411 through RX-0414) does not disclose or suggest at least one processor operable to "convert graphics data format of at least one of the plurality of graphics images prior to blending the graphics images such that the plurality of graphics images have a common graphics data format" as recited in claim 10.

CX-0578C (Havlicek RWS) at Q/A 260-61.

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The administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Video Toaster discloses subject matter that satisfies the limitations particular to claim 10. Dr. Medoff's testimony explains that "LightWave performs blending of images from these different formats, and blending inherently requires a common format."

RX-0382C (Medoff WS) at Q/A 231. While Dr. Havlicek believes the passage Dr. Medoff relies on is inapposite, he has not explained why the passage is inapposite or why Dr. Medoff is wrong. *See* CX-0578C (Havlicek RWS) at Q/A 260-61. Accordingly, if claim 1 is found anticipated, the administrative law judge would also find dependent claim 10 anticipated.

4. Claims 16 and 22

For claims 16 and 22, respondents simply refer to claims 10 and 16, respectively. Resps. Br. at 289. Broadcom does not present a separate argument for claims 16 and 22. Broadcom Br. at 132.

The administrative law judge previously determined claim 10 would be anticipated if claim 1 is found to be anticipated. Based on the parties' arguments, the administrative law judge would also find claims 16 and 22 are anticipated if claims 1 and 10 are found anticipated.

J. Obviousness – Eagle Alone

Respondents argue that "Eagle anticipates and/or renders obvious the asserted claims." Resps. Br. at 244; *see also id.* at 255 ("**Eagle, alone** or in view of Oakley (RX-0149), **renders obvious** claims 2-6, 9, 12-15, and 18-21[.]" (emphasis added)). Respondents' obviousness arguments for claim 1, however, rely on the addition of Porter & Duff. *See* Resps. Br. at 250, 253. Further, the administrative law judge previously determined that Eagle does not anticipate the asserted claims. *See* § IV(F), *supra*.

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To the extent that respondents may seek to present a single-reference obviousness argument, the administrative law judge has determined that respondents have not provided sufficient “suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000).³⁸

Accordingly, the administrative law judge has determined that respondents have not shown the asserted claims would have been obvious in light of Eagle alone.

K. Obviousness – Eagle and Porter & Duff

Respondents argue that “Compositing Digital Images” by Thomas Porter and Tom Duff (“Porter & Duff,” RX-0244) is prior art under 35 U.S.C. § 102(b) because published in July 1984. Resps. Br. at 243. Respondents introduce Porter & Duff as follows:

Porter & Duff discusses an “over” operator that blends two graphics (A and B) together using fractions F_A and F_B ; here, “1” and “ $1-\alpha_A$ ” (α_A being the alpha value for picture A). RX-0244 at 256; RX-0382C Q262; RDX-0089.0023-27. The composite pixel for those two pictures combined with the “over” operator can be computed, component-by-component, “by adding the color of the picture A times its fraction to the color of picture B times its fraction.” RX-0244 at 257; RX-0382C Q262; RDX-0089.0023-27. Foreground A is computed as “FrgdGrass over Rock over Fence over Shadow over BkgdGrass,” that is, by blending multiple

³⁸ The Federal Circuit explained that “In appropriate circumstances, a single prior art reference can render a claim obvious. . . . However, there must be a showing of a suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion. . . . This suggestion or motivation may be derived from the prior art reference itself, . . . from the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. *See Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996); *see also Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1472 (Fed. Cir. 1997) (‘[T]he suggestion to combine may come from the prior art, as filtered through the knowledge of one skilled in the art.’). Determining whether there is a suggestion or motivation to modify a prior art reference is one aspect of determining the scope and content of the prior art, a fact question subsidiary to the ultimate conclusion of obviousness.” *SIBIA Neurosciences*, 225 F.3d at 1356.

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graphics together. RX-0244 at 258; RX-0382C Q262; RDX-0089.0023-27. When blending two graphics images, A and B, with alpha values, α_A and α_B , the new blended image has a new composite alpha value α_O and Porter & Duff identifies the formula for computing this value. Each blending operation uses two alpha values, and the blending results in a blended translucent image that has a composite alpha value that has been computed from the alpha values of all of the images that have been blended and “each of the input colors is premultiplied by its alpha.” RX-0382C Q261; RX-0244 at 256; RDX-0089.0023-27. Porter & Duff states that “ C_O can be computed by averaging contributions made by C_A and C_B , so ... but the denominator is just α_O .” *Id.* The denominator referred to is given by the expression $\alpha_A F_A + \alpha_B F_B$, and as stated above the fractions for A and B are 1 and $1-\alpha_A$ for the “over” operator. *Id.* Porter & Duff discloses mathematical formulas for blending two or more translucent images with each blending operation using two alpha values resulting in a composite alpha computed from the alpha values the individual images. *Id.* Because an opaque image is an image with an alpha value of 1, Porter & Duff discloses blending a translucent image or a blended translucent image with an opaque image. *Id.*

Id. at 243-44.

1. Claim 1

Respondents’ obviousness arguments involving Eagle are limited to limitations [D] and [F]. *See* Resps. Br. at 250, 253.

- a) ***Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,***

(1) Analysis of Respondents’ Argument

Respondents argue:

In the alternative, and to the extent that Complainant argues that Eagle does not disclose [limitation [D]], Porter & Duff discloses this element. RX-0382C.00044-47 at Q172-78; RDX-0093C.0029-37. One of ordinary skill would have found it obvious to modify Eagle’s blitter and/or CPU-write based alpha blending to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to

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generate a blended graphics image. RX-0382C at Q172-78; RDX-0093C.0029-37.

As discussed above, Porter & Duff specifically discusses the “over” operator that blends two images. RX-0244 at 256-58; RX-0382C.00045 at Q175; RDX-0093C.0029-37, *supra*. Porter & Duff showed that blending two images, A and B, with respective alpha values α_A and α_B , produces a blended image has a new composite alpha value α_O for which they clearly point out the part of their formula that computes this value. *Id.* Thus, each blending operation uses two alpha values, and produces a blended translucent image having a composite alpha that has been computed from the alpha values of all of the images that have been blended and where “each of the input colors is premultiplied by its alpha.” RX-0244.00005; RX-0382C.00045 at Q175; RDX-0093C.0029-37. One of ordinary skill would have recognized that the pre-multiplied alpha blending taught by Porter & Duff represents a simpler calculation equation requiring fewer mathematical operations and that incorporating this technique into the system of Eagle would provide significant computational advantages as a predictable result of reducing the required number of calculations. RX-0244 at 256; RX-0382C.00046-47 at Q176-78; RDX-0093C.0029-37. Thus one of ordinary skill would have been motivated to incorporate the pre-multiplied alpha of Porter & Duff into Eagle to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image.

Resps. Br. at 250-51.

Broadcom argues, in part, that:

Porter & Duff (RX-0244) is a Class A reference that discloses one-step blending of graphics onto graphics, and does not teach or suggest blending of graphics with video as the word video does not appear in Porter & Duff. CX-578C (Havlicek WS), at Q/A 74, 109. Rather, Porter & Duff is concerned with blending graphics images together to make a graphics image.

Broadcom Br. at 122.

In reply, respondents argue:

Finally, even under Broadcom’s misleading “class A/class B” taxonomy, the argument that there would be no motivation to combine Eagle with Porter & Duff is unavailing. Broadcom does

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not dispute that Porter & Duff discloses blending a plurality of graphics images together using a plurality of alpha values to generate a blended graphics image. CPostHg. Br. at 121-22. Even accepting Broadcom's erroneous classification of Eagle as only "class B," it would have been obvious to a person of ordinary skill to utilize the teachings of Porter & Duff as the source of the graphics image(s) that Eagle blends with video. RPostHg. Br. at 250-54; RX-0382C at Q73-76, 172-78. Broadcom's unreasonable contention that a combination could only be obvious if the prior art provided a person of ordinary skill with schematic drawings for combining the two teachings (*see* CPostHg. Br. at 123-24) is not supported by any law and should be rejected.

Resps. Reply at 96.

The administrative law judge finds that Porter & Duff discloses blending a plurality of graphics images using a plurality of alpha values, as detailed in limitation [D]. In Q/A 109, Dr. Havlicek states that "Porter & Duff is concerned with blending graphics images together to make a graphics image." CX-0578C (Havlicek RWS) at Q/A 109. The remainder of Dr. Havlicek's answer focuses on video, avoiding the graphics question. *Id.* Further, Dr. Medoff testified that Porter & Duff discloses blending a plurality of graphics:

Q172. You mentioned earlier that Eagle (RX-0087) could also be combined with another reference to render the asserted claims of the '104 Patent obvious. What combination are you referring to?

A. Well, to the extent Broadcom contends that Eagle (RX-0087) does not disclose or render obvious "blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image" or "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values" as recited in claim 1 of the '104 Patent and equivalently recited in claims 11 and 17 under any proposed construction, it would have been obvious to a skilled artisan to combine Eagle (RX-0087) with Porter & Duff (RX-0244) to cure this alleged deficiency of Eagle (RX-0087).

RX-0382C (Medoff WS) at Q/A 172; *see also id.* at Q/A 175.

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Accordingly, the administrative law judge has determined that Porter & Duff discloses subject matter that satisfies limitation [D].

(2) Analysis of Broadcom's Argument

Respondents' entire argument is:

Dr. Medoff testified during the hearing that "[u]nder Broadcom's construction, [his] opinion is that Eagle anticipates claim 1." Tr. (Medoff) at 685:5-7. For similar reasons as under Respondents' construction, the array of "result_pixel" in Eagle, alone or modified by the disclosures of Porter & Duff, also satisfies Complaint's construction—plain and ordinary meaning—or Complainant's alternative construction—"data representing a single view of a mixture of at least two graphics images."

Resps. Br. at 251.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 121-124 (Broadcom's arguments about Porter & Duff are not specific to its constructions); Broadcom Reply, Section II(E).

Accordingly, the administrative law judge has determined that Porter & Duff discloses subject matter that satisfies limitation [D].

b) *Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.*

(1) Analysis of Respondents' Argument

Respondents argue:

To the extent that Eagle alone does not disclose this limitation, the combination of Eagle and Porter & Duff (RX-0244) renders [limitation [F]] of claim 1 of the '104 Patent obvious. As discussed above, Porter & Duff specifically discusses the "over" operator that blends two pictures (A and B) together using fractions F_A and F_B ; here, "1" and " $1-\alpha_A$ " (α_A being the alpha value for picture A). RX-0244.00005-7; RX-0382C.000044-47 (Medoff) at Q172-78, 313; RDX-0093.0068-75. Each blending operation uses two alpha values, and the blending results in a blended

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translucent image having composite alpha which has been computed from the alpha values of all of the images that have been blended and where “each of the input colors is premultiplied by its alpha.” *Id.*

Because each operation of the “over” operator would involve the use of the “ $1\alpha_A$ ” fraction in the calculation of the component-by-component blending operation, Eagle (RX-0087) in view of Porter & Duff (RX-0244) discloses this element under either construction of [limitation [F] of claim 1] of the ‘104 Patent, including “blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image.” RX-0382C.000045 (Medoff) Q175; RDX-0093C.68-75.

Resps. Br. at 253-54.

Broadcom argues that the combination of Eagle and Porter & Duff would yield a one-step blending process:

Even if one were to combine Eagle with Porter & Duff, Respondents have not shown by clear and convincing evidence that the combination would render obvious the claims of the ‘104 Patent. CX-578C (Havlicek WS), at Q/A 72, 108, 112. As explained above, the combination of a Class A reference (Porter & Duff) with a Class B reference (Eagle) does not render the ‘104 Patent claims obvious. CX-578C (Havlicek WS), at Q/A 72, 108, 112. This is because any combination of Eagle with Porter & Duff would still result in the traditional one-step process; the two-step process for blending graphics and video claimed by the ‘104 Patent would still not be present. CX-578C (Havlicek WS), at Q/A 72, 108, 112. For at least these reasons, Respondents have not proven by clear and convincing evidence that Eagle (RX-0087) in combination with Porter & Duff (CX-0244) render obvious claims 1, 10, 11, 16, 17, and 22.

Broadcom Br. at 123-24.

Respondents’ entire reply is:

Finally, even under Broadcom’s misleading “class A/class B” taxonomy, the argument that there would be no motivation to combine Eagle with Porter & Duff is unavailing. Broadcom does not dispute that Porter & Duff discloses blending a plurality of graphics images together using a plurality of alpha values to

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generate a blended graphics image. CPostHg. Br. at 121-22. Even accepting Broadcom's erroneous classification of Eagle as only "class B," it would have been obvious to a person of ordinary skill to utilize the teachings of Porter & Duff as the source of the graphics image(s) that Eagle blends with video. RPostHg. Br. at 250-54; RX-0382C at Q73-76, 172-78. Broadcom's unreasonable contention that a combination could only be obvious if the prior art provided a person of ordinary skill with schematic drawings for combining the two teachings (*see* CPostHg. Br. at 123-24) is not supported by any law and should be rejected.

Resps. Reply at 96.

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Eagle and Porter & Duff discloses a two-step process for blending a blended graphics image with a video image. *See* CX-0578C (Havlicek RWS) at Q/A 129, 132. In particular, it is not clear that a person of ordinary skill would read the combined teachings of Eagle and Porter & Duff as disclosing the claimed two-step process for blending a blended graphics image with a video image. *Id.*

(2) Analysis of Broadcom's Argument

Respondents' entire argument is:

For these reasons, Eagle, alone or modified by Porter & Duff, also satisfies Complaint's construction of plain and ordinary meaning. As discussed above, Dr. Medoff analyzed the claims under both Complainant's construction of the term. Tr. (Medoff) at 684:25:685:7.

Resps. Br. at 254.

For the same reasons provided under respondents' construction, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Eagle and Porter & Duff discloses a two-step process for blending a blended graphics image with a video image.

c) *Respondents' Rationale for the Obviousness Argument*

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Respondents argue:

One of ordinary skill would have been motivated to look for methods of alpha blending to achieve computational savings, *e.g.*, reduced processing requirements. RX-0382C.00046-47 at Q176-78; RX-0244.5; RDX-0093C.75. Eagle is in the same field of application as Porter & Duff, processing of graphics images in computing systems. One of ordinary skill looking for the computational savings as achieved by pre-multiplied alpha as taught by Porter & Duff would understand that achieving such savings is the predictable result of employing a simpler calculation equation requiring fewer mathematical operations.

Broadcom Br. at 254. In Q/A 176, Dr. Medoff testified as follows:

Q176. Would a person of ordinary skill in the art look to Porter & Duff (RX-0244)?

A. Yes. The concept and mathematics of pre-multiplied alpha, and the computational savings provided by pre-multiplied alpha, is clearly and independently taught in Porter & Duff (RX-0244). One of ordinary skill in the art who was developing software or hardware for blending of graphics and video images would be motivated to look for methods of alpha blending to achieve computational savings. By reducing the computations required to perform alpha blending, one of ordinary skill in the art would understand that performance would be increased and implementation of the alpha blending would be lower cost. The desire to reduce computation in a system such as Eagle (RX-0087)'s integrated device was a well-known issue. Porter & Duff (RX-0244) is in the same field of application as that of the Eagle (RX-0087), namely the processing of graphics and video images in computing systems. One of skill in the art, looking for the economies afforded by computational savings as achieved by pre-multiplied alpha as taught by Porter & Duff (RX-0244) would understand that achieving these savings is the predictable result of employing a simpler calculation equation that requires fewer mathematical operations. For all of these reasons it would have been obvious for one of skill in the art considering Eagle (RX-0087) to look to Porter & Duff (RX-0244) with respect to the use of premultiplied alpha and the corresponding equations.

RX-0382C (Medoff WS) at Q/A 176.

Broadcom argues:

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A POSA would not be motivated to combine Eagle (RX-0087) with Porter & Duff (RX-0244). CX-578C (Havlicek WS), at Q/A 110. In contrast to Porter & Duff (a Class A reference), Eagle is a Class B reference that teaches a system for blending graphics images with video images with one step. CX-578C (Havlicek WS), at Q/A 110. Since Porter & Duff does not teach or disclose the blending of graphics images with video images, a POSA would have no motivation to combine Porter & Duff with Eagle. *Id.* Porter & Duff (RX-02440) teaches rules for blending computer graphics images to create synthetic pictures (Section 6, lines 1-2). *Id.* A POSA would not look to Porter & Duff (creation of synthetic images) to modify Eagle, which discloses one step blending of a graphics image with a video image. *Id.* For this reason, there is no motivation to combine Porter & Duff with Eagle. *Id.*

...

The Eagle chip was a proprietary design and a POSA would have no access to that design in order to modify it. CX-578C (Havlicek WS), at Q/A 112. The full extent of the technical design details about Eagle that are disclosed in the Eagle Data Sheet (RX-0087) are reflected by the block diagrams shown in Figure 1 (page 4), Figure 2 (page 4), Figure 3 (page 5), Figure 4 (page 7), Figure 8 (page 14), and Figure 9 (page 25). *Id.* These are all functional diagrams that fail to reveal any of the technical details of the internal circuit designs of the Eagle. *Id.* Moreover, the I/O signal diagram of Figure 10 (page 28) and the timing diagrams in Figures 11-32 on pages 35-46 are useful for designing external circuits to interface to Eagle, but also fail to reveal any technical details about the internal circuit designs of Eagle. *Id.*

Therefore, it would not be possible for a POSA to modify the Eagle's blitter and/or CPU-write based alpha blending as suggested by Dr. Medoff. CX-578C (Havlicek WS), at Q/A 112. Rather, because a POSA would have to re-design the entire chip from the ground up, an endeavor that would offer no reasonable expectation of success. *Id.*

Broadcom Br. at 122-23.

The administrative law judge has also determined that respondents have not shown a person of ordinary skill in the art would have been motivated to modify Eagle, or combine Eagle and Porter & Duff, in the manner that respondents and Dr. Medoff suggest. *See* CX-0578C

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(Havlicek RWS) at Q/A 112. In particular, respondents have not shown that a person of ordinary skill would have the necessary access to modify Eagle's blitter and/or CPU-write based alpha blending. *Id.*

Accordingly, the administrative law judge has determined respondents have not shown, through clear and convincing evidence, that to a person of ordinary skill in the art, claim 1, as a whole, would have been obvious at the time of the invention based upon the disclosures and teachings of Eagle and Porter & Duff.

2. Claim 10

The administrative law judge previously determined that Eagle discloses subject matter that satisfies the particular limitations of claim 10. *See* § IV(F)(2), *supra*. Accordingly, if claim 1 is found obvious, then claim 10 is obvious for the same reasons as claim 1.

3. Claims 11, 16, 17, and 22

Respondents and Broadcom have not presented separate arguments for claims 11, 16, 17, and 22. *See* Resps. Br. at 255 (respondents simply refer to prior arguments); Broadcom Br. at 119-21 (same).

Accordingly, the administrative law judge has determined that respondents have not shown that claims 11, 16, 17, and 22 would have been obvious based upon the same rationale provided with respect to claim 1.

L. Obviousness – Eagle and Oakley or West³⁹

In general, respondents argue:

³⁹ The Joint Outline states that respondents have presented an argument applying “Eagle in view of Porter & Duff, and West or Oakley (claims 2-6, 9, 12-15, 18-21).” *See* Joint Outline at 3. Respondents’ brief, however, only addresses “Eagle, alone or in view of Oakley” and “Eagle, alone or in view of West[.]” This initial determination is limited to Eagle in view of Oakley or West.

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Eagle, alone or in view of Oakley (RX-0149), renders obvious claims 2-6, 9, 12-15, and 18-21 (the “dependent claims”). RX-0382C.000049 at Q191-203; RDX-0093C.00087-124, 00214-218. Moreover, Eagle, alone or in view of West (RX-0150) renders obvious claims 2, 4-6, 9, 12, 13, 18, and 19. RX-0382C.000049 at Q191-203; RDX-0093C.00087-124, 00214-218.

Resps. Br. at 255.

Broadcom’s entire argument follows:

Eagle (RX-0087) does not anticipate or render obvious independent claims 1, 11, or 17, and therefore, Eagle also does not anticipate or render obvious claims 2-6, 9, 12-15, and 18-21. CX-578C (Havlicek WS) at Q/A 137-153, 164-176, 183-195. In addition, Eagle does not disclose the elements of claims 2-6, 9, 12-15, and 18-21, and Dr. Medoff does not point to any evidence in Eagle showing these elements. *Id.*; RX-0382C (Medoff WS) at Q/A 192-203. Dr. Medoff relies on West (RX-0150) or Oakley (RX-0149) to show the element of claims 2-6, 9, 12-15, and 18-21. *Id.* Neither West nor Oakley, however, cures the deficiencies of Eagle discussed above. *Id.* Specifically, neither West nor Oakley discloses the claimed 2-step alpha blending recited in claim 1. *Id.* Further, Dr. Medoff does not rely on West or Oakley to cure the deficiencies in Eagle. *Id.* Thus, claims 2-6, 9, 12-15, and 18-21 are not rendered obvious by the combination of Eagle with West or Oakley. *Id.*

Broadcom Br. at 124.

Dr. Medoff provided detailed, supported testimony opining that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 191-203. Dr. Havlicek’s testimony, on the other hand, presents a conclusory opinion that Dr. Medoff’s testimony is not sufficient. *See, e.g.*, CX-0578C (Havlicek RWS) at Q/A 137-153, 164-176, 183-195. For instance, Dr. Havlicek does not address any of the pinpoint citations provided in Dr. Medoff’s witness statement, and much of his testimony simply refers back to his analysis of claim 1. *Id.*

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The administrative law judge finds that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. The administrative law judge also finds that a person of ordinary skill in the art would have modified Eagle with the teachings of Oakley or West as part of a *routine engineering and product development* effort associated with improving the processing and scaling video signals in television applications. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 203 (“POSITA would have looked to use such filters to enable more variability in sample rate modification, increasing the uses for the Eagle (RX-0087) integrated circuit”).⁴⁰

⁴⁰ In Q/A 203, Dr. Medoff explained: “At the priority date of the ’104 Patent, sample rate conversion was a problem that had been long been identified, understood, and solved in many fields including signal processing for television. For example, for U.S. Patent No. 4,472,732, engineers at Ampex, one of the early pioneers in digital television, developed sample rate conversion techniques for horizontal and vertical scaling of images as early as 1981. Mathematics and implementation methods for polyphase filtering were broadly developed in the 1980’s and 1990’s and applied to television signal processing. These methods were driven by the need to alter the sampling rates and perform low-pass (anti-flutter) filtering of digital television images, which in turn stemmed from the variety of different formats in which video data might be found (*e.g.*, U.S. versus European video standards), the need to display graphic images on interlaced television displays, and the desire to implement vertical and horizontal scaling to change the size of an image before display.

One of skill would have been motivated to modify Eagle (RX-0087)’s low-pass filter to use the polyphase filter disclosed in Oakley (RX-0149) and/or West (RX-0150). Eagle (RX-0087)’s integrated device discloses the use of filters for performing scaling and anti-fluttering functionality. As stated in the Abstract of Oakley (RX-0149), Oakley (RX-0149) is directed to a scaler in an integrated circuit for displaying component video on a television display. A POSITA would logically look to methods of processing and scaling video signals for projection on television displays in designing an integrated circuit for use in consumer electronics products. Likewise, as stated in West (RX-0150)’s Abstract, West (RX-0150) is directed to an “image scaling circuit for increasing or decreasing the size of a sampled image to match a fixed resolution display” and may “resiz[e] the image in the horizontal and vertical dimension.” Modifying Eagle (RX-0087) to use a polyphase filter would be applying a known technique in a known device to yield predictable results. By employing a polyphase filter, Eagle (RX-0087)’s integrated circuit could achieve scaling and anti-flutter without the need for additional filters. This reduces the complexity of the device and provides more flexibility. As polyphase filtering was well-known, a POSITA would have looked to use such filters to enable more variability in sample rate modification, increasing the uses for the Eagle (RX-0087) integrated circuit.”

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Accordingly, if it is found that claim 1 would have been obvious, the administrative law judge also finds claims 2-6, 9, 12-15, and 18-21 would have been obvious over Eagle in view of Oakley or West.

M. Obviousness – Gloudemans Alone

Respondents argue that “*Gloudemans (RX-0073), alone* or in view of Porter & Duff (RX-0244), Oakley (RX-0149), and/or West (RX-0150), also discloses claims 1-6 and 9-22 of the ‘104 Patent.” Resps. Br. at 257 (emphasis added). Respondents’ obviousness arguments for claim 1, however, rely on the addition of Porter & Duff. *See* Resps. Br. at 262, 264. Further, the administrative law judge previously determined that Gloudemans does not anticipate the asserted claims. *See* § IV(G), *supra*.

To the extent that respondents may seek to present a single-reference obviousness argument, the administrative law judge has determined that respondents have not provided sufficient “suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000).

Accordingly, the administrative law judge has determined that respondents have not shown the asserted claims would have been obvious in light of Gloudemans alone.

N. Obviousness – Gloudemans and Porter & Duff

1. Claim 1

Respondents present obviousness arguments in their discussion of limitations [D] and [F]. *See* Resps. Br. at 261-62, 264-65.

- a) *Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,*

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(1) Analysis of Respondents' Argument

Respondents argue:

Combination with Porter & Duff: To the extent that Broadcom argues that Gloudemans does not disclose blending a plurality of graphics images, Porter & Duff (RX-0244) discloses this element. RX-0382C Q260-63; RDX-0089.0017, 0023-27; *see also* Section V.I.E.1.a. One of ordinary skill would have found it obvious to modify Gloudemans' keyer 98 to blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image. RX-0382C Q260-63; RDX-0089.0017, 0023-27.

Gloudemans explains that computers 94 and 96 "work together" to create the graphic images and alpha signals, and delays the video to account for the processing done by computer 94 and 96. RX-0073 at 7:38-41, 45-49; RX-0382C Q262; RDX-0089.0023-27. Blending images together first before blending that blended image with video reduces further delay because only the blended image would need to be blended with the video, rather than individually blending multiple graphics with the video in succession. *Id.* For example, during a live event, such as a football game, some images may be relatively static compared to video images, so blending the static images before blending with video would also preserve processing and memory resources and allow better overall control over the final result by performing only a single blend with the video. *Id.*

Gloudemans is in the same field as Porter & Duff (RX-0244): processing graphics images in computing systems. RX-0382C Q262. One of ordinary skill would have recognized the computational savings achieved by the pre-multiplied alpha taught by Porter & Duff and would also understand achieving such savings is the predictable result of employing a simpler calculation that requires fewer mathematical operations. *Id.*; RX-0244 at 256; RDX-0089.23-27. One of ordinary skill would have found it obvious to modify keyer 98 to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image, as in Porter & Duff. *Id.*

Resps. Br. at 261-62.

Broadcom's entire argument that the claims would not have been obvious follows:

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Gloudemans (RX-0073) in view of Porter & Duff (RX-0244) also do not render obvious claim 1 because, like Gloudemans, Porter & Duff does not disclose the claimed two-step process for blending graphics and video. CX-578C (Havlicek WS), at Q/A 297-337. There is no motivation to combine Gloudemans with Porter & Duff because Gloudemans teaches away from performing step-one of the claimed two-step alpha blending process. *Id.* Further, even if one were to make the combination, the combination of Gloudemans and Porter & Duff does not disclose or suggest all of the claim elements. *Id.*

Porter & Duff is a Class A reference does not teach or suggest the blending of graphics with video; indeed, the word video does not appear in Porter & Duff. *Id.* at Q/A 310. Thus, for the same reasons as discussed above with respect to the improper combination of Eagle and Porter & Duff, there is no motivation to combine Gloudemans with Porter & Duff. *Id.* at Q/A 310, 311; RX-0244 pp. 257-259.

Further, there is no motivation to combine Gloudemans with Porter & Duff because, as discussed above, Gloudemans teaches away from blending graphics with graphics to generate a blended graphics image, and, Gloudemans also teaches away from “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.” *Id.* at Q/A 330. Even if one were to combine Gloudemans with Porter & Duff, Respondents have not presented clear and convincing evidence that the combination would render obvious the claims of the ‘104 Patent. As explained above, the combination of a Class A reference (Porter & Duff) with a Class B reference (Gloudemans) does not render the ‘104 Patent claims obvious. This is because any combination of Gloudemans with Porter & Duff would still result in the traditional one-step process; the two-step process for blending graphics and video claimed by the ‘104 Patent would still not be present. *Id.* at Q/A 79, 328, 329.

Broadcom Br. at 140-41.

The administrative law judge previously determined that Porter & Duff discloses subject matter that satisfies limitation [D]. *See* § IV(K)(1)(a), *supra*. Broadcom’s argument with respect to Gloudemans does not alter that conclusion.

(2) Analysis of Broadcom’s Argument

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The administrative law judge previously determined that Porter & Duff discloses subject matter that satisfies limitation [D] under Broadcom's construction. *See* § IV(K)(1)(a), *supra*.

Broadcom's argument with respect to Gloudemans does not alter that conclusion.

b) Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.

(1) Analysis of Respondents' Argument

Respondents argue:

"Two-step:" To the extent element 1[e] is construed to as a two-step blending process in which all graphics images are blended together before they are blended with video consistent with Respondents' construction, Gloudemans renders this limitation obvious. RDX-0382C Q267; RX-0073 at 7:38-65; RDX-0089.0044-45. Dr. Medoff explained that there are numerous operations to blend graphics with video, including 1) serially blending each graphic with video and 2) the "two-step" process of blending all graphics first before blending the result with video. RDX-0382C Q267. To the extent Gloudemans does not disclose the latter, one of ordinary skill would have been motivated to adopt it because it simplifies the blending of graphics and video and is merely a matter of design choice. RDX-0382C Q267; RX-0073 at 7:38-65; RDX-0089.0044-45.

Respondents' Construction: Respondents' construction—"blend the blended graphics image with the video image using an alpha value derived from the product of one minus the alpha value for every graphics image"—incorporates the second part of the formula in the '104 Patent (*i.e.*, $AR(i) = AR(i-1) * (1 - A(i))$), is consistent with Broadcom's position in the *SiRF* litigation, and is consistent with the proper meaning that one of ordinary skill would give to this term. RX-0382C Q265; JX-0003 at 45:50-57; RX-0313.00017-19; *see also supra* Section VI.B.2.

Under this construction, Gloudemans in view of Porter & Duff (RX-0244) renders obvious limitation 1[e]. Porter & Duff discusses the "over" operator that blends two pictures (A and B) together using fractions F_A and F_B ; here, "1" and " $1 - \alpha_A$ " (α_A being the alpha value for picture A). RX-0244 at 256-58; RX-0382C Q269; RDX-0089.0052-54. Each blending operation uses two alpha values, and the blending results in a blended

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translucent image having a composite alpha that has been computed from the alpha values of all images that have been blended and where “each of the input colors is premultiplied by its alpha.” *Id.* and Section VI.E.1.a. Because each use of the “over” operator uses the “ $1-\alpha A$ ” fraction in the calculation of the component-by-component blending operation, Gloudemans in view of Porter & Duff discloses this element under Respondents’ construction. *Id.*

Resps. Br. at 264-65.

Broadcom has argued that “Gloudemans (RX-0073) in view of Porter & Duff (RX-0244) also do not render obvious claim 1 because, like Gloudemans, Porter & Duff does not disclose the claimed two-step process for blending graphics and video.” Broadcom Br. at 140 (citing CX-0578C (Havlicek WS) at Q/A 297-337).

(a) *Two-Step Process*

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Gloudemans and Porter & Duff (in combination) discloses a two-step process for blending a blended graphics image with a video image. *See* CX-0578C (Havlicek RWS) at Q/A 300-04. In particular, at Q/A 267, Dr. Medoff cites Gloudemans at 7:38-65 as “discussing computers 94 and 96 working together to generate graphics” and then concludes that Gloudemans discloses the two-step process required by the limitation. Dr. Medoff, however, does not fully explain how the cited portion of Gloudemans is applicable, nor does he provide any further support for his conclusion. Dr. Havlicek, on the other hand, explained that the cited portion of Gloudemans relates to foreground and background images, not combined graphics images. *See* CX-0578C (Havlicek WS) at Q/A 304.

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(b) The Blending Formula

Having considered the parties' arguments, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Porter & Duff discloses the formula corresponding to respondents' construction, "using an alpha value derived from the product of one minus the alpha value for every graphics image." Dr. Medoff testified that Porter & Duff, at 256-57, discusses the over operator, using multiple alpha values (*e.g.*, α_A and α_B), and the denominator ($\alpha_A F_A + \alpha_B F_B$) in opining that:

Porter and Duff (RX-0244) has thereby introduced the concepts and provided explicit mathematical formulas for blending two or more translucent images, where each blending operation uses two alpha values, and where the blending results in a blended translucent image having composite alpha which has been computed from the alpha values of all of the images that have been blended.

RX-0382C (Medoff WS) at Q/A 269. Dr. Havlicek's testimony does not refute Dr. Medoff's testimony about the formula. *See* CX-0578C (Havlicek) at Q/A 310. Accordingly, the administrative law judge finds that Porter & Duff discloses the aspect of limitation [F] that entails blending a graphics image with a video image "using an alpha value derived from the product of one minus the alpha value for every graphics image."

(2) Analysis of Broadcom's Argument

The administrative law judge previously determined that Gloudemans, under Broadcom's constructions, discloses subject matter that satisfies this limitation. Nothing in Broadcom's obviousness arguments upsets that conclusion. Broadcom's claim construction arguments for the relevant claim limitation were not, however, those adopted herein.

c) Respondents' Rationale for the Obviousness Argument

For the combination of Gloudemans and Porter & Duff, respondents have argued:

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Gloude-mans is in the same field as Porter & Duff (RX-0244): processing graphics images in computing systems. RX-0382C Q262. One of ordinary skill would have recognized the computational savings achieved by the pre-multiplied alpha taught by Porter & Duff and would also understand achieving such savings is the predictable result of employing a simpler calculation that requires fewer mathematical operations. *Id.*; RX-0244 at 256; RDX-0089.23-27. One of ordinary skill would have found it obvious to modify keyer 98 to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image, as in Porter & Duff. *Id.*

Resps. Br. at 262. In Q/A 262, Dr. Medoff testified:

Q262. You stated that it would have been obvious to combine Gloude-mans (RX-0073) with Porter & Duff (RX-0244). Can you explain why you believe it would have been obvious?

A. In my opinion, one of skill in the art who was developing software or hardware for blending of graphics and video images at the time of filing of the '104 Patent would have been motivated to look for methods of alpha blending to achieve computational savings. By reducing the computations required to perform alpha blending, as in Porter & Duff (RX-0244), one of skill in the art would understand that performance would be increased and implementation of the alpha blending would be lower cost. The need to reduce computation in the system architecture of Gloude-mans (RX-0073) was a well-known problem. Gloude-mans (RX-0073) is also in the same field of application as that of Porter & Duff (RX-0244) – namely the processing of graphics and video images in computing systems. One of skill in the art looking for the economics afforded by computational savings as achieved by pre-multiplied alpha as taught by Porter & Duff (RX-0244) would understand that achieving these savings is the predictable result of employing a simpler calculation equation that requires fewer mathematical operations.

Moreover, 7:38-41 explains that computers 94 and 96 “work together” to create the graphic image and alpha signals, and 7:45-49 explains that the video is delayed to account for the processing done by computer 94 and 96). In my opinion, blending images together first before blending that blended image with video reduces any delay in the display of the video because only the blended image would need to be blended with the video, rather than individually blending multiple graphics with the video in

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succession. For example, during a televised sports match, such as the football game example discussed throughout Gloudemans (RX-0073), certain images are relatively static compared to video images, such as the score or location of a first down line. Consequently, those graphics images may not need to be re-blended with one another each time a new video image is ready for compositing. Blending the graphics first would also preserve processing and memory resources and allow better overall control over the final result by allowing a single blend with the video. These were common design goals in graphics processing systems at the time of filing of the '104 Patent.

For all of these reasons, it would have been obvious one of skill in the art to look to Porter & Duff (RX-0244) and to modify Gloudemans' keyer 98 to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image, to the extent Gloudemans (RX-0073) does not already disclose blending a plurality of graphics using a plurality of alpha values associated with the graphics images.

RX-0382C (Medoff WS) at Q/A 262.

Broadcom argues:

[T]here is no motivation to combine Gloudemans with Porter & Duff because, as discussed above, Gloudemans teaches away from blending graphics with graphics to generate a blended graphics image, and, Gloudemans also teaches away from "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values." *Id.* at Q/A 330. Even if one were to combine Gloudemans with Porter & Duff, Respondents have not presented clear and convincing evidence that the combination would render obvious the claims of the '104 Patent. As explained above, the combination of a Class A reference (Porter & Duff) with a Class B reference (Gloudemans) does not render the '104 Patent claims obvious. This is because any combination of Gloudemans with Porter & Duff would still result in the traditional one-step process; the two-step process for blending graphics and video claimed by the '104 Patent would still not be present. *Id.* at Q/A 79, 328, 329.

Broadcom Br. at 140-41.

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Having considered the parties' arguments, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that one of ordinary skill in the art would have been motivated to improve Gloudemans by reducing the computations required to blend images, and that Porter & Duff provides such a solution. RX-0382C (Medoff WS) at Q/A 262. Broadcom's argument that Gloudemans teaches away from blending graphics relies on an unduly rigid view of obviousness, especially where Gloudemans and Porter & Duff are in the same field of art. *Id.* ("Gloudemans (RX-0073) is also in the same field of application as that of Porter & Duff (RX-0244) – namely the processing of graphics and video images in computing systems."); *see KSR*, 550 U.S. at 420-21 ("familiar items may have obvious uses beyond their primary purposes . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton."). Further, Gloudemans does not sufficiently discourage blending graphics based on pixel-location exclusions, as Dr. Havlicek contends, because it does not suggest that further development is unlikely to be productive. *See Arctic Cat Inc. v. Bombardier Recreational Prod. Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) ("The degree of teaching away will of course depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant."); *see also* RX-0382C (Medoff WS) at Q/A 359-61 (opining that Gloudemans does not teach away). Accordingly, the administrative law judge has determined that a person of ordinary skill in the art would have been motivated to modify Gloudemans in view of Porter & Duff. The administrative law judge has also determined that Gloudemans does not teach away from a combination or modification pertaining to the limitations of claim 1.

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In conclusion, the administrative law judge has determined that claim 1 would have been obvious based on Gloudemans and Porter & Duff under Broadcom's constructions. However, the administrative law judge ultimately finds that claim 1 would not have been obvious under respondents' constructions, which were adopted.

2. Claim 10

The administrative law judge previously determined that Gloudemans discloses subject matter that satisfies claim 10. *See* § IV(G)(3), *supra*. Accordingly, if claim 1 is found obvious, then claim 10 is obvious for the same reasons as claim 1.

3. Claims 11, 16, 17, and 22

Respondents and Broadcom have not presented separate arguments for claims 11, 16, 17, and 22. *See* Resps. Br. at 265-66 (respondents simply refer to prior arguments); Broadcom Br. at 139-40 (same).

Accordingly, the administrative law judge has determined that respondents have not shown that claims 11, 16, 17, and 22 would have been obvious based upon the same rationale provided with respect to claim 1.

O. Obviousness – Gloudemans, Porter & Duff, and West or Oakley

Respondents argue:

Gloudemans (RX-0073), alone or in combination with Porter & Duff (RX-0244), and Oakley (RX-0149), renders obvious claims 2-6, 9, 12-15, and 18-21. RX-0382C Q191-203, 282-87; RDX-0089.0061-93, 0100-02, 0104-06. And Gloudemans, alone or in view of Porter & Duff, and West (RX-0150) renders obvious claims 2, 4-6, 9, 12, 13, 18, and 19. *Id.* Claims 2-6, 9, 12-15, and 18-21 recite additional features, including a polyphase filter (claims 2 and 13), using a polyphase filter to vertically and/or horizontally scale images (claims 4, 5, 9, 12-14, 19), a programmable polyphase filter (claims 6, 9, 13, 19), and antialiasing filtering (claims 3, 14, 15, 20, and 21) using a polyphase filter (claim 3). RX-0382C Q191-92. Broadcom does not dispute that

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Oakley and West disclose these elements. CX-0578C (Havlicek) Q338-56, 362-73, 378-89; *see also supra* Section VI.E.1.a.

For claims 2-6, 9, 12-15, and 18-21, one of ordinary skill would have been motivated to modify Gloudemans to use the polyphase filter disclosed in Oakley. For claims 2, 4-6, 9, 12, 13, 18, and 19, one of ordinary skill would have been motivated to modify Gloudemans to use the polyphase filter disclosed in West (RX-0150). RX-0382C Q191-203, 282-87; RDX-0089.61-93, 0100-02, 0104-06. Oakley is directed to a scaler in an integrated circuit for displaying component video on a television display. RX-0149 at Abstract; RX-0382C Q287; RDX-0089.64-65. One of ordinary skill would logically look to methods of processing and scaling video signals for projection on television displays in designing an integrated circuit for use in consumer electronics products. West is directed to an “image scaling circuit for increasing or decreasing the size of a sampled image to match a fixed resolution display” and “resiz[ing] the image in the horizontal and vertical dimension.” RX-0150 at Abstract; RX-0382C Q287; RDX-0089.64-65.

Modifying Gloudemans to use the polyphase filters in Oakley and West would be applying a known technique in a known device to yield predictable results, would enable scaling and anti-fluttering (in the case of Oakley) without the need for additional filters, would reduce the complexity of the device, and would provide more flexibility. RX-0382C Q287; RDX-0089.0064-65. As polyphase filtering was well-known, one of ordinary skill would have looked to use such filters to enable more variability in sample rate modification. *Id.*

Resps. Br. at 266-67.

Broadcom argues:

Gloudemans (RX-0073) does not anticipate or render obvious independent claims 1, 11, or 17, and therefore, Gloudemans (RX-0073) also does not anticipate or render obvious claims 2-6, 9, 12-15, and 18-21. CX-578C (Havlicek WS) at Q/A 339-55, 363-91. In addition, Gloudemans (RX-0073) does not disclose the elements of claims 2-6, 9, 12-15, and 18-21, and Dr. Medoff does not point to any evidence in Gloudemans (RX-0073) showing these elements. *Id.*; RX-0382C (Medoff WS) at Q/A 282-87. Dr. Medoff relies on West (RX-0150) or Oakley (RX-0149) to show the element of claims 2-6, 9, 12-15, and 18-21. *Id.* Neither West nor Oakley, however, cures the deficiencies of Gloudemans

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(RX-0073) discussed above. *Id.* Specifically, neither West nor Oakley discloses the claimed 2-step alpha blending recited in claim 1. *Id.* Further, Dr. Medoff does not rely on West or Oakley to cure the deficiencies in Gloudemans (RX-0073). *Id.* Thus, claims 2-6, 9, 12-15, and 18-21, are not rendered obvious by the combination of Gloudemans (RX-0073) with West or Oakley. *Id.*

Broadcom Br. at 141.

Having considered the parties arguments, if claim 1 is found obvious, the administrative law judge would find that claims 2-6, 9, 12-15, and 18-21 would have been obvious based on the teachings of Gloudemans and Porter & Duff, further in view of West and Oakley. *See* RX-0382C (Medoff WS) at Q/A 191-203, 282-87. Dr. Medoff provided detailed, supported testimony opining that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. *See, e.g.,* RX-0382C (Medoff WS) at Q/A 191-203 (introducing West and Oakley), 282-87 (providing testimony with regard to Gloudemans, West, and Oakley). Dr. Havlicek's testimony, on the other hand, presents conclusory opinions that Dr. Medoff's testimony is not sufficient. *See, e.g.,* CX-0578C (Havlicek RWS) at Q/A 339-55, 363-91. For instance, Dr. Havlicek does not address any of the pinpoint citations provided in Dr. Medoff's witness statement. *Id.*

The administrative law judge finds that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. The administrative law judge also finds that a person of ordinary skill in the art would have modified Gloudemans and Porter & Duff with the teachings of Oakley or West as part of a *routine engineering and product development* effort associated with improving the processing and scaling video signals in television applications. *See, e.g.,* RX-0382C (Medoff WS) at Q/A 203, 287 ("A POSITA would logically look to methods of processing and scaling

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video signals for projection on television displays in designing an integrated circuit for use in consumer electronics products.”).

Accordingly, if it is found that claim 1 would have been obvious, the administrative law judge also finds claims 2-6, 9, 12-15, and 18-21 would have been obvious over Gloudemans and Porter & Duff in view of Oakley or West.

P. Obviousness – Myhrvold Alone

Respondents argue that “*Myhrvold, alone* or in view of Porter & Duff (RX-0244), Oakley (RX-0149), and/or West (RX-0150), also discloses claims 1-6 and 9-22.” Resps. Br. at 267 (emphasis added). Respondents’ obviousness arguments for claim 1, however, rely on the addition of Porter & Duff. *See* Resps. Br. at 272, 274. Further, the administrative law judge previously determined that Myhrvold does not anticipate the asserted claims. *See* § IV(H), *supra*.

To the extent that respondents may seek to present a single-reference obviousness argument, the administrative law judge has determined that respondents have not provided sufficient “suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000).

Accordingly, the administrative law judge has determined that respondents have not shown the asserted claims would have been obvious in light of Myhrvold alone.

Q. Obviousness – Myhrvold and Porter & Duff

1. Claim 1

Respondents present obviousness arguments in their discussion of limitations [D] and [F]. *See* Resps. Br. at 271-72, 274-76.

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Broadcom's entire non-obviousness argument is:

Myhrvold (RX-0083) in view of Porter & Duff (RX-0244) does not render obvious Claim 1 because, like Myhrvold, Porter & Duff does not disclose the claimed two-step process for blending graphics and video. CX-578C (Havlicek WS), at Q/A 399-414. There is no motivation to combine Myhrvold with Porter & Duff, and that even if one were to make the combination, the combination of Myhrvold and Porter & Duff does not disclose or suggest all of the claim elements. *Id.*

A POSA would not be motivated to combine Myhrvold (RX-0083) with Porter & Duff (RX-0244). Both Porter & Duff and Myhrvold are Class A references that teach blending of graphics images (gsprites in the case of Myhrvold) together in one-step blending. *Id.* Since Porter & Duff does not teach or disclose the blending of graphics images with video images, and it certainly does not disclose blending a gsprite with video, a POSA would have no motivation to combine Porter & Duff with Myhrvold. *Id.* Porter & Duff (RX-02440) teach rules for blending computer graphics images to create synthetic pictures (Section 6, lines 1-2). *Id.* at Q/A 413. A POSA would not look to Porter & Duff (creation of synthetic images) to enhance the combining of gsprites disclosed in Myhrvold. *Id.* For this reason, there is no motivation to combine Porter & Duff with Myhrvold. *Id.*

Combining Myhrvold with Porter & Duff would only result in the traditional one-step process for blending graphics image with a graphics image (or gsprite for Myhrvold); the two-step process for blending graphics and video claimed by the '104 Patent would still not be present since neither references discloses how to blend a gsprite with video. *Id.* at Q/A 412.

Broadcom Br. at 144.

- a) ***Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,***

Respondents argue, in part:

To the extent that Broadcom newly argues that Myhrvold does not disclose blending a plurality of images because it allegedly blends gsprites ("graphics images") in a different order than the '104 Patent, Porter & Duff (RX-0244) bolsters the teachings of

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Myhrvold by explaining that the result of blending graphics images is the same no matter whether the images are blended from front-to-back or back-to-front. RX-0382C (Medoff) Q302-04, 315; RDX-0090.0013-40; *see also* RX-0244 at 256. One of ordinary skill would have found it obvious to modify Myhrvold's compositing buffer 210 to enable blending of a plurality of graphics images in any order (as taught by Porter & Duff) using a plurality of alpha values associated with the graphics images to generate a blended graphics image. RX-0382C Q302-04; RDX-0090.0013-40; RX-0244 at 256.

Myhrvold (RX-0083) is in the same field as Porter & Duff (RX-0244): processing of graphics and video images in computing systems. RX-0382C Q304. Myhrvold is also already configured for blending images in a particular order. *Id.*; RX-0083 at 15:30-35. One of ordinary skill would have recognized that blending graphics images is the same no matter whether the images are blended from front-to-back or back-to-front. RX-0382C (Medoff) Q304, 315; *see also* RX-0244 at 256. Thus, one of ordinary skill would have found it obvious to look to Porter & Duff and to modify Myhrvold's compositing buffer 210 to enable blending of a plurality of graphics images in any order using a plurality of alpha values associated with the graphics images to generate a blended graphics image. *Id.*

Resps. Br. at 272.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 142, 144 (contesting limitations [E] and [F] only); Broadcom Reply, Section II(E).

The administrative law judge previously determined that Myhrvold discloses a processor that can blend a plurality of graphics images using a plurality of alpha values, as described in claim 1. *See, e.g.,* RX-0382C (Medoff WS) at Q/A 301 (and the evidence cited in the answer, including RX-0083 at 7:58-62); *see* § IV(H)(1)(d), *supra*. The administrative law judge previously determined that Porter & Duff discloses subject matter that satisfies limitation [D]. *See* § IV(K)(1)(a), *supra*. Nothing in respondents' or Broadcom's obviousness arguments upsets those conclusions.

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- b) *Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.*

Respondents argue:

Under this construction, Myhrvold in view of Porter & Duff renders element 1[e] obvious. Myhrvold includes equations for compositing, including when gsprites are sorted in front-to-back order (alpha value for each pixel is $A_{new}=A_{old}-(A_{old} * A_{in})$; color is $C_{new}=C_{old}+(C_{in} * (A_{old} * A_{in}))$) and when gsprites are sorted in back-to-front order (alpha value for each pixel is $A_{new}=A_{in}+((1-A_{in}) * A_{old})$; color is $C_{new}=(C_{in} * A_{in})+((1-A_{in}) * C_{old})$). RX-0382C Q309; RX-0083 at 71:29-72:35; RDX-0090.0044-66. Using “Aold” to calculate “Anew” requires computing and maintaining alpha values for each subsample. RX-0083 at 71:29-72:35; RX-0382C Q311. That yields a composite alpha value similar to that in the ‘104 Patent. RX-0382C Q309; RX-0083 at 71:29-72:35. Compare JX-0003 at 45:50-57, 46:6-17 ($AR(i) = AR(i-1) * (1-A(i))$) with RX-0083 at 62:30-36 ($Alpha(new)=Alpha(dst) * (1 - Alpha(src))$). The formula in Myhrvold meets element 1[e]. RX-0382C Q309, 311.

In the alternative, and as explained in Section VI.E.1.a, Porter & Duff specifically discusses the “over” operator that blends two pictures (A and B) together using fractions F_A and F_B ; here, “1” and “ $1-\alpha_A$ ” (α_A being the alpha value for picture A). . . .

Resps. Br. at 274-75.

Broadcom argues, in part:

. . . Myhrvold (RX-0083) only discloses how to blend gsprites together in a one-step process, and Myhrvold does not disclose how to blend gsprites with video images. *Id.* at Q/A 407 (citing RX-0073 at 7:58-62, 27:7-11, 62:30-36). . . .

Broadcom Br. at 143.

The administrative law judge previously determined that respondents have not shown, through clear and convincing evidence, that Myhrvold discloses a processor that blends a blended graphics image with video (under either party’s constructions). Porter & Duff does not cure this deficiency. See CX-0578C (Havlicek RWS) at Q/A 405-410, 412. Further,

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respondents have not shown that Myhrvold and Porter & Duff disclose a two-step process for blending graphics. *Id.* Accordingly, the administrative law judge has determined that limitation [F] would not have been obvious based on the teaching of Myhrvold and Porter & Duff.

c) Respondents' Rationale for the Obviousness Argument

Respondents argue:

Myhrvold is in the same field as Porter & Duff: processing of graphics and video images in computing systems. RX-0382C Q314. One of ordinary skill would have been motivated to look for methods of alpha blending to achieve computational savings, *e.g.*, reduced processing requirements, and would recognize such savings from pre-multiplied alpha as taught by Porter & Duff as the predictable result of a simpler equation with fewer operations. *Id.*; RX-0244 at 256.

Resps. Br. at 275-76.

Broadcom argues, in part, that a person of skill would not combine the references as “Porter & Duff does not teach or disclose the blending of graphics images with video images, and it certainly does not disclose blending a gsprite with video, a POSA would have no motivation to combine Porter & Duff with Myhrvold.” Broadcom Br. at 144.

The administrative law judge has determined that a person of ordinary skill would not combine Myhrvold with Porter & Duff. *See* CX-0578C (Havlicek WS) at Q/A 413. Respondents have not shown that a person of ordinary skill would look to a reference that teaches the creation of synthetic images (Porter & Duff) to enhance the combining of gsprites (Myhrvold). *Id.*

2. Claim 10

The administrative law judge previously determined that Myhrvold discloses subject matter that satisfies claim 10. *See* § IV(H)(3), *supra*. Accordingly, if claim 1 is found obvious, then claim 10 is obvious for the same reasons as claim 1.

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3. Claims 11, 16, 17, and 22

Respondents and Broadcom have not presented separate arguments for claims 11, 16, 17, and 22. *See* Resps. Br. at 276-77 (respondents simply refer to prior arguments); Broadcom Br. at 142-44 (same).

Accordingly, the administrative law judge has determined that respondents have not shown that claims 11, 16, 17, and 22 would have been obvious based upon the same rationale provided with respect to claim 1.

R. Obviousness – Myhrvold, Porter & Duff, and West or Oakley

Respondents argue:

With respect to claims 2-6, 9, 12-15, 18, and 19, one of ordinary skill would have been motivated to modify Myhrvold to use the polyphase filter disclosed in Oakley. As to claims 2, 4-6, 9, 12, 13, 18, and 19, one of ordinary skill would have been motivated to modify Myhrvold to use the polyphase filter disclosed in West. RX-0382C Q191-203, 326-31; RDX-0090.0066-99, .0105-07, .0109, .0110. Oakley is directed to a scaler in an integrated circuit for displaying component video on a television display. RX-0149 at Abstract; RX-0382C Q327, 331; RDX-0090.0070. One of ordinary skill would look to methods of processing and scaling video signals for television displays in designing an integrated circuit for use in consumer electronics products. West is directed to an “image scaling circuit for increasing or decreasing the size of a sampled image to match a fixed resolution display” and “resiz[ing] the image in the horizontal and vertical dimension.” RX-0150 at Abstract; RX-0382C Q327, 331; RDX-0090.0071.

Modifying Myhrvold to use the polyphase filters in Oakley and West would be applying a known technique in a known device to yield predictable results, would enable scaling and anti-fluttering (in the case of Oakley) without the need for additional filters, would reduce complexity of the device, and would provide more flexibility. RX-0382C Q327, 331; RDX-0090.0070. As polyphase filtering was well-known, one of ordinary skill would have looked to use such filters to enable more variability in sample rate modification. *Id.*

Resps. Br. at 277-78.

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Broadcom argues:

Myhrvold (RX-0083) does not anticipate or render obvious independent claims 1, 11, or 17, and therefore, Myhrvold (RX-0083) also does not anticipate or render obvious claims 2-6, 9, 12-15, and 18-21. CX-578C (Havlicek WS) at Q/A 421-39, 445-56, 461-72. In addition, Myhrvold does not disclose the elements of claims 2-6, 9, 12-15, and 18-21, and Dr. Medoff does not point to any evidence in Myhrvold showing these elements. *Id.*; RX-0382C (Medoff WS) at Q/A 326-31. Dr. Medoff relies on West (RX-0150) or Oakley (RX-0149) to show the element of claims 2-6, 9, 12-15, and 18-21. *Id.* Neither West nor Oakley, however, cures the deficiencies of Myhrvold discussed above. *Id.* Specifically, neither West nor Oakley discloses the claimed 2-step alpha blending recited in claim 1. *Id.* Further, Dr. Medoff does not rely on West or Oakley to cure the deficiencies in Myhrvold. *Id.* Thus, claims 2-6, 9, 12-15, and 18-21, are not rendered obvious by the combination of Myhrvold with West or Oakley. *Id.*

Broadcom Br. at 145.

The administrative law judge finds that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. *See* RX-0382C (Medoff WS) at Q/A 191-203, 326-31. The administrative law judge also finds that a person of ordinary skill in the art would have modified Myhrvold and Porter & Duff with the teachings of Oakley or West as part of a *routine engineering and product development effort* associated with improving the processing and scaling video signals in television applications. *See* RX-0382C (Medoff WS) at Q/A 327-31 (“A POSITA would logically look to methods of processing and scaling video signals for projection on television displays in designing an integrated circuit for use in consumer electronics products.”).

Accordingly, if it is found that claim 1 would have been obvious, the administrative law judge also finds that claims 2-6, 9, 12-15, and 18-21 would have been obvious based on the teachings and disclosures of Myhrvold and Porter & Duff in view of Oakley and West.

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S. Obviousness – Video Toaster Alone

Respondents argue that “Video Toaster anticipates and/or renders obvious the asserted claims.” Resps. Br. at 278; *see also id.* at 289 (“Claims 2-6, 9, 12-15, and 18-21 are invalid in view of Video Toaster.”). Respondents’ obviousness arguments for claim 1, however, rely on the addition of Porter & Duff. *See* Resps. Br. at 284-85, 286-87. Further, the administrative law judge previously determined that Video Toaster does not anticipate the asserted claims. *See* § IV(I), *supra*.

To the extent that respondents may seek to present a single-reference obviousness argument, the administrative law judge has determined that respondents have not provided sufficient “suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000).

Accordingly, the administrative law judge has determined that respondents have not shown the asserted claims would have been obvious in light of Video Toaster alone.

T. Obviousness – Video Toaster and Porter & Duff

1. Claim 1

Respondents present obviousness arguments in their discussion of limitations [D] and [F]. *See* Resps. Br. at 284-87.

- a) ***Limitation [D]: blend a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image for storage in the at least one memory,***

(1) Analysis of Respondents’ Argument

Respondents argue, in part:

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To the extent Video Toaster does not disclose limitation [D], it would have been obvious to combine Video Toaster with Porter & Duff (RX-0244). RX-0382C at Q222. One of ordinary skill would have found it obvious to modify the ToasterPaint or the LightWave3D programs to enable blending of a plurality of graphics images using a plurality of alpha values associated with the graphics images to generate a blended graphics image using the existing hardware of the Video Toaster System. RX-0382C at Q222.

Resps. Br. at 283.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 132-33 (arguing that Video Toaster and Porter & Duff do “not disclose the claimed two-step alpha blending process of the ‘104 Patent.”); Broadcom Reply, Section II(E).

The administrative law judge previously determined that Porter & Duff discloses subject matter that satisfies limitation [D]. *See* § IV(K)(1)(a), *supra*. Broadcom’s argument with respect to Video Toaster does not alter that conclusion.

(2) Analysis of Broadcom’s Argument

The administrative law judge previously determined that Porter & Duff discloses subject matter that satisfies limitation [D]. *See* § IV(K)(1)(a), *supra*. Broadcom’s argument with respect to Video Toaster does not alter that conclusion.

b) Limitation [E]: process the graphics images and/or the blended graphics image to place the blended graphics image in a format suitable for blending with a video image, and

The administrative law judge previously determined that Video Toaster does not disclose subject matter corresponding to limitation [E]. *See* § IV(I)(1)(e), *supra*. Respondents have not argued that limitation [E] would have been obvious if Video Toaster did not disclose the

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limitation. *See* Resps. Br. at 285-86.⁴¹ Accordingly, the administrative law judge finds that claim 1 would not have been obvious in light of Video Toaster, at least because it does not teach or suggest limitation [E].

- c) ***Limitation [F]: blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values.***

Respondents argue, in part:

If the Video Toaster System does not meet a construction requiring a particular two-step blending process, it would have been obvious to one of ordinary skill to combine the Video Toaster System with Porter & Duff (RX-0244). RX-0382C.000062. The concept and mathematics of pre-multiplied alpha and the computational savings they provide are taught in Porter & Duff (RX-0244). RX-0382C.000063. One of ordinary skill developing software or hardware for blending of graphics and video images would be motivated to look for methods of alpha blending to achieve computational savings. *Id.* By reducing the computations required to perform alpha blending, one of ordinary skill understands that performance would be increased and implementation of the alpha blending would be lower cost. *Id.* The need to reduce computation in a system such as the Video Toaster System's device is a well-known problem. *Id.* Porter & Duff (RX-0244) is also in the same field of application as that of the Video Toaster System, namely the processing of graphics and video images in computing systems. *Id.* One of ordinary skill looking for the economies afforded by computational savings achieved by pre-multiplied alpha taught by Porter & Duff (RX-0244) would understand that achieving these savings is the predictable result of employing a simpler calculation method requiring fewer mathematical operations. *Id.* It would thus have been obvious for one of ordinary skill to look to Porter & Duff and combine it with the Video Toaster System for the use of pre-multiplied alpha and the corresponding equations. *Id.*

Resps. Br. at 286-87.

⁴¹ In some instances respondents argue that a missing limitation would have been obvious based on a given reference "alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation." *See, e.g.,* RX-0383C (Stevenson WS) at Q/A 87, 333. Limitation [E] of Video Toaster is not one of those instances.

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Broadcom argues, in part:

Video Toaster in view of Porter & Duff (RX-0244) does not render obvious Claim 1 because, as described above, Porter & Duff also does not disclose the claimed two-step alpha blending process of the '104 Patent. CX-578C (Havlicek WS) at Q/A 197, 203. There is no motivation to combine Video Toaster System with Porter & Duff, and that even if one were to make the combination, the combination of Video Toaster and Porter & Duff does not disclose or suggest all of the claim elements. *Id.*

Broadcom Br. at 132.

The administrative law judge previously determined that respondents have not shown, through clear and convincing evidence, that Video Toaster discloses a processor that blends a blended graphics image with video. Porter & Duff does not cure this deficiency. *See* CX-0578C (Havlicek RWS) at Q/A 197, 203 (“Video Toaster in view of Porter & Duff does not render obvious claim 1 because none of these references disclose the claimed two-step alpha blending process of the '104 patent.”). Further, respondents have not shown that Video Toaster and Porter & Duff disclose a two-step process for blending graphics. *Id.* Accordingly, the administrative law judge has determined that limitation [F] would not have been obvious based on the teaching of Video Toaster and Porter & Duff.

d) Respondents' Rationale for the Obviousness Argument

Respondents argue that:

One of ordinary skill developing software or hardware for blending of graphics and video images would be motivated to look for methods of alpha blending to achieve computational savings. *Id.* By reducing the computations required to perform alpha blending, one of ordinary skill understands that performance would be increased and implementation of the alpha blending would be lower cost. *Id.* The need to reduce computation in a system such as the Video Toaster System's device is a well-known problem. *Id.* Porter & Duff (RX-0244) is also in the same field of application as that of the Video Toaster System, namely the processing of graphics and video images in computing systems.

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Id. One of ordinary skill looking for the economies afforded by computational savings achieved by pre-multiplied alpha taught by Porter & Duff (RX-0244) would understand that achieving these savings is the predictable result of employing a simpler calculation method requiring fewer mathematical operations. *Id.* It would thus have been obvious for one of ordinary skill to look to Porter & Duff and combine it with the Video Toaster System for the use of pre-multiplied alpha and the corresponding equations. *Id.*

Resps. Br. at 287.

Broadcom argues, in part:

A POSA would NOT be motivated to modify Video Toaster to disclose “blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values” as required by claim 1 of the ‘104 Patent because Video Toaster neither teaches nor suggests creating a blended graphics image, let alone blending a blended graphics image a video image. [CX-0578C (Havlicek WS)] at Q/A 232.

Broadcom Br. at 132. Broadcom also argues that the combination of Video Toaster and Porter & Duff would not be operable because “once a video signal is present at the input of the analog video mixer on the NewTek hardware card, Toaster Paint and LightWave 3D can no longer be used to blend graphics images.” *Id.* at 133.

The administrative law judge has determined that a person of ordinary skill would not combine Video Toaster with Porter & Duff. *See* CX-0578C (Havlicek WS) at Q/A 209, 232. Respondents have not shown that a person of ordinary skill would look to Porter & Duff to improve a reference that cannot blend live video at certain times of operation (*e.g.*, the Video Toaster). *Id.* at 209-10. Further, there is no reasonable expectation of success as Toaster Paint and LightWave 3D cannot blend graphics images “once a video signal is present at the input of the analog video mixer on the NewTek hardware card[.]” *Id.*

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2. Claim 10

The administrative law judge previously determined that Video Toaster discloses subject matter that satisfies claim 10. *See* § IV(I)(3), *supra*. Accordingly, if claim 1 is found obvious, then claim 10 is obvious for the same reasons as claim 1.

3. Claims 11, 16, 17, and 22

Respondents and Broadcom have not presented separate arguments for claims 11, 16, 17, and 22. *See* Resps. Br. at 289-90 (respondents simply refer to prior arguments); Broadcom Br. at 127, 131 (same).

Accordingly, the administrative law judge has determined that respondents have not shown that claims 11, 16, 17, and 22 are anticipated based upon the same rationale provided with respect to claim 1.

U. Obviousness – Video Toaster, Porter & Duff, and West or Oakley

Respondents argue:

Claims 2-6, 9, 12-15, and 18-21 are invalid in view of Video Toaster. RX-0382C.000067. If Broadcom contends that Video Toaster does not disclose a polyphase filter or scaling of the graphics images of claims 2-6, 9 12-15, and 18-21, it would have been obvious to one of ordinary skill to combine Video Toaster with Oakley and/or West. RX-0382C.000067. As discussed previously, polyphase filters are disclosed in both Oakley and West. RX-0382C.000067. For the reasons discussed above, at least Oakley (RX-0149) discloses the additional features required by claims 2-5, 9, 12-15, and 18-21. *Id.* For the reasons discussed above, for claims 2, 4-6, 9, 12, 13, 18, 19, West (RX-0150) discloses the limitations of these dependent claims. *Id.*

One of ordinary skill would have been motivated to modify Video Toaster to use the polyphase filter of Oakley and/or West. RX-0382C.000067. Oakley is directed to a scaler in an integrated circuit for displaying component video on a television display. *Id.* One of ordinary skill would logically look to methods of processing and scaling video signals for projection on television displays in designing an integrated circuit for use in consumer

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electronics products. *Id.* Likewise, West discloses an “image scaling circuit for increasing or decreasing the size of a sampled image to match a fixed resolution display” and may “resiz[e] the image in the horizontal and vertical dimension.” *Id.* at 000067-68. Modifying Video Toaster to use a polyphase filter would be applying a known technique in a known device to yield predictable results. RX-0382C.000068. By employing a polyphase filtering, Video Toaster could achieve scaling and anti-flutter without the need for additional filters. *Id.* This reduces the complexity of the device and provides more flexibility. *Id.* As polyphase filtering was well-known, one would have looked to use such filters to enable more variability in sample rate modification. *Id.*

Resps. Br. at 289-90.

Broadcom argues:

Video Toaster System (RX-0410 to RX-0414) does not anticipate or render obvious independent claims 1, 11, or 17, and therefore, the Video Toaster System (RX-0410 to RX-0414) also does not anticipate or render obvious dependent claims 2-6, 9, 12-15, and 18-21. CX-578C (Havlicek WS) at Q/A 242-58, 268-77, 284-96. In addition, Video Toaster System does not disclose the elements of claims 2-6, 9, 12-15, and 18-21, and Dr. Medoff does not point to any evidence in Video Toaster System showing these elements. *Id.* Dr. Medoff relies on West (RX-0150) or Oakley (RX-0149) to show the element of claims 2-6, 9, 12-15, and 18-21. *Id.*; RX-0382C (Medoff WS) at Q/A 240-45. Neither West nor Oakley, however, cures the deficiencies of Video Toaster System discussed above. *Id.* Specifically, neither West nor Oakley discloses the claimed 2-step alpha blending recited in claim 1. *Id.* Further, Dr. Medoff does not rely on West or Oakley to cure the deficiencies in Video Toaster System (RX-0410 to RX-0414). *Id.* Thus, claims 2-6, 9, 12-15, and 18-21, are not rendered obvious by the combination of Video Toaster System (RX-0410 to RX-0414) with West or Oakley. *Id.*

Broadcom Br. at 133-34.

The administrative law judge finds that Oakley discloses subject matter claimed by claims 2-6, 9, 12-15, and 18-21 and that West discloses subject matter claimed by claims 2, 4-6, 9, 12, 13, 18, and 19. *See* RX-0382C (Medoff WS) at Q/A 191-203, 241-45. The administrative law judge also finds that a person of ordinary skill in the art would have modified Video Toaster

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and Porter & Duff with the teachings of Oakley or West as part of a *routine engineering and product development* effort associated with improving the processing and scaling video signals in television applications. *See, e.g.*, RX-0382C (Medoff WS) at Q/A 241-45 (“A POSITA would logically look to methods of processing and scaling video signals for projection on television displays in designing an integrated circuit for use in consumer electronics products.”).

Accordingly, if it is found that claim 1 would have been obvious, the administrative law judge also finds claims 2-6, 9, 12-15, and 18-21 would have been obvious over Video Toaster and Porter & Duff in view of Oakley or West.

V. Obviousness – Secondary Considerations

Apart from teaching away, which is discussed above in relation to Gloudemans, Broadcom has not clearly argued that secondary considerations support a non-obviousness finding.⁴² *See generally* Broadcom Br., Section IV(B)(7) (*e.g.*, commercial success, unexpected results, long-felt need, failure of others, etc. are not discussed); Broadcom Reply, Section II(E).

Respondents argue, in part:

Broadcom has asserted that secondary considerations of non-obviousness exist and support a conclusion that the asserted claims are not obvious. Broadcom has failed to prove, however, that secondary considerations exist. RX-0382C (Medoff) at Q358-61. . . .

Resps. Br. at 290; *see also* Resps. Reply, Section IV(D)(1) (secondary considerations are not mentioned).

⁴² The administrative law judge determined that Gloudemans did not teach away from a combination with Porter & Duff.

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Accordingly, in light of Broadcom and respondents' arguments concerning secondary considerations, the administrative law judge has determined that no evidence of secondary considerations supports a non-obviousness finding.

W. Indefiniteness

Respondents' entire argument is:

The claim terms "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values" / "blend the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values to generate the display image" / "blending the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values to generate the display image" in claims 1, 11 and 17 are indefinite if not construed according to Respondents' proposed construction. This is because the claim language presents uncertainty as to whether alpha values or a value derived from the alpha values are used to blend the blended graphics image with the video image. The "and/or" claim language presents multiple interpretations of this limitation, all of which are reasonable readings. To infringe, must a system 1) blend the blended graphics image with the video image using the alpha values, 2) blend the blended graphics image with the video image using a value derived from the alpha values, and 3) blend the blended graphics image with the video image using both the alpha values and a value derived from the alpha values? Or would a system performing just one of those infringe? Because one could reasonably interpret these claim terms differently, the claim fails to "inform those skilled in the art about the scope of the invention with *reasonable certainty*." See Bryan Garner, "LawProse Lesson #209: Ban 'and/or,'" available at <<http://www.lawprose.org/lawprose-lesson-209-ban-andor/>> ("Although using and/or seems like a quick and easy drafting tool, it's more of a quick and dirty one: it too often reflects a failure to think something through or to understand what the parties intend. It creates room for disagreement and litigation.").

Resps. Br. at 292-93.

Broadcom argues:

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Respondents have not proven claims 1, 11, and 17 of the '104 Patent are invalid because the claim phrase [to place the blended graphics image in] "a format suitable for blending with a [the] video image" is indefinite. This claim limitation is not indefinite and that in the context of blending graphics images with video, a POSA would easily understand that the graphics images and/or the blended graphics image must be in the same format [a format suitable for blending] as the video image in order to blend them together. *Id.* at Q/A 42. Alpha blending of images means weighted adding of images, and that one cannot meaningfully add two images unless they are the same size and unless their pixels represent the same units of spatial extent and color space. *Id.* These are elementary image processing concepts that would be easily understood by a POSA at the time of the invention. *Id.* Accordingly, this claim element is not indefinite.

In addition, Respondents have not proven that claims 1, 11, and 17 of the '104 Patent are invalid because the claim phrase "blend[ing] the blended graphics image with the video image using the alpha values and/or at least one value derived from the alpha values" is indefinite. CX-0578C (Havlicek WS) at Q/A 47-48. The claim element is not indefinite. *Id.* Specifically, the '104 Patent specification discloses exactly how the derived blending value AR(i) is to be calculated in the preferred embodiment (JX-0003 ('104 Patent)) at 45:52-57, 46:9-23, and 47:23-28); CX-0578C (Havlicek WS) at Q/A 43-46.

Moreover, the claim language itself makes it clear that the alpha values themselves and/or other values derived from the alpha values may be used to blend the blended graphics image with the video image in other embodiments. CX-0578C (Havlicek WS) at Q/A 43-46. In light of the claim language and the specification of the '104 Patent, a POSA would understand that, depending on the specific design goals and specific requirements of the application at hand, the blended graphics image could be blended with the video image using the derived values AR(i) prescribed for the preferred embodiment or using the alpha values and/or some other value or values derived from the alpha values as required for the application. *Id.* Thus, this claim element is not indefinite.

Broadcom Br. at 145-46.

Respondents reply:

Broadcom asserts that the claims are definite because the specification discloses the specific formula that Respondents'

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construction incorporates: $AR(i) = AR(i-1) * (1-A(i))$. CPostHg Br. 146. Broadcom then reverses course, asserting that “other values derived from the alpha values” or “the alpha values themselves” can **also** satisfy this element. *Id.* Broadcom’s admissions lead to one of two conclusions: either the claims require the formula in the specification or the claims cover unknown “other values” and thus fail to “inform those skilled in the art about the scope of the invention with reasonable certainty.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014).

Resps. Reply at 98.

The administrative law judge finds that respondents have not shown that claims 1, 11, and 17 are invalid for failing to delineate the scope of the invention with reasonable certainty. *See Nautilus*, 134 S. Ct. at 2124. The evidence shows that one of ordinary skill in the art would understand the contested phrases with reasonable certainty. *See* CX-0578C (Havlicek RWS) at Q/A 510; CX-0004C (Havlicek WS) at Q/A 47-48.

In addition, respondents have not cited any evidence supporting their position, nor have respondents identified any precedent where a claim using the phrase “and/or” was found indefinite. Accordingly, respondents have not shown that the claims of the ‘104 Patent are indefinite.

V. U.S. PATENT NO. 8,284,844

A. Overview of the ‘844 Patent

The ‘844 Patent (JX-0001), entitled “Video decoding system supporting multiple standards,” issued on October 9, 2012. The application that would issue as the ‘844 Patent, Application No. 10/114,798, was filed on April 1, 2002. The ‘844 Patent discloses a system that uses hardware accelerators to assist in decoding digital media from a variety of encoding/decoding formats.

B. Claim Construction

1. Level of Ordinary Skill in the Art

Broadcom's expert, Dr. Acton, testified as follows:

Q60. Dr. Acton have you formed an opinion as to the knowledge that a person of ordinary skill in the art with regard to the '844 and '059 patents would have had at the time of the claimed inventions?

A. In my opinion a POSA at the time of the invention of the '844 patent, which is JX-0001, and '059 patent, which is JX0002, would have had a Bachelor's Degree in Electrical Engineering, Computer Science, or a similar discipline with one to two years of experience in this or a related field. The POSA would also have been familiar with software or hardware related to digital signal image and video processing. I understand this is the definition of the level of ordinary skill in the art proposed by Broadcom and I agree with it

Q61. Are you aware of any definitions of the level of ordinary skill in the art that Respondents have proposed?

A. Yes I am I do not believe any of the various definitions proposed by Respondents should be adopted. But, if the Judge does adopt any of those definitions none of my opinions would change.

CX-0003C (Acton WS) at Q/A 60-61.

Respondents' expert, Dr. Stevenson, testified as follows:

Q47. What is your opinion on the level of ordinary skill in the art for the '844 patent?

A47. In my opinion, a person of ordinary skill in the field of art of the '844 patent would have had a combination of education and experience in engineering and communications systems. This typically would consist of at least a Master's degree in Electrical Engineering, Computer Science, or Computer Engineering with at least two to three years of experience in development and programming relating to video digital signal processing, or an equivalent degree and/or experience. The person of ordinary skill in the art would be familiar with the design of programmable real-time media processors. Superior education would compensate for a deficiency in experience, and vice-versa.

...

Q49. Did you consider the perspective of a POSITA in arriving at your expert opinions?

A49. Yes. In arriving at my expert opinions regarding the '844 patent, I have considered the issues from the perspective of this person of ordinary skill in the art, at the timeframe of the alleged invention of the subject matter of the '844 patent. I have also considered the issues from the perspective of Complainant's definition of a person of ordinary skill in the art at the timeframe of the alleged invention of the '844 patent.

RX-0383C (Stevenson WS) at Q/A 47, 49.

With respect to the '844 and '059 Patents, Broadcom states: "[t]he differences between the levels of ordinary skill in the art proposed by Broadcom and Respondents are minimal and do not effect analyses in this Investigation." Broadcom Reply at 2, n.2.

Having considered the experts' testimony, the administrative law judge has determined that a person of ordinary skill in the art would have a master's degree in electrical engineering, computer science, or computer engineering with two to three years of experience in development and programming relating to video digital signal processing, or an equivalent degree and/or experience. RX-0383C (Stevenson WS) at Q/A 47, 49. Dr. Acton's opinions do not change under this level of ordinary skill, *see* CX-0003C (Acton WS) at Q/A 61, and the differences between the levels of skill proposed by Broadcom and respondents are not material.

2. Disputed Constructions

The parties dispute the following terms and phrases from claim 1:

- "a processor adapted to control a decoding process"
- "a hardware accelerator"
- "digital media data stream"

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- “the accelerator is configurable to perform the decoding function according to a plurality of decoding methods”

Joint Outline at 3; Broadcom Br. at 153; Resps. Br. at 17-26.

Claim 1, with the disputed terms and phrases emphasized, follows:

1. A digital media decoding system comprising:

a processor adapted to control a decoding process; and

a hardware accelerator coupled to the processor and adapted to perform a decoding function on a *digital media data stream*, wherein *the accelerator is configurable to perform the decoding function according to a plurality of decoding methods*.

See JX-0001 at 20:17-23 (emphasis added).

a) “a processor adapted to control a decoding process”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	a core decoder processor designed to orchestrate decoding for each pipeline stage

See Broadcom Br. at 153; Resps. Br. at 17.

Broadcom argues:

As described in Broadcom’s claim construction briefing, this term does not need to be construed and should receive its plain and ordinary meaning. Dr. Acton agrees that this term does not need to be construed, as it is clear and would have a well-understood meaning to a POSA. CX-0003C (Acton WS) at Q/A 64. The ‘844 Patent uses the term “a processor adapted to control a decoding process” in its ordinary way and imposes no special definition. See JX-0001 (‘844 Patent), 2:43-45; 15:3-11; 16:13-20; 17:39-41; 18:36-48; claim 1.

Broadcom Br. at 153-54. Broadcom then critiques respondents’ construction. *Id.* at 154-55.

Respondents argue:

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Respondents' construction is consistent with how the '844 Patent repeatedly characterizes the "invention." RX-0383C.0015 (Stevenson) Q36. Specifically, the '844 Patent states that its "*present invention . . . provides flexible and programmable decoding resources,*" using two main elements, a core processor and accelerators. *Id.* at 3:57-59 (emphasis added). Indeed, the patent distinguishes "the decoding system of the present invention" from others by noting that "each hardware accelerator runs in parallel according to a processing pipeline dictated by the firmware in the core processor." *Id.* at 5:7-26. "Upon completion of the high-level functions, each accelerator notifies the main core processor, which in turn decides what the next processing pipeline step should be." *Id.* at 5:26-29.

Resps. Br. at 17. Respondents rely further on the specification and Dr. Acton's testimony. *Id.* at 18-19.

The administrative law judge construes "a processor adapted to control a decoding process" to mean "a core decoder processor designed to orchestrate decoding for each pipeline stage."

Broadcom's proposed "plain and ordinary meaning" construction does not provide a basis for understanding the phrase or its limits. Although Dr. Acton provides some discussion of what a person of ordinary skill in the art would understand the phrase to mean, *see* CX-0003C (Acton WS) at Q/A 64, the discussion does not elucidate understanding of the term. For example, in explaining what "adapted to" means to one of ordinary skill, Dr. Acton explains "Adapted is also a term with a commonly understood meaning and especially in the context of a processor one of skill would understand that one way a processor is adapted to do a certain function is when it is programmed." CX-0003C (Acton WS) at Q/A 64. Similarly, in explaining what "control" means to a person of skill in the art, Dr. Acton testified that the verb "could be satisfied by selecting the proper decoding standard configuring the decoder for that standard and

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initiating the decoding process.” CX-0003C (Acton WS) at Q/A 64.⁴³ Explanation is indeed needed to provide additional understanding of the phrase. Yet, Dr. Acton’s testimony does not address the parts of the specification that Dr. Stevenson discusses. *See id.*

Respondents’ proposed construction provides context for determining the objective scope of the disputed phrase. In particular, the meaning of “a processor adapted to control a decoding process” is not immediately apparent from the words themselves. Likewise, the meaning is not immediately apparent from adjacent words of claim 1 or the dependent claims, as these do not further inform the disputed phrase in a meaningful way. The specification, however, provides the following guidance on what the processor is and does:

The decoding system of the present invention employs high-level granularity acceleration with internal programmability or configurability to achieve the requirements above by implementation of very fundamental processing structures that can be configured dynamically *by the core decoder processor*. This contrasts with a system employing fine-granularity acceleration, such as multiply-accumulate (MAC), adders, multipliers, FFT functions, DCT functions, etc. In a fine-granularity acceleration system, the decompression algorithm has to be implemented with firmware that uses individual low-level instructions (such as MAC) to implement a high-level function, and each instruction runs on the core processor. In the high-level granularity system of the present invention, the firmware configures each hardware accelerator, which in turn represent high-level functions (such as motion compensation) that run (using a well defined specification of input data) without intervention from the main core processor. Therefore, each hardware accelerator runs in parallel according to a processing pipeline dictated by the firmware in the core processor. Upon completion of the high-level functions, each accelerator notifies the main core processor, which in turn decides what the next processing pipeline step should be.

⁴³ Dr. Acton also testified that “Control would be controlling, doing things like starting, providing data, stopping, checking status.” Acton Tr. 155-156.

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The software control typically consists of a simple pipeline that orchestrates decoding by issuing commands to each hardware accelerator module for each pipeline stage, and a status reporting mechanism that makes sure that all modules have completed their pipeline tasks before issuing the start of the next pipeline stage.

... The core processor 302 also orchestrates the macroblock (MB) processing pipeline for all modules and fetches the required data from main memory via the bridge 304. The core processor 302 also handles some data processing tasks.

JX-0001 at 5:7-47(emphasis added); *see also id.* at 7:60-61 (“The core processor 302 is the master of the decoding system 300. It controls the data flow of decoding processing.”); *id.* at 16:13-18; 17:39-41; RX-0383C (Stevenson WS) at Q/A 36.

The administrative law judge notes that the parties do not argue that the prosecution history has any material contribution that informs the construction of the phrase. For example, neither party cites to specific portions of the prosecution history (*i.e.*, JX-0004).⁴⁴

b) “a hardware accelerator”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning Alternatively: a hardware component that performs one or more operations separately from the processor to perform decoding faster than the processor alone	specialized hardware that assists the processor by accelerating decoding function(s)

See Broadcom Br. at 155; Resps. Br. at 19.

Broadcom argues:

The specification of the ‘844 Patent uses the term “hardware accelerator” consistent with its plain and ordinary meaning. The background section of the ‘844 Patent specifically describes prior art systems that relied solely on general purpose processors to do

⁴⁴ Apart from expert testimony, the parties do not cite to extrinsic evidence.

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all the decoding. JX-0001 ('844 Patent), 1:59-2:36. Dr. Acton explained that using only a single processor results in slower decoding operations. CX-0579C (Acton WS) at Q/A 20. The '844 Patent also acknowledges other processor-based systems in the prior art. This includes the use of a general purpose processor, along with special-purpose processors – called digital signal processors (DSPs). The '844 Patent notes that these DSP solutions are difficult to program and are “limited in performance, despite very high clock rates” and do “not lend itself to creating mass market, commercially attractive systems.” JX-0001 ('844 Patent), 2:12-26. The '844 Patent further acknowledges the use of processor-based accelerators: “where the processors are dedicated for decoding compressed video, special processing accelerators are tightly coupled to the instruction pipeline and are part of the core of the main processor.” *Id.* at 2:23-26. The background section of the '844 Patent makes clear that the invention of the '844 is not directed to programmable general purpose processors or DSPs, but instead to configurable **hardware** accelerators. CX-0579C (Acton WS) at Q/A 20. Also, the '844 specification explicitly distinguishes a DSP “coprocessor” from the claimed “hardware accelerators.” Specifically, the '844 Patent states that: “In an illustrative embodiment of the present invention, the PVL module 306 is designed as a coprocessor to the core processor 302, while the rest of the modules 308, 309, 310, 312 and 314 are designed as hardware accelerators.” JX-0001 ('844 Patent), 6:28-31.

Respondents' proposed construction does not add clarity and improperly narrows the claim term. Respondents proposed addition of the word “specialized” does not clarify the meaning of this term. Respondents also attempt to limit the term “hardware accelerator” to “hardware that assists the processor,” but this is not supported by any intrinsic evidence. In addition, Respondents' proposed construction improperly imports limitations and functionality that is expressly described other claims. For example, dependent claim 5 requires that “the hardware accelerator is adapted to assist the processor.”

Broadcom Br. at 155-57.

Respondents argue, in part:

Both parties' constructions reflect that the hardware accelerator is meant to speed up operations. But defining the term based on speed alone fails to accurately capture the meaning of the term as used in the '844 Patent. The intrinsic evidence provides that the

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“hardware accelerators” both assist the processor and are specialized. For example, the ‘844 Patent characterizes the invention in terms of the relationship between the hardware accelerator and the processor, namely in the former assisting the latter. *See* JX-0001 (‘844 Patent) at 4:43-47, 5:24-35.

In addition, the patent characterizes “hardware accelerator” as hardware specialized for particular tasks. The ‘844 Patent discloses that in the “**present invention**” the accelerators speed up discrete decoding functions, such as “inverse quantization (IQ), inverse discrete cosine transform (IDCT), pixel filtering (PF), motion compensation (MC), and de-blocking/de-ringing (loop filtering or post-processing).” *Id.* at 4:55-65 (emphases added). That is, the ‘844 Patent relies on the accelerators having a specialized functionality.

Resps. Br. at 19.

The administrative law judge construes “a hardware accelerator” to mean “a hardware component that performs one or more operations separately from the processor to perform decoding faster than the processor alone.”⁴⁵ *See* CX-0003C (Acton WS) at Q/A 66. The construction comports with the claim language and assists in understanding the disputed term. It also accounts for dependent claim 5, which clarifies that a hardware accelerator can be adapted to assist a processor.

Respondents’ proposed construction introduces uncertainty insofar as how the hardware is “specialized” is somewhat ambiguous. Further, although respondents rely on the “present invention” in arguing for their construction, the patent’s use of “present invention” does not describe the features of the invention as a whole—indeed, the phrase “present invention” is used throughout the specification to describe many different aspects of video decoding systems. *See*,

⁴⁵ Broadcom has also argued that: “The broadest reasonable construction of the term ‘hardware accelerator’ as it is used in the ‘844 Patent is ‘a hardware component that performs one or more operations separately from the processor to perform decoding faster than the processor alone.’” IPR2017-01111, Patent Owner’s Preliminary Response at 12 (July 6, 2017). Broadcom’s preliminary response is RX-0174.

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e.g., JX-0001 at 1:37-40; 2:32-36; 2:40; 2:47; 2:56; 2:64; 3:9-10; 3:24-53; 3:55-63; 4:31; 5:7; 5:37; 7:67; 9:7; 10:21; 11:59-60; 14:4-14; 14: 32-35; 15:5; 16:2; 17:31; 18:27; 19:6; 20:3.

c) “digital media data stream”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	a transport stream

See Broadcom Br. at 157; Resps. Br. at 23.

Broadcom argues:

As described in Broadcom’s claim construction briefing, this term does not need to be construed and should be given its plain and ordinary meaning. Dr. Acton testified that the term “digital media data stream” would have a well understood meaning to one of ordinary skill in the art. CX-0003C (Acton WS) at Q/A 62. It is simple a stream digital media data. *Id.* at Q/A 41, 62, 63. And no additional words are necessary to understand this term.

Respondents propose limiting the term “digital media data stream” to a specific type of stream, a “transport stream.” This is wrong for three reasons. First, the ‘844 Patent specification uses the term “digital media data stream” in its ordinary way and does not limit the term to a transport stream. *See* JX-0001 (‘844 Patent), 2:43-45; 2:47-48; 2:64-65; 4:3-7; 15:12-15; claims 1, 3, 5, 6. The specification specifically discusses “digital media data streams of a plurality of formats.” *Id.* at 20:45-51. A transport stream is specific to the MPEG-2 format. CX-0579C (Acton WS) at Q/A 55. By referring to digital media data streams of a plurality of formats (*i.e.*, standards) the specification makes clear that the term digital media data stream is not limited to one type of stream from one particular standard. Because Respondents’ proposed construction would limit the “digital media data stream” to a single format, it should not be adopted.

Second, one of Respondents’ own experts, Dr. Stevenson, conceded at trial that the term “digital media data stream” can be used to describe an MPEG-2 “elementary stream.” He admitted that an MPEG-2 elementary stream, which is transported inside a

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transport stream, is also a “digital media data stream.” Tr. (Stevenson) at 644:16-645:16.

Third, the specification uses the term “transport stream” (*see e.g.*, JX-0001, 4:31-33), yet the claim language does not use that term and, instead, uses the broader term “digital media data stream.” If the patentees intended to limit the claim scope to a transport stream, they would have used that term.

Broadcom Br. at 157.

Respondents argue, in part:

There is no dispute that the ‘844 Patent discloses a transport processor that receives and processes an incoming transport stream. JX-0001 (‘844 Patent) at 4:31-32 (“Transport streams are parsed by the transport processor 102”). In describing what the transport processor receives and processes, the ‘844 Patent uses the terms “digital media data stream” and “transport stream” interchangeably. *Id.* at 4:3-7 (“The transport processor 102 receives and processes a digital media data stream”). No other incoming stream type is described as being received by the transport processor.

The incoming “digital media data stream” is further described as having an “audio portion” and a “video portion” consistent with a transport stream. *Id.* at 4:3-7, 4:31-36. Indeed, it is a transport stream that the ‘844 Patent envisions the transport processor receiving and processing to “provide[] the audio portion of the data stream to the audio decoder 104 and provide[] the video portion of the data stream to the digital video decoder 116.” *Id.* at 31-33 (“Transport streams are parsed by the transport processor”).

Resps. Br. at 23. Respondents conclude that their “construction captures the ‘844 Patent’s disclosure that a digital media data stream is a transport container that contains multiplexed audio and video.” *Id.* at 24 (citing Stevenson Tr. 645-647).

The administrative law judge has determined that the term “digital media data stream” does not need construction. The ‘844 Patent does not limit a “digital media data stream” to a transport stream as respondents suggest. In particular, although the ‘844 Patent uses the term

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“transport stream” in the specification, it is omitted from the claims. Thus, construing a “digital media data stream” to mean a “transport stream” would unnecessarily narrow the term.

- d) *“wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.”*

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	the accelerator is internally programmable by the processor to perform its decoding function according to a plurality of decoding methods

See Broadcom Br. at 158; Resps. Br. at 25.

Broadcom argues:

As described in Broadcom’s claim construction briefing, this phrase does not need to be construed and should receive its plain and ordinary meaning. Dr. Acton explained that this phrase does not need to be construed, as it is clear and would have a well-understood meaning to a POSA. CX-0003C (Acton WS) at Q/A 65. The ‘844 Patent specification uses the phrase in its ordinary way, and imposes no special definition. See JX-0001 (‘844 Patent), Abstract, 2:45-46; 5:7-12; 11:48-54; 12:18-24; 15:15-24; claims 1-6, 10.

Broadcom Br. at 158. Broadcom then critiques respondents’ construction. *Id.* at 158-60.

Respondents argue:

The parties’ dispute centers on whether the term “accelerator is configurable . . .” means the accelerator must be internally programmable by the processor. See RX-0383C (Stevenson) Q38. The claim is so limited when read in light of the specification. See RX-0383C (Stevenson) Q40. Indeed, the U.S. Patent Office recently held that the hardware accelerator of the ‘844 Patent “is configurable only if its functionality can be internally reprogrammed.” IPR2017-01624, Denial, at 8 (Dec. 19, 2017). The internal programmability of the hardware accelerator is core to the ‘844 Patent’s invention:

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The decoding system of **the present invention** employs high-level granularity acceleration with **internal programmability or configurability** to achieve the requirements above by implementation of very fundamental processing structures that can be **configured dynamically by the core decoder processor**.

JX-0001 ('844 Patent) at 5:7-12 (emphasis added); *see also* RX-0383C.0016 (Stevenson) Q40.

Not only is the accelerator's internal programmability described as the core of the invention, it is the sole basis on which the '844 Patent distinguishes the prior art. *See* RX-0383C (Stevenson) Q40. The patent distinguishes internal programmability of the "present invention" with the fine level granularity in prior art hardware accelerator-based systems. JX-0001 ('844 Patent) at 5:14-29; RX-0383C (Stevenson) Q40. The programmable hardware accelerators of the '844 Patent are in contrast to the prior art "fixed hardware implementations." JX-0001 at 4:66-5:6; RX-1083C (Bovik) Q27, 26.

Broadcom disagrees with Respondents, arguing: (1) the internal programmability requirement "improperly reads limitations into the claim from the specification" and (2) the recitation of "its decoding function" excludes hardware accelerators that perform multiple decoding functions. Compl. Op. CC 10 (EDIS 620336). Both arguments fail. First, Broadcom ignores the express disclaimer in the specification and prosecution history, requiring an internally programmable hardware accelerator, which is described as being programmed by the processor. The Patent Office's ruling is in accord, which Broadcom also ignores. Second, the "its decoding function" language only clarifies that the accelerator is performing the decoding function(s) it is configured to perform.

Resps. Br. at 25-26.⁴⁶

⁴⁶ In denying LG's request for *inter partes* review, when construing "configurable," the Patent Trial and Appeal Board noted the following: "In construing this term, we have considered the specification of the '353 patent and its prosecution history. *Microsoft Corp. v. Proxycinn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015). In accord with these portions of the '844 patent specification and file history discussed *supra*, we conclude that a hardware accelerator is configurable only if its functionality can be internally reprogrammed. Thus, under our construction, an accelerator selected by an API or other instrumentality would not itself be

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The administrative law judge construes “wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods” to mean “the accelerator is internally programmable by the processor to perform its decoding function according to a plurality of decoding methods.”

As an initial matter, the words of claim 1—those apart from the disputed phrase—do not further explain the meaning of the disputed phrase. *See* RX-0383C (Stevenson WS) at Q/A 40. The dependent claims, however, provide additional detail as to what the accelerator is able to do, and how it does it. *See, e.g.*, JX-0001 at 20:17-67 (claims 1-10).

The specification and prosecution history further support the construction. In particular, the specification states that “Each hardware module 306, 308, 309, 310, 312 and 314 is internally configurable or programmable to allow changes according to various processing algorithms.” JX-0001 at 5:62-64; *see also* RX-0383C (Stevenson WS) at Q/A 40. The specification also states that the invention’s fundamental processing structures “can be configured dynamically” by the core processor. *Id.* at 5:7-12. Additionally, in an appeal brief that includes a summary of claim 1, the applicant explained that “Each hardware module 306, 308, 309, 310, 312 and 314 is internally configurable or programmable to allow changes according to various processing algorithms.” JX-0004 at 3264. Taken together, the specification and the prosecution history support the construction.⁴⁷

‘configurable.’ This will be discussed further *infra*.” IPR2017-01624, Denial, at 8 (Dec. 19, 2017)

⁴⁷ Apart from expert testimony, the parties do not cite to extrinsic evidence.

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C. Whether Sigma Infringes the Asserted Claims

Broadcom asserts claims 1-4 and 6-10. *See* Broadcom Br. at 162-66, 166-71. Claims 2-4 and 6-10 all depend from claim 1. JX-0001 at 20:17-67.

In general, Sigma argues that it does not infringe claim 1 because its SX-6 SoC does not include “a processor adapted to control a decoding process” (limitation [A]) or “a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream” (limitation [C]). *See* Resps. Br. at 51, 53; Resps. Reply at 27.

1. Claim 1

Claim 1, which Broadcom divides into five limitations, follows:

1. [Preamble] A digital media decoding system comprising:
 - [A] a processor adapted to control a decoding process; and
 - [B] a hardware accelerator coupled to the processor and
 - [C] adapted to perform a decoding function on a digital media data stream,
 - [D] wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.

See Broadcom Br. at 162; JX-0001 at 20:17-23.

a) *[Preamble]: A digital media decoding system comprising:*

Broadcom argues:

The evidence shows that the SX-6 SoC provides a digital media decoding system. CX-0003C (Acton WS) at Q/A 153-54. At trial, Dr. Stevenson conceded that there is no dispute regarding infringement of the preamble. Tr. (Stevenson) at 615:20-616:6. Thus, to the extent that the preamble of claim 1 is a limitation, the SX-6 SoC meets this element.

Broadcom Br. at 162.

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Sigma does not clearly rebut this argument. *See generally* Resps. Br. at 49-54; Resps. Reply at 27 (contesting limitations [A] and [C]).

The evidence shows that the SX-6 SoC decodes digital media, as described by the preamble. *See* CX-0003C (Acton WS) at Q/A 153-54. Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies the preamble.

b) Limitation [A]: a processor adapted to control a decoding process; and

The administrative law judge construed "a processor adapted to control a decoding process" to mean "a core decoder processor designed to orchestrate decoding for []." *See* § V(B)(2)(a), *supra*.

For infringement, Broadcom argues:

The evidence shows that the SX-6 satisfies this limitation under Broadcom's proposed construction. As discussed above, the '844 Patent describes varying degrees of control. *See supra* Section V.A.1.a. One level of control involves simply configuring and starting the hardware accelerators. *Id.* The SX-6 SoC includes a [

] controls the decoding process.

The fact the SX-6's [

] is further confirmed by the SX-6 datasheet and Sigma's own corporate witness. The SX-6's datasheet expressly states that the [

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].” *Id.* at 59:1-10.

Further, neither Respondents’ Prehearing Brief nor Dr. Stevenson’s Witness Statement on infringement disputes that the [] controls the decoding process under Broadcom’s construction. Respondents’ Prehearing Brief at 57-61; RX-1079C (Stevenson WS) at Q/A 60-69.

Broadcom Br. at 162-64. Broadcom also argues that the [] satisfies this limitation under respondents’ construction. Broadcom Br. at 167-68; *see also* CX-0003C (Acton WS) at Q/A 161 (testifying that his opinion “doesn’t change” under respondents’ construction).

Respondents argue:

... based upon Respondents’ claim construction, the [] does not meet this limitation. As discussed above, Sigma’s SX6 chip’s host processor, [] including of the decoding process. RX-0620C.00009; RX-1079C at Q62-63. In fact, even Broadcom’s expert Dr. Acton agreed. CX-0003C at Q183-184. Specifically, Dr. Acton testified that “[] also controls the video decoder functionality.” *Id.* at Q185.

Further, the [] does not orchestrate decoding for [] of Sigma’s SX6 chip. The experts agree that []

[]. RX-1079C at Q63.

[]

[]. RX-1079C at Q63. Because the [] alone does not orchestrate decoding of “each pipeline stage,” the [] does not meet the claim 1

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requirement of “a processor adapted to control a decoding process.” *Id.* at Q62-63.

Resps. Br. at 51.

Broadcom replies, in part:

Sigma argues Dr. Acton effectively admitted that the []
[]. *Id.* at 51
(citing CX-0003C at Q/A 183-184). But that misquotes Dr. Acton.
Dr. Acton testified that “[

[] controls the
decoding process.

While Sigma does not dispute that the SX6 includes []
[], Sigma argues that the “[] alone does not
orchestrate decoding of ‘each pipeline stage.’” *Id.* at 51-52.
However, Sigma never states what pipeline stages are not
orchestrated by the []. *Id.* at 51-53. Sigma appears to
suggest that [

[]. However, the ‘844 patent makes clear those two
things are not decoding functions, so the fact that they are
performed outside the [

[] processor from being a core decoder processor under
Respondents’ construction. *See e.g.*, JX-0001 (‘844 Patent),
15:34-36, Fig. 6. In fact, LG’s expert admitted that tasks
performed prior to decoding (such as the two identified by Sigma
above) are not part of the decoding process: “One of ordinary skill
would understand that tasks performed to initiate decoding are not
decoding functions themselves. RX-1083C (Bovik) Q169.”
RPostHB at 43. Accordingly, even under Respondents’ proposed
construction, the SX-6 satisfies this claim limitation.

Broadcom Reply at 60 (footnote omitted).

Having considered the parties’ arguments, the administrative law has determined that
Broadcom has not shown, by a preponderance of the evidence, that the [] is
a processor that controls the decoding process, as described in claim 1. The evidence shows that

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the SX-6's [

] See RX-1079C (Stevenson RWS) at Q/A 62-64; RX-0612C at 23-24; RX-0620C at 9. Although Broadcom contends that Sigma's representative testified that the [] controls decoding, Broadcom did not establish that the deponent's answer was specific to the terminology the '844 Patent employs. Additionally, Dr. Acton's testimony, CX-0003C (Acton WS) at Q/A 161, relies on defining a "core decoder processor" as "a processor other than the host processor" in order to reach infringement.

Accordingly, the administrative law judge has determined that Broadcom has not shown, by a preponderance of the evidence, that Sigma's SX-6 SoC satisfies this limitation.

c) Limitation [B]: a hardware accelerator coupled to the processor and

Broadcom argues:

The evidence shows that the SX-6 satisfies this limitation under Broadcom's proposed construction. The SX-6 SoC includes hardware accelerators such as [

] CX-0003C (Acton WS) at Q/A 162-67 (citing source code and Sigma corporate witness testimony). Dr. Acton identified [

] that comprise the hardware accelerators. *Id.* Sigma does not dispute this. In fact, at trial, Dr. Stevenson admitted that the SX-6 contains hardware accelerators, and specifically agreed [

] are hardware accelerators. Tr. (Stevenson) at 614:19-620:8. Accordingly, the SX-6 SoC satisfies this limitation.

Broadcom Br. at 164.

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Sigma does not clearly rebut this argument under either Broadcom's or respondents' constructions. *See generally* Resps. Br. at 49-54; Resps. Reply at 27 (contesting limitations [A] and [C]).

The evidence shows that the SX-6 SoC includes a hardware accelerator coupled to the processor, as described by limitation [B]. *See* CX-0003C (Acton WS) at Q/A 162-67. Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation under Broadcom's or respondents' constructions.

d) *Limitation [C]: adapted to perform a decoding function on a digital media data stream,*

Broadcom argues:

The evidence shows that the SX-6 satisfies this limitation under Broadcom's proposed construction. As discussed above, the '844 Patent describes a "digital media data stream" broadly and describes the hardware accelerators as performing their respective decoding functions on the transport stream's elementary video stream data. *See supra* Section V.A.1.c. Thus, the ordinary meaning of a "digital media data stream" includes not only the transport stream (as Respondents argue) but also the elementary stream data it contains. Notably, on cross-examination at trial, Dr. Stevenson agreed that an MPEG 2 elementary stream could be considered a digital media data stream. Tr. (Stevenson) at 644:16-645:16.

It is undisputed that a SX-6 receives [

] for decoding. *See supra* Section V.A.2.a. It is also undisputed that the SX-6 SoC's hardware accelerators ([

)]

each perform their respective decoding functions on the [], *i.e.*, a digital media data stream. CX-0003C (Acton WS) at Q/A 162-67 (citing source code and Sigma corporate witness testimony); RX-1079C (Stevenson WS) at Q/A 70. Accordingly, the SX-6 SoC's hardware accelerators are adapted to perform their decoding functions on a digital media stream.

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Broadcom Br. at 164-65.

Respondents argue:

Claim 1 also requires “a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream.” Respondents contend the term “digital media data stream” should be construed as “a transport stream.” RX-0424. Consistent with Respondents’ claim construction, the [

].”). Thus, the SX6 does not have a hardware accelerator that performs a decoding function on a transport stream. *Id.* Moreover, the [] does not receive a transport stream. *Id.* Rather, it receives a []”) (emphasis added); *see* RX1079C at Q72; RX-0613.00010.

Dr. Acton also argues the purported hardware accelerators ([

]) are “are adapted to perform a decoding function on a digital media data stream.” CX-0003C at Q162-164 (emphasis added); RX-0613C.00015-18; RX-0612C.00033. These hardware accelerators, however, do not operate on a transport stream, but []. RX-0612C.00033 (“PES decoder”) (emphasis added); *see* RX1079C at Q72; RX-0613C.00010 (“[]”).

Further, Dr. Acton’s comparison of the [

], which is not what is claimed by the ‘844 Patent. RX-1079C at Q72. As such, Sigma’s

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Accused SoCs do not meet this limitation under Respondents' proper construction and do not infringe claim 1 of the '844 Patent.

Resps. Br. at 53-54.

The evidence shows that the SX-6 SoC includes a hardware accelerator that decodes a digital media data stream, as described by limitation[C].⁴⁸ In particular, the SX-6 SoC includes an [], which are hardware accelerators. See CX-0003C (Acton WS) at Q/A 163-64. The [] performs a decoding function by performing [], and the [] module performs a decoding function by performing [] operations. *Id.*

Sigma's non-infringement argument relies on construing "digital media data stream" to just "a transport stream." The administrative law judge, however, did not adopt respondents' construction.

Accordingly, the administrative law judge has determined that Sigma's SX-6 SoC satisfies this limitation (provided the [] satisfies limitation [A], which was ultimately not found).

- e) ***Limitation [D]: wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.***

Broadcom argues:

Lastly, claim 1 requires "wherein the accelerator is configurable to perform a decoding function according to a plurality of decoding

⁴⁸ Dr. Acton opines that the [] is the processor. The administrative law judge previously determined that [] [] is the processor. The limitation is not satisfied if the [] processor is the processor, because Dr. Acton opines: "The SX6' s plurality of hardware accelerators are also each coupled to the []." CX-0003C (Acton WS) at Q/A 162.

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methods.” The evidence shows that the SX-6 satisfies this limitation under Broadcom’s proposed construction. In the SX-6, the [

]). This is further confirmed by Sigma’s own corporate witnesses. CX-0003C (Acton WS) at Q/A 171 (citing CX-0515C (Liang Dep. Tr.) at 56:11-57:3; CX-0513C (Ignaszewski Dep. Tr.) at 63:4-64:8). And it was also confirmed at trial by Dr. Stevenson, who admitted on cross-examination that the [hardware accelerators are both configurable. Tr. (Stevenson) at 614:6-620:8. Accordingly, the SX-6 SoC satisfies this limitation.

Broadcom Br. at 165.

Sigma does not clearly rebut this argument. *See generally* Resps. Br. at 49-54; Resps. Reply at 27 (contesting limitations [A] and [C]).

The evidence shows that the SX-6 SoC includes a hardware accelerator that is configurable to perform decoding per multiple decoding methods, as described by limitation [D]. *See* CX-0003C (Acton WS) at Q/A 162-67. Accordingly, the administrative law judge has determined that Sigma’s SX-6 SoC satisfies this limitation.

2. Claims 2-4 and 6-10

Broadcom argues:

The evidence shows that the SX-6 infringes dependent claims 2-4 and 6-10 when those claims are properly construed as proposed by Broadcom. CX-0003C (Acton WS) at Q/A 173-80. With respect to claims 2-4 and 6-10, Sigma does not present any non-infringement arguments other than those presented for independent claim 1. Accordingly, if infringement is found with respect to claim 1, Sigma does not dispute infringement of dependent claims 2-4 and 6-10.

Broadcom Br. at 166. Broadcom also argues:

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With respect to claims 2-4 and 6-10, Sigma does not present any new non-infringement arguments specific to Respondents' proposed constructions. If infringement is found with respect to claim 1 under Respondents' proposed constructions, Sigma does not dispute infringement of dependent claims 2-4 and 6-10. Accordingly, for the reasons discussed above with respect to Broadcom's proposed constructions, the SX-6 SoC infringes claims 2-4 and 6-10.

Id. at 171.

Sigma's entire argument is:

Claims 2-4 and 6-10 of the '844 Patent depend either directly or indirectly from independent claim 1. Because Sigma's SoCs do not infringe claim 1 of the '844 Patent, the Sigma Accused SoCs do not infringe dependent claims 2-4 and 6-10. RX-1079C at Q75-90.

Resps. Br. at 54. Thus, Sigma has not presented separate argument for claims 2-4 and 6-10.

The administrative law judge determined that Sigma's SX-6 SoC does not infringe claim 1. Accordingly, the administrative law judge finds that Sigma does not infringe dependent claims 2-4 and 6-10. *See Ferring, supra*. If it is later determined that Sigma's SX-6 SoC infringes claims 1, then the administrative law judge would find that claims 2-4 and 6-10 are infringed. *See CX-0003C (Acton WS) at Q/A 173-80*.

D. Whether VIZIO Infringes the Asserted Claims

Broadcom argues:

The Accused VIZIO Products []. *See* Acc. Prods. Stmt. Specifically, the only accused VIZIO products at issue in this Investigation are the VIZIO products that [] identified in Exhibit F to the Joint Statement Regarding Identification of Accused Products. Any consumer audiovisual product containing an accused SoC, [], which, as discussed above is representative of [], infringes claims 1-4 and 6-10 of the '844 Patent. *See, e.g., CX-0003C (Acton WS) at Q/A 9, 223*.

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Broadcom Br. at 171.

VIZIO argues:

VIZIO's accused products do not infringe any claim of the '844 Patent at least [] does not infringe those claims. RX-1079C at Q138. Further, Broadcom has failed to show that any accused VIZIO product is adapted in the manner described by the claims of the '844 Patent. *Id.* Claim 1 of the '844 Patent recites "a processor adapted to control a decoding process" and "a hardware accelerator coupled to the processor and adapted to perform a decoding function on a digital media data stream." *Id.* at Q140; JX-0001.0022 at claim 1. But Dr. Acton does not cite to or describe testing of any accused VIZIO product to show that the purported processors and accelerators allegedly in the VIZIO products are adapted as described by the claims of the '844 Patent. RX-1079C at Q140. Indeed, Dr. Acton has failed to provide *any* evidence of testing of a VIZIO accused product at all. *Id.* Instead, Dr. Acton based his VIZIO infringement opinions solely on []. Tr. (Acton) at 133:1-4. Because Dr. Acton has not provided evidence of testing a VIZIO product, he cannot establish that the accused VIZIO products contain processors or accelerators adapted in the manner described by the claims of the '844 Patent. RX-1079C at Q140.

Moreover, Broadcom has failed to provide any evidence or testing to establish the functionality of the software (source code) that is actually installed in the accused VIZIO products. Tr. (Acton) at 133:5-134:11; RX-1079C at Q141. VIZIO does not: (1) [

]"), (2) have any [] that may be included [], and (3) know what [

]. RX-1086C at Q42-44; Tr. (Hwang) at 507:9-12. Indeed, [], as long as they []. RX-1086 at Q13-16. But Broadcom failed to name any of [] as respondents or attempt to seek any discovery from them. And Dr. Acton did not examine any final software associated with any VIZIO product to determine whether the products operate in the manner alleged. Tr. (Acton) at 133:5-134:11; RX-1079C at Q141. Thus, Broadcom did not prove direct, literal infringement.

Resps. Br. at 54-55.

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Having considered the parties' arguments, the administrative law judge has determined that the accused VIZIO products either infringe, or do not infringe, [] either do or do not infringe. VIZIO did not present (*e.g.*, cite) any expert testimony opining that its televisions do not infringe the asserted claims. Similarly, while VIZIO faults Broadcom for the thoroughness of its argument, VIZIO does not present any argument explaining how the alleged deficiencies are material. Accordingly, the administrative law judge has determined that the accused VIZIO products must receive [].

E. Whether Broadcom Practices Claims 1-13

Broadcom argues that the [] practices claims 1-13 of the '844 Patent. Broadcom Br. at 192-93. Broadcom provides argument under its constructions and respondents' constructions. *Id.* at 194-200.

1. Claim 1

a) [Preamble]: A digital media decoding system comprising:

Broadcom argues:

The [] SoC practices claim 1 of the '844 Patent. CX-0003C (Acton WS) at Q/A 231-55. The preamble of claim 1 recites "A digital media decoding system comprising." The [] SoC provides a digital media decoding system. CX-0003C (Acton WS) at Q/A 232-33. Thus, to the extent that the preamble of claim 1 is a limitation, the [] SoC meets this element.

Broadcom Br. at 194.

Respondents do not clearly rebut this argument. *See generally* Resps. Br. at 57; Resps. Reply at 30-31 (contesting limitations [A], [C] and [D]).

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The evidence shows that the [] decodes digital media, as described by the preamble. *See* CX-0003C (Acton WS) at Q/A 232-33. Accordingly, the administrative law judge has determined that the [] satisfies the preamble.

b) Limitation [A]: a processor adapted to control a decoding process; and

Broadcom argues:

Claim 1 further requires “a processor adapted to control a decoding process.” To the extent it is determined that Broadcom’s proposed constructions are not limited as proposed by Respondents, Respondents do not appear to dispute that the [] practices this claim limitation.

The evidence shows that the [] SoC [

]. *Id.*

Broadcom Br. at 194-95. Under respondents’ construction, Broadcom argues:

As discussed above, Respondents’ proposed construction of the term “a processor adapted to control a decoding process” improperly narrows the claim term and should be rejected. Even if their claim construction is adopted, however, the evidence shows that the [] practices this limitation. [

]. *Id.*

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Id. at 198.

Respondents argue:

The [] SoC does not comprise “a processor adapted to control a decoding process” under either proposed construction. RX-1079C at Q151. Broadcom’s expert identifies [

]” Tr. (Acton) 122:2-5. But, Dr. Acton does not allege that any one of those processors meets this limitation, or explain how [] can satisfy a claim limitation that is directed to a single processor. RX-1079C at Q151-154.

No one of the [] controls the decoding process. *See id.* According to Dr. Acton’s identification of [],” the “decoding process” consists of the “[

]” CX-0003C at Q240. So limitation 1[a] is met only if those [] are controlled by the same processor. But Dr. Acton admits that none of the processors he identified controls all [] alleged “hardware accelerators.” [

]” (Tr. (Acton) 122:15-18)—the remaining four hardware accelerators are part of that “front-end hardware” and “back-end hardware.” Tr. (Acton) 123:12-23. Thus, no one of the processors identified by Broadcom’s expert controls or orchestrates the alleged “hardware accelerators.” RX1079C at Q152-155. Therefore, no one of the processors is “a core decoder processor designed to orchestrate decoding for each pipeline stage” under Respondents’ construction. *Id.*

Resps. Br. at 57 (footnote omitted).

The evidence shows that [] constitute “a processor adapted to control a decoding process.” *See* CX-0003C (Acton WS) at Q/A 237; CX-0051C at 8. [

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].” *Id.*

Dr. Stevenson’s testimony [], and concludes that neither can be the claimed processor because neither [] controls every function:

[

].”

RX-1079C (Stevenson RWS) at Q/A 153-54.

While the core decoder processor must orchestrate decoding for each pipeline stage, [] constitute the central control unit of the [] decoding system.

Accordingly, the [] satisfies this limitation.

c) ***Limitation [B]: a hardware accelerator coupled to the processor and***

Broadcom argues:

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Claim 1 further requires “a hardware accelerator coupled to the processor.” Respondents appear to concede that the [] practices this claim limitation under Broadcom’s proposed constructions.

The evidence shows that the [] SoC contains a plurality of hardware accelerators, such as [

], each of which are adapted to perform a decoding function on a digital media data stream. CX-0003C (Acton WS) at Q/A 240-48.

Broadcom Br. at 195.

Respondents do not clearly rebut this argument. *See generally* Resps. Br. at 57-58 (limitation [B] is skipped); Resps. Reply at 30-31 (contesting limitations [A], [C] and [D]).

The evidence shows that the [] includes a hardware accelerator coupled to the processor, as described by limitation [B]. *See* CX-0003C (Acton WS) at Q/A 240-48.

Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

d) *Limitation [C]: adapted to perform a decoding function on a digital media data stream,*

Broadcom argues:

Claim 1 further requires “a hardware accelerator ... adapted to perform a decoding function on a digital media stream.” Respondents appear to concede that the [] practices this claim limitation under Broadcom’s proposed constructions. The evidence shows that each hardware accelerator performs its respective decoding function “on a digital media data stream” by performing their associated decoding functions on the elementary stream data of the transport stream. CX-0003C (Acton WS) at Q/A 240-48.

Broadcom Br. at 195-96.

Respondents argue:

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The [] does not comprise “a hardware accelerator . . . adapted to perform a decoding function on a digital media data stream.” RX-1079C at Q156. *First*, the alleged hardware accelerators of the [] SoC cannot “assist” the [] in decoding, as Dr. Acton does not opine that the [] within the [] performs decoding functions. RX-1079C at Q158; CX-0003C at Q228-230. *Second*, the alleged “hardware accelerators” (*i.e.*, []

[]) do not perform a decoding function on a transport stream. RX-1079C at Q158. Dr. Acton responds that “the [] hardware is practicing this claim limitation because they are processing the digital media data, specifically the elementary stream data, within the transport stream.” CX-0003C at Q248. But processing an elementary stream is not the same as processing a transport stream. RX-1079C at Q158. Thus, the [] alleged “hardware accelerators” do not perform a decoding function on a transport stream. *Id.*

Resps. Br. at 58. Dr. Stevenson’s testimony in Q/A 158 opines that “[] SoC does not practice this limitation under Respondents’ proposed constructions.” RX-1079C (Stevenson RWS) at Q/A 158.

Broadcom replies:

Respondents do not dispute that the [] hardware accelerators perform their respective decoding functions on the elementary stream data, which is extracted from the incoming transport stream. RPostHB at 58. Regardless of the construction adopted for the term “digital media data stream,” the [] practices this claim limitation.

Broadcom Reply at 63.

Respondents reply:

With respect to limitation 1[c], Broadcom continues to argue the alleged “hardware accelerators” of the [] decode elementary stream data. CPostHg. Br. 199. Elementary stream data can be carried in a transport stream, but that data is parsed from the transport stream before it is input to the alleged “hardware accelerators.” RX-1079C at Q158. The fact that elementary stream data might have been encapsulated in a

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transport stream, does not mean that it is forever thereafter a transport stream, regardless of how it is subsequently modified. *Id.* Thus, the five alleged “hardware accelerators” in the [] do not perform a decoding function on a transport stream.

Resps. Reply at 30-31.

The evidence shows that the [] includes a hardware accelerator that decodes a digital media data stream, as described by limitation[C]. *See* CX-0003C (Acton WS) at Q/A 240-48. Respondents’ argument is premised on limiting “a digital media stream” to a transport stream, which the administrative law judge previously declined to do.

- e) ***Limitation [D]: wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.***

Broadcom argues:

Lastly, claim 1 requires “wherein the accelerator is configurable to perform a decoding function according to a plurality of decoding methods.” To the extent it is determined that Broadcom’s proposed constructions are not unduly limited as Respondents have proposed, it appears undisputed that the [] practices this claim limitation.

The [] SoC’s hardware accelerators each satisfy this limitation of the claim. CX-0003C (Acton WS) at Q/A 249-55. Each hardware accelerator is configurable to perform the decoding function according to a plurality of video encoding standards, and each of the various video encoding standards dictates its own unique method for encoding and thus requires a unique decoding method. *Id.* Accordingly, each hardware accelerator performs a decoding function according to a plurality of decoding methods. *Id.*

Broadcom Br. at 196.

Respondents argue:

The [] SoC does not practice limitation 1[d] with respect to the [] because, as previously discussed, the [] does not configure any of the alleged “hardware accelerators.” RX-1079C at Q162. Rather, the []

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is only capable of communicating with the [redacted], neither of which is a “hardware accelerator.” *Id.* Thus, the [redacted] does not configure aspects internal to any of the alleged “hardware accelerators.” *Id.*

As discussed with respect to limitation 1[a] the [REDACTED] and [REDACTED] only communicate with a subset of the alleged “hardware accelerators.” The [REDACTED] is only capable of communicating with the [REDACTED], therefore, the remaining [REDACTED] alleged “hardware accelerators” cannot be “hardware accelerators” with respect to the [REDACTED]. See Tr. (Acton) 122:19-21; see also RX-1079C at Q162. Conversely, the [REDACTED] is not capable of communicating with the [REDACTED], therefore, it cannot be a “hardware accelerator” with respect to the [REDACTED]. See Tr. (Acton) 122:15-18, 123:12-23; see also RX-1079C at Q162. “At bottom, no processor that controls the decoding process also configures each of the purported hardware accelerators”. RX-1079C at Q162.

Broadcom's expert also failed to show that the alleged "hardware accelerators" are "configurable to perform the decoding function according to a plurality of decoding methods." RX-1079C at Q162. For example, Dr. Acton opined that the "[redacted] hardware accelerator is configurable to perform its decoding functions according to a plurality of encoding standards" and identifies "[redacted]."

[redacted]. CX-0003C at Q250. But he failed to provide any indication of what [redacted]. RX-1079C at Q162. Moreover, he failed to demonstrate that the [redacted]."

Id.

Resps. Br. at 59-60.

The evidence shows that the [] includes a hardware accelerator that is configurable to perform decoding per multiple decoding methods, as described by limitation [D]. See CX-0003C (Acton WS) at Q/A 249-55. The [] hardware accelerators are configurable to perform the decoding function according to a plurality of video encoding standards, and each video encoding standards utilizes a unique method for encoding, and thus

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requires a unique decoding method. *Id.* Thus, each hardware accelerator performs a decoding function according to a plurality of decoding methods. *Id.*

Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

2. Claims 2-4, 6, 7, and 9-13

Broadcom's entire argument is:

The evidence shows that the [] practices each of dependent claims 2-4, 6, 7, and 9-13, when those claims are properly construed as proposed by Broadcom. CX-0003C (Acton WS) at Q/A 256-58, 263, 264, 266-75. With respect to claims 2-4, 6, 7, and 9-13, Respondents do not present any arguments other than those presented for independent claim 1. Accordingly, if the [] is found to practice claim 1, it also practices dependent claims 2-4, 6, 7, and 9-13.

Broadcom Br. at 196.

Respondents do not clearly rebut this argument. *See generally* Resps. Br. at 60 (respondents contest "limitation 5[a]" and "limitation 8[a]"); Resps. Reply at 30-31 (contesting claims 1 and 8 only).

The administrative law judge has determined that if the [] is found to practice claim 1 (as is the case herein), it also practices dependent claims 2-4, 6, 7, and 9-13. *See* CX-0003C (Acton WS) at Q/A 256-58, 263, 264, 266-75.

3. Claim 5

Claim 5 follows:

5. The digital media decoding system of claim 1 wherein the processor is adapted to perform decoding functions on a digital media data stream and wherein the hardware accelerator is adapted to assist the processor in performing a decoding function on the digital media data stream, wherein the accelerator is configurable to assist the processor according to a plurality of decoding methods.

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JX-0001 at 20:62-67.

Broadcom argues:

... Each of the [] satisfy the “processor is adapted to perform decoding functions on a digital media data stream” limitation of claim 5. CX-0003C (Acton WS) at Q/A 260. In addition, each of the [] satisfy the “wherein the hardware accelerator is adapted to assist the processor in performing a decoding function on the digital media data stream” limitation of claim 5. *Id.* at Q/A 261. Each of the [] also satisfy the “wherein the accelerator is configurable to assist the processor according to a plurality of decoding methods” limitation of claim 5. *Id.* at Q/A 262.

Broadcom Br. at 196-97.

Respondents argue:

[], or any other Broadcom SoC, does not practice a “processor [that] is adapted to perform decoding functions on a digital media data stream,” as can be found in limitation 5[a]. RX-1079C at Q165. Dr. Acton’s analysis is incorrect under this claim for at least the same reasons explained above regarding the claims from which this claim depends. *Id.* Further, as shown in Dr. Acton’s Witness Statement in response to Q260, Dr. Acton does not opine that []

[] of the stream type or informing them that information is available for decoding does not constitute “decoding functionality.” *Id.*

Resps. Br. at 60.

The evidence shows that the [] includes a processor is adapted to perform decoding functions on a digital media data stream, as claim 5 requires. *See* CX-0003C (Acton WS) at Q/A 260-62. Further, the [] also includes a hardware accelerator that is adapted to assist the processor in performing a decoding function on the digital media data stream, wherein the accelerator is configurable to assist the processor according to a plurality of

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decoding methods. *Id.* Respondents' argument is premised on limiting "a digital media stream" to a transport stream, which the administrative law judge previously declined to do.

Accordingly, the administrative law judge has determined that the [] practices claim 5 (assuming claim 1 is practiced).

4. Claim 8

Claims 7 and 8 follow:

7. The digital media decoding system of claim 1 wherein the processor is adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded.

8. The digital media decoding system of claim 7 wherein the accelerator includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator and wherein the processor programs the registers or the memory in order to configure the accelerator.

JX-0001 at 20:48-57.

Broadcom argues:

Claim 8 of the '844 Patent depends from dependent claim 7 and further requires either "a set of registers" or "memory coupled to an internal processor" that dictates operational parameters of the accelerator and wherein the processor programs the registers or the memory in order to configure the accelerator. In the [

] CX-0003C (Acton WS) at Q/A 265. Thus, the evidence shows that the [] practices claim 8.

Broadcom Br. at 197.

Respondents argue:

[], or any other Broadcom SoC, does not comprise an "accelerator [that] includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator" RX-1079C at Q166.

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Broadcom's expert failed to show that any of the purported accelerators "includes . . . an internal processor." *Id.* at Q167. Nor has Broadcom's expert shown that any of [

] in Broadcom's products are internal to any of the purported hardware accelerators. *Id.* For this additional reason, Broadcom's expert has not shown that the purported "hardware accelerators" practice limitation 8[a]. *Id.*

Resps. Br. at 60.

The evidence shows that the [] includes a processor that programs the hardware accelerators' registers, which dictate operational parameters such as the decoding standard associated with the encoded video. CX-0003C (Acton WS) at Q/A 265. Accordingly, the administrative law judge has determined that the [] practices claim 8 (assuming claim 1 is practiced).

F. Anticipation – Reader

Respondents argue that U.S. Patent No. 6,192,073 ("Reader") (RX-0317) "anticipates and/or renders obvious claims 1-13 of the '844 Patent." Resps. Br. at 63. Respondents also argue that:

[Reader] was filed on August 19, 1996, and issued on February 20, 2001, and therefore, it is prior art to the '844 Patent under 35 U.S.C. § 102(b). RX-0383C.0021 (Stevenson) Q68. As discussed below, because the MSP-1EX appendices A and B [RX-0318] were part of the Reader patent application in the Reader File History, they were publically available when the Reader patent issued.

Resps. Br. at 61.

Broadcom argues that the appendices are not a part of Reader and are not publically available:

Respondents have failed to prove that the appendices mentioned in the Reader Patent are part of the Reader Patent because they are not incorporated by reference into the Reader Patent. *See* CX-0579C (Acton WS) at Q/A 36. Respondents contend that the

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appendices mentioned in the Reader Patent, for example “Appendix A,” which is the MSP-1EX appendix (RX-0319), should be included as part of the Reader Patent (RX-0317). However, the MSP-1EX is merely mentioned in the Reader Patent, and not identified using any detailed particularity, and not expressly incorporated by reference. *See generally* RX-0317. A “mere *reference* to another application, or patent, or publication is not an *incorporation* of anything therein.” *Callaway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1346 (Fed. Cir. 2009) (quoting *In re De Seversky*, 474 F.2d 671, 674 (C.C.P.A. 1973)) (emphasis in original).

...

The Appendices mentioned in Reader cannot be combined with Reader because Respondents simply point to the fact that the appendices are in the Reader Patent’s file history. Respondents have failed, however, to prove that they were publicly available prior to the ‘844 Patent’s priority date of April 1, 2002. Simply showing that the Reader appendices are in the file history of the Reader Patent as it exists now, is not adequate to prove that they were publicly available prior art under 35 U.S.C. §102. For example, the Federal Circuit has held that part of a copyright application, available to the public on request, did not constitute a printed publication (for Patent prior art purposes) merely because someone who knew of its existence and relevance could have requisitioned it. *In re Lister*, 583 F.3d 1307, 1313-14 (Fed. Cir. 2009). Thus, Respondents have failed to show that the Appendices were publicly available.

Broadcom Br. at 205.

The administrative law judge has determined that Reader, including its appendices, are prior art under 35 U.S.C. § 102(b). Reader issued more than one year before the ‘844 Patent’s earliest filing date, and the appendices appear in the file history. *See* RX-0318 at 19, 207 (Appendices A and B, respectively). Further, Reader explicitly references the MSP-1EX specification, which is Appendix A. *See* RX-0317 at 3:19-24 (“In some embodiments, processor 110 is a type MSP-1EX (Trademark) processor whose specification is produced at Samsung

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Semiconductor Corporation of San Jose, Calif. Processor MSP-1EX is described in Appendix A below.”).

1. Claim 1

a) [Preamble]: A digital media decoding system comprising:

Respondents argue:

Reader discloses a “digital media decoding system.” RX-0383C (Stevenson) Q78; RDX-0007.0001-0009. The MSP-1EX system decodes video data. RX-0383C (Stevenson) Q78; RX-0317 (‘073 Reader Patent) at 1:15-34; Fig. 1; RX-0318 (MSP-1EX Appendices A and B) at Fig. 1, Pg. A-1 – A-2. Broadcom and its expert, Dr. Acton, do not dispute this limitation is met by Reader.

Resps. Br. at 66.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 201 (contesting hardware-accelerator and digital-media-data-stream limitations); Broadcom Reply, Section III(D) (same).

The evidence and argument cited in respondents’ brief shows that Reader discloses a digital media decoding system as described in the preamble. *See, e.g.*, RX-0383C (Stevenson) Q/A 78. Accordingly, the administrative law judge has determined that Reader discloses subject matter that satisfies the preamble.

b) Limitation [A]: a processor adapted to control a decoding process; and

Respondents argue:

Under all proposed constructions, Reader discloses “a processor adapted to control a decoding process.” RX-0383C.0024-0025 (Stevenson) Q81-86; RDX-0007.0009-0023. Reader discloses that the scalar processor (*i.e.*, ARM7 RISC processor) of the MSP-1EX system is the “master processor” and controls the decoding process. RX-0383C (Stevenson) Q81; RX-0317 (‘073 Reader Patent) at 1:15-34, 4:59-5:3, 5:23-36, 5:37-44; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-21, ¶ 3; Pg. A-24, ¶ 6; A-103,

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¶ 1; Pg. A-128, ¶ 3 – Pg. A-129. Broadcom and Dr. Acton do not dispute this limitation is met by Reader under any proposed construction. *See, e.g.*, CX-0579C.00013-00014 (Acton).

Respondents' Construction: The scalar processor is “a core decoder processor designed to orchestrate decoding for each pipeline stage.” RX-0383C.0024-0025 (Stevenson) Q84; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-21, ¶ 3; Pg. A-103, ¶ 1; Pg. A-128, ¶ 3 – Pg. A-129. The scalar processor de-multiplexes the audio-video signal, parses header data, and moves video and audio data to SDRAM before it is provided to the bitstream and vector processors. RX-0383C.0024-0025 (Stevenson) Q84; RX-0317 ('073 Reader Patent) at 5:23-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-131, ¶ 2. It also initializes and synchronizes the bitstream and vector processors. RX-0383C.0024-0025 (Stevenson) Q84; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-128, ¶ 3 – Pg. A-129; Pg. A-131, ¶ 3; Pg. A-141, ¶ 3. The scalar, bitstream, and vector processors form each of the pipeline stages of the decoding process. RX-0317 ('073 Reader Patent) at 1:14-34.

Complainant's Construction: For these same reasons, the scalar processor also satisfies Complaint's construction—plain and ordinary meaning. RX-0383C.0024 (Stevenson) Q85.

Resps. Br. at 66-67.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 201 (contesting hardware-accelerator and digital-media-data-stream limitations); Broadcom Reply, Section III(D) (same).

Having considered the parties' arguments, the administrative law has determined that Reader includes a processor adapted to control a decoding process, as described in claim 1. *See* RX-0383C (Stevenson WS) at Q/A 81-86. Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Reader discloses a processor—the scalar processor—that satisfies this limitation.

c) ***Limitation [B]: a hardware accelerator coupled to the processor and***

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Respondents argue:

Reader discloses “a hardware accelerator coupled to the processor.” RX-0383C (Stevenson) Q87-88; RDX-0007.22-43. Reader discloses two distinct hardware accelerators (bitstream processor and the vector processor) coupled to the scalar processor through cache subsystem 230 and/or IOBUS 240, as shown in Fig. 2. RX-0383C (Stevenson) Q87; RX-0317 (‘073 Reader Patent) at Fig. 2, 4:18-34; RX-0318 (MSP-1EX Appendices A and B) at Fig. 2, A-5, ¶ 3 – Pg. A-6, ¶ 3.

Respondents’ Construction: Each is “specialized hardware that assists the processor by accelerating decoding functions.” RX-0383C (Stevenson) Q89. “Scalar processor 210, vector processor 220 and bitstream processor 245 can operate on different blocks of data in parallel.” RX-0317 (‘073 Reader Patent) at 5:23-36. “Video data processing is divided between scalar processor 210, vector processor 220 and bitstream processor 245 so as to achieve a high processing speed.” RX-0383C.0026 (Stevenson) Q89; RX-0317 (‘073 Reader Patent) at 4:59-5:3.

The bitstream processor is a “specialized hardware logic block” that assists the scalar processor by performing the decoding functions of zig-zag bitstream processing and Huffman decoding. RX-0383C. (Stevenson) Q89; RX-0317 (‘073 Reader Patent) at 5:23-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-42, ¶ 2-3, Pg. A-122, ¶ 1 – Pg. A-123 (“Bitstream processor . . . is a specialized hardware logic block . . .”). Dr. Acton does not dispute that the bitstream processor of Reader satisfies limitation 1[b]. RX-0383C.0026 (Stevenson) Q90; CX-0579C.00014 (Acton) at Q47.

Similarly, the vector processor is a specialized DSP engine that assists the scalar processor by performing the decoding functions of dequantization, inverse discrete cosine transform, motion compensation, and post processing, such as smoothing edges of picture images. RX-0383C (Stevenson) Q91; RX-0317 (‘073 Reader Patent) at 5:10-11; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-24, ¶ 7 - Pg. A-25, ¶ 1 (“The Vector Processor is the DSP engine of the MSP.”), Pg. A-53, ¶ 1 - Pg. A-54, Pg. A-132, ¶¶ 1-2.

Dr. Acton opined, for the first time at a very late stage in this Investigation, that a vector processor is a coprocessor and thus is not the claimed hardware accelerator. RX-0383C.0026-0027 (Stevenson) Q93; CX-0003C.0009-0012. As discussed in § B.2,

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supra, however, the intrinsic evidence clearly contradicts Dr. Acton's purported distinction. A coprocessor can be a hardware accelerator, and the vector processor is such an accelerator. *See* RX1079C.0008-09 (Stevenson) Q32-45.

Complainant's Construction: For these same reasons, each of the bitstream processor and vector processor satisfies this limitation under Complainant's construction—plain and ordinary meaning. RX-0383C.0026 (Stevenson) Q92. Regarding Complainant's alternative construction, each is “a hardware component that performs one or more operations separately from the processor to perform decoding faster than the processor alone.” Each is separated from the scalar processor by buses and/or the cache subsystem, and each processes video data “so as to achieve a high processing speed.” RX-0383C.0026 (Stevenson) Q92; RX-0317 ('073 Reader Patent) at 4:59-5:3; 5:23-36.

Resps. Br. at 67-69.

Broadcom argues that Reader's vector processor “is not a ‘hardware accelerator’ because it is a DSP and co-processor” and Reader's bitstream processor “is not a hardware accelerator because it is a processor.” Broadcom Br. at 202-203 (citing CX-0579C (Acton RWS) at Q/A 47).

Respondents reply that the '844 Patent's specification explicitly discloses hardware accelerators comprising processors. Resps. Reply at 32 (quoting JX-0001 at 19:64-20:2 (“some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/decoding formats . . .”)).⁴⁹

⁴⁹ The entire citation of '844 Patent states:

In another illustrative embodiment, some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors, in addition to programming registers as appropriate to the design.

JX-0001 at 19:64-20:2.

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The evidence shows that Reader includes hardware accelerators—the vector and bitstream processors—that perform decoding operations separately from the processor in order to increase decoding speed. *See* RX-0383C (Stevenson WS) at Q/A 87-93; RX-0317 at Fig. 2, 4:18-34, 4:59-5:36 (*e.g.*, “Scalar processor 210, vector processor 220 and bitstream processor 245 can operate on different blocks of data in parallel.”); RX-0318 (Reader Appendix) at Fig. 2, A-5, ¶ 3 – Pg. A-6, ¶ 3. Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Reader discloses hardware accelerators—the vector and bitstream processors—that satisfy this limitation.

d) *Limitation [C]: adapted to perform a decoding function on a digital media data stream,*

Respondents argue:

Reader discloses limitation 1[c]. RX-0383C (Stevenson) Q95-98; RDX-0007.0049-0068. Each of the bitstream processor and vector processor performs a decoding function. *Id.* The bitstream processor performs the decoding functions of zig-zag bitstream processing and Huffman decoding. RX-0383C (Stevenson) Q89; RX-0317 (‘073 Reader Patent) at 5:23-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-42, ¶ 2-3, Pg. A-122, ¶ 1 – Pg. A-123. The vector processor performs the decoding functions of dequantization, IDCT, motion compensation, and post processing. RX-0383C.0026 (Stevenson) Q91; RX-0317 (‘073 Reader Patent) at 5:4-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-24, ¶ 7 – Pg. A-25, ¶ 1, Pg. A-53, ¶ 1 - Pg. A-54, Pg. A-132, ¶¶ 1-2.

And each performs decoding on a digital media data stream. The bitstream processor supports “various bit streams,” and the vector processor can receive and process the output of the bitstream processor. RX-0383C (Stevenson) Q95; RX-0317 (‘073 Reader Patent) at 4:50-58, 5:23-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-123, ¶ 1, Pg. A-132, ¶ 2.

Respondents’ Construction: The vector processor may also optionally, in the video conferencing setting, process received data first. RX-0383C (Stevenson) Q96; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-131. In this optional scenario also, the streams would include transport streams. RX-0383C

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(Stevenson) Q98. Indeed, video conferencing usually occurs over a network, and Dr. Acton admits that transport streams, as opposed to program streams, are used to transport audio and video over a network. CX-0003 (Acton) at Q23. Thus, the vector processor would process an audio-video data stream received over a network – a transport stream. RX-0383C (Stevenson) Q96.

Alternatively, Reader in view of Fandrianto '459 renders this limitation obvious. . . .

Complainant's Construction: For the same reasons as stated above, each of the bitstream processor and vector processor also satisfies this limitation under Complainant's construction—plain and ordinary meaning. RX-0383C.0027-0028 (Stevenson) Q103.

Resps. Br. at 69-70.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 201 (contesting hardware-accelerator and digital-media-data-stream limitations); Broadcom Reply, Section III(D) (same).

Having considered the parties' arguments, the administrative law has determined that Reader includes a hardware accelerator that is adapted to perform a decoding function, as described in claim 1. *See* RX-0383C (Stevenson WS) at Q/A 95-98. Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Reader discloses a processor that satisfies this limitation.

e) Limitation [D]: wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.

Respondents argue, in part:

Reader discloses this limitation. RX-0383C.0029-0032 (Stevenson) Q105; RDX-0007.0068-0108. Each of the bitstream processor and vector processors is configurable to perform a decoding function according to a plurality of decoding methods under all proposed constructions. RX-0383C.0031 (Stevenson) Q111.

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Resps. Br. at 70. Respondents further argue that Reader's scalar processor "configures the bitstream processor by initializing its internal registers, programming through Huffman tables" and that the scalar processor "can configure the vector processor through co-processor instructions, which are loaded into memory of the vector processor and which specify the standard format of the data being decoded." *Id.* at 70, 72. Dr. Stevenson relies on Reader and its appendices

With respect to the vector processor, Broadcom argues, in part:

Reader's vector processor is not "configurable to perform the decoding function according to a plurality of decoding methods" because it simply chooses from a plurality of distinct software decoder modules, which was clearly excluded as being "configurable" in the prosecution history of the '844 Patent. *See* CX-0579C (Acton WS) at Q/A 57-58. During prosecution of the '844 Patent, the BPAI rejected the argument that system in the Sullivan reference (RX-258) discloses a hardware accelerator that "is configurable to perform the decoding function according to a plurality of decoding methods" because it was Sullivan's software API, running on a processor, that configures the system by picking and choosing particular hardware components that are each non-configurable, that is, they perform specific functions for specific video standards. JX-0004.3406-11 ('844 Patent Prosecution History). Dr. Acton testified that a system that performs simple path selection does not include configurable components because the benefits of a configurable system, for example, conservation of resources, are not gained by having the path selection system. *See* CX-0579C (Acton WS) at Q/A 58. Like the system of Sullivan, the software in Reader's vector processor simply chooses from several video-format specific and non-configurable components. Specifically, Reader's vector processor is designed to choose specifically designed software subroutines to assist in decoding. RX-0319 (MSP-1EX Appendix) at A-31. Each subroutine is dedicated to particular video format and is independently non-configurable. *Id.* The prosecution history to the '844 Patent makes clear that this simple path selection process does not disclose a "configurable" hardware accelerator

Reader's vector processor in combination with the BP_Mode register of Reader's bitstream processor is not "configurable to perform the decoding function according to a plurality of decoding

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methods” because the proposed combination does not remedy the fact that the vector processor simply chooses from a plurality of distinct software decoders, which is not “configurable.” *See* CX-0579C (Acton WS) at Q/A 58.

Broadcom Br. at 202-03.

With respect to the bitstream processor, Broadcom argues, in part:

Additionally, Reader’s bitstream processor is not configurable. Considering the Reader Patent disclosure only, the bitstream processor is not “configurable to perform the decoding function according to a plurality of decoding methods” because the Reader Patent does not explicitly or inherently disclose how the bitstream processor performs the decoding operations for the various video data formats. *See id. at* Q/A 59. As discussed in detail below, the Reader Appendix, MSP-1EX, should not be considered as a part of the Reader Patent and cannot be combined with the Reader Patent because it was not publicly available. Dr. Acton explained that neither Dr. Stevenson nor the Reader specification explains how the bitstream processor is a configurable hardware accelerator. *Id.* Further, Dr. Stevenson cites the bitstream processor’s registers to support configurability but the Reader Patent fails to explain how the registers are used or what information is provided in those registers. CX-0579C (Acton WS) at Q/A 59. Reader’s specification discusses that the bitstream processor “can handle” decoding various standards but does not explain how this is done. *Id.* (citing RX-0317 (Reader) at 4:50-58).

Id. at 204.

Respondents reply, in part, that “Rather, Reader’s vector processor is the hardware accelerator, and unlike Sullivan’s fixed hardware accelerators, the vector processor is configured by the DSP subroutines.” Resps. Reply at 33 (citing RX-0383C (Stevenson WS) at Q/A 107; RX-0318.0047-49 (MSP-1EX Appendices A and B) at Pg. A-29 – A-31, Table 6; RPreHg. Br. at Exhibit 1.09; RX-0317 at 1:43-56).

The administrative law judge has determined that respondents have not shown, though clear and convincing evidence, that the vector processor is configurable, as claim 1 requires. *See* CX-0579C (Acton RWS) at Q/A 58. In particular, the vector processor chooses from several

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video-format specific and non-configurable components rather than being internally programmed by the processor to perform its decoding function according to a plurality of decoding methods.

Id.

The evidence does show, however, that Reader's bitstream processor is internally programmable by the scalar processor to perform a decoding function according to a plurality of decoding methods. *See* RX-0383C (Stevenson WS) at Q/A 105. As Dr. Stevenson explains:

With regard to the bitstream processor, Reader discloses that the scalar processor configures the bitstream processor by initializing its internal registers. [*See* RX-0317 (Reader) at 5:45-54; RX-0318 (Reader) at Pg. A-128, ¶ 3 – Pg. A-129; Pg. A-131, ¶ 3; Pg. A-134; Pg. A-141, ¶ 3]. In particular, one of the internal registers of the bitstream processor is called “BP_Mode.” [*See* RX-0318 (Reader) at Pg. A-136]. Reader describes that “this register is to denote the video standard type.” *Id.* Three bits within the register correspond to the “standard_format,” which is defined in Table 26 of Reader. [*See* RX-0318 (Reader) at Pg. A-141 – A-142]. In Table 26, Reader describes values of bites corresponding to MPEG-1 video decoding (“001”), MPEG-2 video decoding (“011”), H.261 decoding (“101”), H.263 decoding (“111”). [*See* RX-0318 (Reader) at Pg. A-142]. Reader describes that the scalar processor should always specify the standard format before the bitstream processor is enabled for all video encoding and decoding applications. [*See* RX-0318 (Reader) at Pg. A-141]. After the “BP_Mode” register of the bitstream processor is initiated by the scalar processor, Reader discloses that the bitstream processor alters its behavior to match the specific standard. For example, Reader discloses the bitstream processor supports “all Huffman tables which are recommended in MPEG-1, MPEG-2, H.261, and H.263 video standards.” [*See* RX-0318 (Reader) at Pg. A-173, ¶ 1]. Different Huffman decoding tables are coded to shared memory. [*See* RX-0317 (Reader) at Abstract]. The tables can be implemented in lookup tables, which are summarized in Table 41 of Appendix A and Table 1 of Appendix B of the MSP-1EX Appendix of Reader. [*See* RX-0318 (Reader) at Pg. A-173, ¶ 1; B-1]. As shown in Tables 41 and 1, different Huffman tables correspond to different standards. [*See* RX-0318 (Reader) at Pg. A-174, Table 41; Pg. B-3, Table 1]. The “BP_Mode” register informs the bitstream processor's selection of different Huffman tables for different standards. [*See* RX-0318 (Reader) at Pg. B-2]. In particular, using the “mode” input signal, along with other input

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signals such as “table type” and “VLC/value,” an address generator generates the address of the appropriate ROM table. [See RX-0318 (Reader) at Pg. B-2]. Using the appropriate table, Reader discloses that decoded data can be derived by the bitstream processor from the Huffman table values. [See RX-0318 (Reader) at Pg. B-2]. This description in Reader is similar to the ‘844 patent’s description of configuring the PVL D at column eight lines 36 through 51, where the PVL D “includes a register that the core processor can program to guide the PVL D 306 to search for the VLC table of the appropriate encoding/decoding algorithm.”

RX-0383C (Stevenson WS) at Q/A 105.

Broadcom and Dr. Acton’s argument excludes the appendices. *See, e.g.*, Broadcom Br. at 204 (“Considering the Reader Patent disclosure only, the bitstream processor is not . . . “); CX-0579C (Acton RWS) at Q/A 59 (“If Reader does not include the appendices, then Dr. Stevenson provides only two citations . . . “). Thus, Broadcom and Dr. Acton have not rebutted Dr. Stevenson’s testimony.

Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Reader’s bitstream processor (inclusive of the discussion in the appendices) is a configurable accelerator that satisfies this limitation.

2. Claim 2

Claim 2 follows:

2. The digital media decoding system of claim 1 wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding standards.

JX-0001 at 20:24-26.

Respondents argue:

Reader and/or Reader-Fandrianto disclose claim 2 for the same reasons as element 1[d]. RX-0383C.0032 (Stevenson) Q115; RDX-0007.0108.

Resps. Br. at 75.

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For claims 2-13, Broadcom argues:

Claims 2-13 are not invalid in view of the asserted prior art for the same reasons provided for claim 1. *Id. at* Q/A 34-119. Claim 4 is not invalid in view of the asserted prior art for the same reasons provided for claim 3. *Id. at* Q/A 76-79. Claim 8 is not invalid in view of the asserted prior art for the same reasons provided for claim 7. *Id. at* Q/A 92-95. Claim 10 is not invalid in view of the asserted prior art for the same reasons provided for claims 3 and 9. *Id. at* Q/A 100-101. Claim 11 is not invalid in view of the asserted prior art for the same reasons provided for claims 9 and 10. *Id. at* Q/A 102-111. Claims 12 and 13 are not invalid in view of the asserted prior art for the same reasons provided for claims 9, 10, and 11. *Id. at* Q/A 112-115.

Broadcom Br. at 210. In Q/A 62-65, Dr. Acton opines that “Reader does not disclose claim 2 for the same reasons that I discussed with respect to claim 1.” CX-0579C (Acton RWS) at Q/A 62-65.

The administrative law judge previously determined that Reader anticipates claim 1. The administrative law judge determines that respondents have shown, through clear and convincing evidence, that Reader anticipates claim 2 based upon the same evidence and analysis relied upon in discussing claim 1. *See* RX-0383C (Stevenson WS) at Q/A 115-16.

3. Claim 3

Claim 3 follows:

3. The digital media decoding system of claim 1 comprising a plurality of hardware accelerators coupled to the processor, each accelerator adapted to perform a decoding function on a digital media data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods.

JX-0001 at 20:27-33.

Respondents argue:

Reader and/or Reader-Fandrianto disclose “a plurality of hardware accelerators coupled to the processor.” RX-0383C (Stevenson)

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Q117; RDX-0007.0108-0114. The combination of the bitstream processor and vector processor is a plurality of hardware accelerators coupled to the scalar processor. RX-0383C (Stevenson) Q87, Q117; RX-0317 ('073 Reader Patent) at Fig. 2, 4:18-34; RX-0318 (MSP-1EX Appendices A and B) at Fig. 2, A-5, ¶ 3 – Pg. A-6, ¶ 3.

Resps. Br. at 75.

Broadcom argues:

Reader (the Patent alone or in combination with the appendices) or Reader in combination with Bailey does not disclose or renders obvious claims 3 and 10, which require a “plurality of hardware accelerators coupled to the processor, ... wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods.” *Id. at* Q/A 66-75, 100-101. The vector processor is not a configurable hardware accelerator and, thus, Reader does not disclose or render obvious a plurality of configurable hardware accelerators. *Id. at* Q/A 67. As discussed above for claim 1, the bit stream processor is not a configurable hardware accelerator and, thus, Reader does not disclose or render obvious a plurality of configurable hardware accelerators. *Id. at* 73; *see e.g.*, RX-0317 (Reader) at 1:42-56; 4:6-17; 4:13, Fig. 3; RX-0319 (MSP-1EX Appendix) at A-124.

Broadcom Br. at 206-07.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that both the vector and bitsream processors are configurable. In particular, as discussed in relation to claim 1, respondents have not shown the vector processor is configurable. Accordingly, the administrative law judge has determined that Reader does not anticipate claim 3.

4. Claim 4

Claim 4 follows:

4. The digital media decoding system of claim 3 wherein the hardware accelerators are configurable to perform their associated decoding functions according to a plurality of decoding standards.

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JX-0001 at 20:34-37.

Respondents' entire argument is: "**Claim 4:** *See* claims 1 and 3. RX-0383C (Stevenson) Q127; RDX-0007.0114-0115." Resps. Br. at 77.

Broadcom argues "Claim 4 is not invalid in view of the asserted prior art for the same reasons provided for claim 3." Broadcom Br. at 210.

The administrative law judge previously determined Reader does not anticipate claim 3. Accordingly, the administrative law judge determines that Reader does not anticipate claim 4 based upon the same evidence and analysis relied upon in discussing claims 1 and 3.

5. Claim 5

Claim 5 follows:

5. The digital media decoding system of claim 1 wherein the processor is adapted to perform decoding functions on a digital media data stream and wherein the hardware accelerator is adapted to assist the processor in performing a decoding function on the digital media data stream, wherein the accelerator is configurable to assist the processor according to a plurality of decoding methods.

JX-0001 at 20:38-44.

Respondents argue:

Limitation 5[a]: Reader and/or Reader-Fandrianto disclose "the processor is adapted to perform decoding functions on a digital media data stream." RX-0383C Q129; RDX-0007.0115-0121. Reader discloses that the scalar processor performs video processing, picture level processing, and demultiplexing. RX-0383C Q130; RX-0317 ('073 Reader Patent) at 1:14-34; 4:59-5:3; 5:4-22; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-131, ¶ 2; A-187, ¶ 1. The scalar processor "demultiplexes the system data into video and audio components, and performs sequence layer, GOP, and picture layer decoding of the video data." RX-0383C.0035 (Stevenson) Q129; RX-0317 ('073 Reader Patent) at 5:23-36; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-131, ¶ 2; A-187, ¶ 1. These are decoding functions performed by the scalar processor on a digital media data stream.

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RX-0383C.0035 (Stevenson) Q130. Dr. Acton does not dispute this.

Limitation 5[b]: *See* element 1[c]. RX-0383C.0035 (Stevenson) Q131.

Limitation 5[c]: *See* element 1[d]. RX-0383C.0036 (Stevenson) Q132.

Resps. Br. at 77.

Broadcom argues: “Claims 2-13 are not invalid in view of the asserted prior art for the same reasons provided for claim 1.” Broadcom Br. at 210. Dr. Acton’s testimony also relies upon the same opinions he presented in relation to claim 1. *See* CX-0579C (Acton RWS) at Q/A 80-83.

The administrative law judge determined that Reader anticipates claim 1. Broadcom has not presented an independent argument as to why claim 5 is also not anticipated. *See, e.g.*, CX-0579C (Acton WS) at Q/A 81 (“For all the reasons that I discussed previously with respect to claim 1, it is my opinion that Reader alone or in combination with the cited secondary references does not anticipate or render obvious claim 5.”). Moreover, as noted above, respondents have set forth independent evidence as to why claim 5 is anticipated.

Accordingly, the administrative law judge has determined that Reader anticipates claim 5.

6. Claim 6

Claim 6 follows:

6. The digital media decoding system of claim 1 wherein the accelerator is configurable to perform the decoding function on digital media data streams of a plurality of formats.

JX-0001 at 20:45-47.

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Respondents' entire argument is: "*See* element 1[d]. RX-0383C.0036 (Stevenson) Q134; RDX-0007.0121-0122." Resps. Br. at 78.

Broadcom argues: "Claims 2-13 are not invalid in view of the asserted prior art for the same reasons provided for claim 1." Broadcom Br. at 210. Dr. Acton's testimony also relies upon the same opinions he presented in relation to claim 1. *See* CX-0579C (Acton RWS) at Q/A 84-87.

The administrative law judge determined that Reader anticipates claim 1. Broadcom has not presented an independent argument as to why claim 6 is also not anticipated. *See, e.g.,* CX-0579C (Acton WS) at Q/A 85 ("For all the reasons that I discussed previously with respect to claim 1, it is my opinion that Reader alone or in combination with the cited secondary references does not anticipate or render obvious claim 6."). Accordingly, the administrative law judge has determined that Reader anticipates claim 6.

7. Claim 7

Claim 7 follows:

7. The digital media decoding system of claim 1 wherein the processor is adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded.

JX-0001 at 20:48-51.

Respondents' entire argument is: "*See* element 1[d]. RX-0383C.0036 (Stevenson) Q136; RDX-0007.0122." Resps. Br. at 78.

Broadcom argues:

The Reader Patent does not disclose "the processor is adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded," as required by claim 7 . . . because the Reader Patent does not disclose that the

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scalar processor configures the vector processor or the bitstream processor. [CX-0579C (Acton RWS)] at Q/A 89, 117.

Broadcom Br. at 207.

Broadcom has not presented an independent argument as to why claim 7 is also not anticipated. Moreover, the administrative law judge previously determined that Reader's bitstream processor discloses limitation [D] of claim 1. Dr. Acton's testimony, CX-0579C (Acton RWS) at Q/A 89, 117, excludes the bitstream processor, as it is discussed in the appendices. Accordingly, the administrative law judge has determined that Reader anticipates claim 7.

8. Claim 8

Claim 8 follows:

8. The digital media decoding system of claim 7 wherein the accelerator includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator and wherein the processor programs the registers or the memory in order to configure the accelerator.

JX-0001 at 20:58-61.

Respondents argue:

Limitation 8[a]: Reader and/or Reader-Fandrianto disclose "the accelerator includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator." RX-0383C (Stevenson) Q138; RDX-0007.0122-0123. For example, by co-processor instructions and/or configuring registers (as described above), each of the bitstream processor and vector processor is internally programmable by the scalar processor to perform a decoding function according to a plurality of decoding standards. *Id.*; RX-0317 ('073 Reader Patent) at 1:43-56, 2:17-25, 5:45-54; RX-0318 (MSP-1EX Appendices A and B) at Pg. A-21, Pg. A-29 – A-31, Table 6, Pg. A-128, ¶ 3 – Pg. A-129; Pg. A-131, ¶ 3; Pg. A-134; Pg. A-141, ¶ 3. Further, as shown in Fig. 3, the bitstream processor has an internal core unit, which includes a register file, and as discussed for limitation 1[d], the BP_Mode register specifies the standard

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format, which informs the bitstream processor's decoding operations, such as derivation of Huffman tables. RX-0383C (Stevenson) Q138, Q105; RX-0317 ('073 Reader Patent) at Fig. 3; RX-0318 (MSP-1EX Appendices A and B) at Pg. B-2. Similarly, the scalar processor can configure the vector processor through co-processor instructions to load subroutines into memory of the vector processor to adapt to the standard of the data being decoded. RX-0383C.0025-0026, -0030; RX-0317 ('073 Reader Patent) at Fig. 11, 2:17-25; RX-0318 (MSP-1EX Appendices A and B) at Fig. 11, Pg. A-21, A-128, Pg. A-132, ¶ 1-2. Thus, both satisfy element 8[a].

Limitation 8[b]: *See* elements 1[d] and 8[a]. RX-0383C (Stevenson) Q140.

Resps. Br. at

Broadcom argues that "Claim 8 is not invalid in view of the asserted prior art for the same reasons provided for claim 7." Broadcom Br. at 210.

Broadcom has not presented an independent argument as to why claim 8 is also not anticipated. Moreover, the administrative law judge determined that Reader anticipates claim 7. Accordingly, the administrative law judge has determined that Reader anticipates claim 8.

9. Claim 9

Claim 9 follows:

9. The digital media decoding system of claim 1 wherein the digital media decoding system is a video decoding system and wherein the hardware accelerator is adapted to perform the decoding function on a video data stream.

JX-0001 at 20:58-61.

Respondents' entire argument is:

Limitation 9[a]: *See* element 1[pre]. RX-0383C (Stevenson) Q142; RDX-0007.0123.

Limitation 9[b]: *See* element 1[c]. RX-0383C (Stevenson) Q143; RDX-0007.0124.

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Resps. Br. at 78-79.

Broadcom argues: “Claims 2-13 are not invalid in view of the asserted prior art for the same reasons provided for claim 1.” Broadcom Br. at 210. Dr. Acton’s testimony also relies upon the same opinions he presented in relation to claim 1. *See* CX-0579C (Acton RWS) at Q/A 97 (“For all the reasons that I discussed previously with respect to claim 1, it is my opinion that Reader alone or in combination with the cited secondary references does not anticipate or render obvious claim 9.”).

The administrative law judge determined that Reader anticipates claim 1. Broadcom’s brief does not present an independent argument as to why claim 9 is also not anticipated. *See* Broadcom Br. at 210 (claim 9 is not mentioned). Accordingly, the administrative law judge has determined that Reader anticipates claim 9.

10. Claim 10

Claim 10 follows:

10. The video decoding system of claim 9 comprising a plurality of hardware accelerators coupled to the processor, each accelerator adapted to perform a decoding function on the video data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods.

JX-0001 at 20:62-67.

Respondents’ entire argument is: “*See* claims 1, 3, and 9. RX-0383C (Stevenson) Q145; RDX-0007.0124-0125.” Resps. Br. at 79.

Broadcom argues that “Reader (the Patent alone or in combination with the appendices) or Reader in combination with Bailey does not disclose or renders obvious claims 3 and 10[.]” Broadcom Br. at 206-07.

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The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that both the vector and bitsream processors are configurable. In particular, as discussed in relation to claim 1, respondents have not shown the vector processor is configurable. Accordingly, the administrative law judge has determined that Reader does not anticipate claim 10.

11. Claim 11

Claim 11 follows:

11. The video decoding system of claim 10 wherein the plurality of hardware accelerators comprise: a programmable entropy decoder adapted to perform entropy decoding on the data stream; an inverse quantizer adapted to perform inverse quantization on the data stream; an inverse transform accelerator adapted to perform inverse transform operations on the data stream; a pixel filter adapted to perform pixel filtering on the data stream; and a motion compensator adapted to perform motion compensation on the data stream.

JX-0001 at 20:24-26.

Respondents' entire argument is:

See claims 1, 3, and 10. RX-0383C (Stevenson) Q146; RDX-0007.0125-0145.

Limitation 11[a]: *See* claims 1, 3, and 10. RX-0383C.0038 (Stevenson) Q146.

Limitation 11[b]: *See* claims 1, 3, and 10. RX-0383C.0038 (Stevenson) Q148.

Limitation 11[c]: *See* claims 1, 3, and 10. RX-0383C.0038 (Stevenson) Q150.

Limitation 11[d]: *See* claims 1, 3, and 10. RX-0383C.0038 (Stevenson) Q152.

Resps. Br. at 79.

Broadcom argues, in part:

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As stated above, neither the vector processor nor bitstream processor of Reader is a configurable hardware accelerator. And, even if the vector processor and bitstream processor are considered to be configurable hardware accelerators, neither of them includes a pixel filter, which is required by claim 11.

Reader does not disclose “a pixel filter adapted to perform pixel filtering on the data stream.” Dr. Stevenson points to generic filtering but the claimed “pixel filter” is a specific type of filter that is not described in Reader. *Id.* at Q/A 107, 111 (citing RX-0383C (Stevenson WS) at Q/A 152, 153). Dr. Stevenson points to Reader’s disclosures of smoothing edges and an FIR filter and argues that it is a pixel filter. RX-0383C (Stevenson WS) at Q/A 152. But this is generic filtering, not a pixel filter. The ‘844 Patent’s “pixel filter” is more than a general filter: “The pixel filter 310 performs the interpolation necessary when a reference block is translated (motion-compensated) by a vector that cannot be represented by an integer number of whole-pixel locations.” JX-0001 (‘844 Patent) at 11:16-19. Accordingly, Reader does not disclose, and Dr. Stevenson does not provide any arguments, that the Reader system includes a pixel filter, as described in the ‘844 Patent. *See* CX-0579C (Acton WS) at Q/A 107.

Broadcom Br. at 208.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Reader discloses “a pixel filter adapted to perform pixel filtering on the data stream.” In particular, the evidence that Dr. Stevenson cites does not clearly disclose a pixel filter, and Dr. Stevenson has not sufficiently shown that the vector processor or the MSP-1EX can also satisfy this limitation. Accordingly, the administrative law judge has determined that Reader does not anticipate claim 11.

12. Claim 12

Claim 12 follows:

12. The video decoding system of claim 11 wherein the plurality of hardware accelerators further comprise a de-blocking filter adapted to perform de-blocking operations on the data stream.

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JX-0001 at 20:24-26.

Respondents' entire anticipation argument is: "See claims 1, 3, 10 and 11. RX-0383C (Stevenson) Q156." Resps. Br. at 80. Dr. Stevenson testifies:

Q156. Does Reader disclose claim 12?

A156. Yes. Reader discloses "the plurality of hardware accelerators further comprise a de-blocking filter adapted to perform de-blocking operations on the data stream." Reader alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious claim 12 for the same reasons it discloses and/or renders obvious limitation 11[d]. To the extent Reader does not anticipate this claim, it would have been obvious to modify Reader with Fandrianto to arrive claim 12 for the same reasons it would have been obvious to modify Reader with Fandrianto to meet limitation 11[d].

RX-0383C (Stevenson WS) at Q/A 156.

Broadcom argues:

Reader does not disclose "a de-blocking filter adapted to perform de-blocking operations on the data stream" because Dr. Stevenson points to his discussion of claim limitation 11[d], which is the pixel filter claim limitation, as his support for claim 12. *Id.* at Q/A 112-115. However, claim 12 requires a "deblocking filter" and claim limitation 11[d] requires a "pixel filter." JX-0001 ('844 Patent) at Claim 11, 12. These are different filters and Dr. Stevenson does not explain how his discussion in claim 11[d] applies to claim 12's recited limitation. Accordingly, Reader does not anticipate or render obvious claim 12. *See* CX-0579C (Acton WS) at Q/A 112-115.

Dr. Stevenson's discussion with respect to the combination of Reader and Fandrianto fails to provide anything more than a conclusory sentence that there would be an expectation of success in modifying Reader in combination with Fandrianto. *Id.* at Q/A 113. As stated above in the discussion of claim 11, this is insufficient. *Id.*

Broadcom Br. at 209-10.

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The administrative law judge determined that Reader does not anticipate claim 11. Respondents' argument simply references claim 11; respondents do not advance any new argument. Accordingly, the administrative law judge has determined that Reader does not anticipate claim 12.

13. Claim 13

Claim 13 follows:

13. The digital media decoding system of claim 11 wherein the processor is adapted to configure each of the accelerators to perform the decoding function according to a format of the media data to be decoded.

JX-0001 at 20:24-26.

Respondents' entire anticipation argument is: "See claims 1, 3, 10 and 11. RX-0383C (Stevenson) Q158." Resps. Br. at 80.

The administrative law judge determined that Reader does not anticipate claim 11. Respondents' argument simply references claim 11; respondents do not advance any new argument. Accordingly, the administrative law judge has determined that Reader does not anticipate claim 13.

G. Anticipation – Fandrianto

Respondents argue that U.S. Patent No. 5,982,459 to Fandrianto et al. ("Fandrianto") (RX-0324) "anticipates and/or renders obvious claims 1-13 of the '844 Patent under all constructions." Resps. Br. at 85. Respondents also argue that Fandrianto "qualifies as prior art to the '844 Patent under 35 U.S.C. § 102(b) because was filed on June 11, 1997 and issued on November 9, 1999." *Id.* at 63.

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Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-16 (discussing Fandrianto without disputing its prior-art status); Broadcom Reply, Section III(D) (same).

Accordingly, the administrative law judge has determined that Fandrianto is prior art under 35 U.S.C. § 102(b).

1. Claim 1

a) [Preamble]: A digital media decoding system comprising:

Respondents argue:

Fandrianto discloses a “digital media decoding system.” RX-0383C at Q164; RDX-0008.00002-00007. Fandrianto discloses a multimedia system that decodes video and audio data in compliance with H.261, MPEG-1, MPEG-2, or custom proprietary compression standards. RX-0383C at Q164; see RX-0324 (Fandrianto) at Fig. 1-2, 3:21-22; 4:13-21.

Dr. Acton did not dispute that Fandrianto’s system is a digital media decoding system that satisfies limitation 1[pre]. RX-0383C at Q165.

Resps. Br. at 86.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-13 (contesting hardware-accelerator and digital-media-data-stream limitations); Broadcom Reply, Section III(D) (same).

The evidence and argument cited in respondents’ brief shows that Fandrianto discloses a digital media decoding system as described in the preamble. *See, e.g.*, RX-0383C (Stevenson) Q/A 164. Accordingly, the administrative law judge has determined that Fandrianto discloses subject matter that satisfies the preamble.

b) Limitation [A]: a processor adapted to control a decoding process; and

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Respondents argue:

Fandrianto discloses “a processor adapted to control a decoding process” under all proposed constructions. RX-0383C.0042-0043 at Q166; RDX-0008.00007-8. The RISC processor 220 supervises the processing resources – such as the Huffman and H.221/BCH decoders – for input of compressed data, error correction, parsing of bit streams, and separating audio and video data to form a bit stream. RX-0383C at Q166; *see* RX-0324 (Fandrianto) at 4:21-37, 4:64-5:10. The RISC processor 220 also downloads subroutines for and activates the video processor 280 by writing to a command processor 960 of the video processor to enable the video processor to decode video data of different standards. RX-0383C at Q166; *see* RX-0324 (Fandrianto) at 4:64-5:10; 12:64-13:11. Thus, the RISC processor is a processor adapted to control a decoding process. *Id.*

Dr. Acton does not dispute that VCP system is a digital media decoding system that satisfies limitation 1[a] under any construction. RX-0383C at Q165.

Respondents’ Construction: The RISC processor 220 is “a core decoder processor designed to orchestrate decoding for each pipeline stage.” RX-0383C at Q169. As discussed, the RISC processor 220 “supervises hardware resources for input and output of compressed [audio and video] data,” including “supervis[ing] operation[s] of [the] VCP,” as well as Huffman codec 260 and H.221/BCH decoder 240. *Id.*; *see* RX-0324 (Fandrianto) at 4:21–22, 5:14–15, 9:19–28. It also downloads subroutines for the video processor, activates it, and passes data to it. RX-0383C at Q169; *see* RX-0324 (Fandrianto) at 12:62-13:11. Thus, it orchestrates decoding for the pipeline stages (*i.e.*, video processor and hardware resources). RX-0383C at Q169.

Complainant’s Construction: For these same reasons, the RISC processor also satisfies Complaint’s construction—plain and ordinary meaning. RX-0383C at Q170.

Resps. Br. at 86-87.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-13 (contesting hardware-accelerator and digital-media-data-stream limitations); Broadcom Reply, Section III(D) (same).

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The evidence and argument cited in respondents' brief shows that Fandrianto discloses a processor adapted to control a decoding process, as described in claim 1. *E.g.*, RX-0383C (Stevenson) Q/A 164. Accordingly, the administrative law judge has determined that Fandrianto discloses a processor—the RISC processor (220)—that satisfies this limitation.

c) Limitation [B]: a hardware accelerator coupled to the processor and

Respondents argue:

Fandrianto discloses “a hardware accelerator coupled to the processor.” RX-0383C at Q171; RDX-0008.00008-00011. Fandrianto discloses at least three hardware accelerators: the video processor 280, the Huffman codec 260, and the H.221/BCH decoder 240. RX-0383C at Q171; *see* RX-0324 (Fandrianto) at 1:47-62; 9:13-22; 11:40-47; 12:48-63. The three hardware accelerators are connected to the RISC processor through data buses 204 and 294, a portal 250, and/or memory 284, which can be seen on Figure 2 of the patent. RX-0383C at Q171; *see* RX-0324 (Fandrianto) at Fig. 2, 5:11-32, 12:5-38.

Respondents' Construction: Each of the video processor, Huffman codec and H.221/BCH decoder implements “specialized” decoding tasks. RX-0383C at Q173; *see* RX-0324 (Fandrianto) at 1:47-62. The video processor 280 is a specialized signal processor that performs certain decoding functions (discussed further in limitation 1[c]) to assist the RISC processor. RX-0383C at Q173; *see* RX-0324 (Fandrianto) at 1:47-62 and 12:48-63. Similarly, the Huffman codec 260 is a specialized block that helps the RISC processor 220 process data and perform decoding. RX-0383C at Q173; *see* RX-0324 (Fandrianto) at 9:13-22, 11:40-47. The H.221/BCH decoder 240 is also a specialized block that also helps the RISC processor 220 parse and process data. RX-0383C at Q173; *see* RX-0324 (Fandrianto) at 4:64-5:10; 9:13-22. Thus, each is “specialized hardware that assists the processor by accelerating decoding functions.” RX-0383C at Q173.

Complainant's Construction: For these same reasons, each of the hardware accelerators also satisfies Complaint's construction—plain and ordinary meaning. *Id.* at Q175. Regarding Complainant's alternative construction, each of the video processor, Huffman codec, and H.221/BCH decoder performs decoding functions separate from the RISC processor 220 to

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decode faster. *Id.* This can be seen visually in Figure 2, which shows these components are separate from the RISC processor 220. *Id.*

Dr. Acton does not dispute the Huffman codec and H.221/BCH decoder are hardware accelerators under any construction. *Id.* at Q176. Dr. Acton, however, similar to his opinion for Reader, opines that “the video processor is not a ‘hardware accelerator’ because it is a programmable DSP co-processor.” *Id.* at Q174. But, as discussed with respect to the vector processor of Reader and in the claim construction section, hardware accelerators can be coprocessors. *Id.*; see § B.2, *supra*.

Resps. Br. at 87-88.

With regard to the video processor, the H.221/BCH decoder, and the Huffman decoder, Broadcom argues that:

- “Fandrianto’s video processor is not a ‘hardware accelerator’ because it is a programmable DSP co-processor, which the ‘844 Patent specification clearly excludes from being a ‘hardware accelerator.’” Broadcom Br. at 211.
- “Fandrianto’s H.221/BCH decoder is not the claimed hardware accelerator because the H.221/BCH decoder sub-components Dr. Stevenson cites either (1) do not perform a decoding function or (2) are not configurable.” Broadcom Br. at 211.
- “Fandrianto’s Huffman decoder is not ‘configurable to perform the decoding function according to a plurality of decoding methods’ because it only includes the relevant decoding table for a single standard at any given time and is not “configurable to perform the decoding function according to a plurality of decoding methods” as claimed in the ‘844 Patent.” Broadcom Br. at 212.

Dr. Acton’s testimony is limited to contesting the video processor:

Q122. Dr. Acton, please look at question and answer Q/A 171 in RX-0383C. Do you agree with Dr. Stevenson’s conclusion that “Fand[r]ianto ‘459 discloses at least three hardware accelerators: the video processor, the Huffman decoder, and the H.221/BCH decoder”?

A No. I disagree with Dr. Stevenson’s conclusion that the video processor is a hardware accelerator.

CX-0579C (Acton RWS) at Q/A 122.

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Having considered the parties arguments, the administrative law judge has determined that the video processor, the H.221/BCH decoder, and the Huffman decoder are hardware accelerators. *See* RX-0383C (Stevenson WS) at Q/A 173-76. Fandrianto's video processor (280) is a separate component that performs decoding operations separately from the RISC processor (220). *Id.*; *see also* RX-0324 at 1: 58-62 ("The video processor and associated hardware units performs video processing operations such as video scaling, DCT (discrete cosine transform), inverse DCT, temporal filtering, output interpolation, color conversion, and picture-in-picture."). Further, Dr. Acton does not dispute that the H.221/BCH decoder and the Huffman decoder are hardware accelerators. *See* RX-0383C (Stevenson WS) at Q/A 173; CX-0579C (Acton RWS) at Q/A 122. Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Fandrianto discloses hardware accelerators—the video processor, the H.221/BCH decoder, and the Huffman decoder—that satisfy this limitation.

d) Limitation [C]: adapted to perform a decoding function on a digital media data stream,

Respondents argue:

Fandrianto discloses "a hardware accelerator . . . adapted to perform a decoding function on a digital media data stream." RX-0383C at Q177; RDX-0008.00011-20. Each of the video processor 280, Huffman codec 260, and H.221/BCH decoder 240 performs a decoding function on a digital media data stream. RX-0383C at Q177. The video processor performs the decoding functions of motion estimation, loop filtering, inverse discrete cosine transform, inverse quantization, zigzag scanning, video scaling, temporal filtering, and output interpolation on a digital media data stream. RX-0383C at Q177; *see* RX-0324 (Fandrianto) at 1:47-62, 12:48-63. The Huffman codec 260 and H.221/BCH decoder 240 help the RISC processor process non-byte-aligned data structures of a digital media data stream. RX-0383C at Q177; *see* RX-0324 (Fandrianto) at 9:13-22, 11:40-47. And, the H.221/BCH decoder 240 also parses the digital media data stream

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by separating audio data from video data. RX-0383C at Q177; *see* RX-0324 (Fandrianto) at 4:64-5:10, 9:13-22. In addition, the Huffman codec 260 also performs variable length decoding on a digital media data stream. RX-0383C at Q177; *see* RX-0324 (Fandrianto) at 11:40-47. Each of the above is a decoding function. RX-0383C at Q177.

Dr. Acton opines, however, that the H.221/BCH decoder does not meet this limitation because it “only separates different data types (e.g., video and audio data) and does not perform any decoding (i.e., decompression) functions.” *Id.* at Q178; *see* Dr. Acton Rebuttal Report at ¶ 84. Separating video and audio data, however, is decoding. RX-0383C at Q178. Separating video and audio data is a form of parsing. *Id.* at Q178. Indeed, Fandrianto refers to the H.221/BCH decoder as a “H.221/BCH bit stream **parser/multiplexer 240**.” RX-0324 at 9:20 (emphasis added). And Fandrianto discloses that this type of parsing is decoding. *Id.* at 1:52-57 (“[A]ssociated hardware implement communications protocols for video conferencing, **perform bitstream parsing (decoding)** . . .”) (emphasis added). Dr. Acton also ignores the other functions that the H.221/BCH decoder performs, such as processing non-byte aligned data, which are also configurable decoding functions, as discussed *infra*. RX-0383C at Q178.

Respondents’ Construction: The H.221/BCH decoder can perform decoding functions on a transport stream. RX-0383C at Q180. In particular, Fandrianto discloses that the H.221/BCH decoder 240 separates audio data from video data of a digital media data stream. *Id.*; *see* RX-0324 (Fandrianto) at 4:64-5:10, 9:13-22. Because Fandrianto discloses use of its systems over a video conferencing **network**, one of ordinary skill would understand Fandrianto to disclose a transport stream. RX-0383C at Q102, Q180; RX-0324 (Fandrianto) at 2:63-3:9, 9:23-41; CX-0003C.0008 (Acton) at Q23 (“[T]ransport streams are used to package data such as audio and video **for transmission over a network**. . .”) (emphasis added).

Complainant’s Construction: For the reasons stated above, each of these hardware accelerators satisfies Complaint’s construction—plain and ordinary meaning. RX-0383C at Q181.

Resps. Br. at 88-90.

With regard to the H.221/BCH decoder Broadcom argues that:

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Dr. Stevenson points to “bit stream parser 510” (a sub-component of H.221/BCH decoder) as a structure that performs a decoding function. But Dr. Acton testified that the bit stream parser 510 does not perform a decoding function. Dr. Acton also testified that the “bit stream parser 510” only separates different data types, such as, video and audio data (*Id.* at Q/A 125), which the ‘844 Patent specification describes as processing the digital media data stream and not as a decoding function (JX-0001 (‘844 Patent) at 4:3-7).

Broadcom Br. at 211 (Broadcom’s arguments with respect to the video processor or the Huffman codec relate to limitation [D]).

Having considered the parties arguments, the administrative law judge has determined that the video processor, the H.221/BCH decoder, and the Huffman decoder are hardware accelerators that are adapted to perform a decoding function of a digital media stream. *See* RX-0383C (Stevenson WS) at Q/A 177. In particular, Dr. Stevenson testified that:

Fandrianto discloses that the video processor implements decoding functions on a digital media data stream. [*See* RX-0324 (Fandrianto) at 1:47-62, 12:48-63]. In addition, the Huffman codec and H.221/BCH decoder help the RISC processor process non-byte-aligned data structures of a digital media data stream. [*See* RX-0324 (Fandrianto) at 9:13-22, 11:40-47]. And, the H.221/BCH decoder separates audio data from video data of a digital media data stream. [*See* RX-0324 (Fandrianto) at 4:64-5:10, 9:13-22]. In addition, the Huffman codec performs variable length decoding on a digital media data stream. [*See* RX-0324 (Fandrianto) at 11:40-47].

Id. at Q/A 177.

In response, Dr. Acton argues that:

Dr. Stevenson also states that “Dr. Acton also ignores the other functions that the H.221/BCH decoder performs, such as processing non-byte aligned data.” However, as I stated in my expert report, to the extent that Dr. Stevenson tries to argue that the H.261 compliant H.221/BCH bit stream parser/multiplexer’s other components, which are the “H.261 frame alignment decoder 520” and a “BCH error detector 530,” disclose the limitations of claim 1, he would be wrong, because these components are dedicated to

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performing operations based on only the H.261 standard and, thus, are not configurable as required by claim 1.

CX-0579C (Acton RWS) at Q/A 125. Thus, Dr. Acton has not addressed Dr. Stevenson's opinion that the H.221/BCH decoder performs a decoding function. Further, Dr. Acton's response does not address the video processor or Huffman decoder.

Accordingly, the administrative law judge finds that respondents have shown, through clear and convincing evidence, that Fandrianto's hardware accelerators are adapted to perform a decoding function of a digital media stream.

- e) ***Limitation [D]: wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.***

Respondents argue:

Fandrianto discloses limitation 1[d]. RX-0383C at Q182; RDX-0008.00020-26. Each of the video processor, Huffman codec, and H.221/BCH decoder is configurable to perform a decoding function according to a plurality of decoding methods, and each satisfies limitation 1[d] under all proposed constructions. *Id.*

Respondents' Construction: Each of the video processor, Huffman codec, and H.221/BCH decoder "is internally programmable by the processor to perform its decoding function according to a plurality of decoding methods." RX-0383C at Q186. The RISC processor 220 can write to VCP registers that "control operation of the hardware input, output, and processing resources and [that] are distributed in video processor [] and various hardware resources ..." *Id.* at Q182; *see* RX-0324 (Fandrianto) at 4:21-44, 5:17-20. These hardware resources include the Huffman codec 260 and H.221/BCH decoder 240. For example, in H.221/BCH decoder 240, registers 514A and 514B contain templates, which indicate the formats of bytes in the bit stream to the H.221/BCH decoder 240 for the decoding functions of parsing and byte alignment. RX-0383C at Q182; *see* RX-0324 (Fandrianto) at Fig. 5, 9:42-54. The RISC processor 220 changes the templates according to the protocol being employed in the bit stream. *Id.* Thus, the H.221/BCH decoder 240 is internally configurable to perform a decoding function according to a plurality of decoding methods. *Id.*

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Similarly, the Huffman codec 260 uses look-up tables 716 and 726 to implement encoding and decoding. RX-0383C at Q183; *see* RX-0324 (Fandrianto) at 11:40-47. In particular, as shown in Fig. 7, look up table 716 is contained in memory located within the Huffman decoder. RX-0383C at Q183; *see* RX-0324 (Fandrianto) at Fig. 7, 11:40-47. The look-up tables can be modified to address changes in encoding standards – one of ordinary skill would have understood that different encoding standards utilize different Huffman tables. *Id.* In addition, the RISC processor can write to VCP registers distributed in the Huffman codec to inform it which standard is being decoded. RX-0383C at Q183; *see* RX-0324 (Fandrianto) at 4:21-44, 5:17-20, 9:13-22. Thus, the Huffman codec is internally configurable to perform a decoding function according to a plurality of decoding methods. *Id.*

Dr. Acton argues that the Huffman codec could determine the standard itself, but Dr. Acton provides no evidence that Fandrianto discloses anything other than the RISC Processor programming the Huffman codec. Further, Dr. Acton argues that the Huffman codec cannot decode more than one standard at a time, but nothing in the '844 Patent requires the hardware accelerators to decode two standards at once. Indeed, the '844 Patent discusses the same configuration scheme for the PVLD module, which is guided to an individual VLC table appropriate for the current decoding algorithm. *See* JX-0001 ('844 Patent) at 8:41-48.

Regarding the video processor 280, the RISC processor 220 loads software for the video processor 280 into RAM 282 and writes to a command processor 960 to activate the video processor 280. RX-0383C at Q184; *see* RX-0324 (Fandrianto) at 4:46-53; 12:64-13:11 ("On-chip SRAM 282 allows RISC processor 220 to download new subroutines for video processor 280. RISC processor 220 activates video processor 280 by writing to a command processor 960 which selects a subroutine from ROM 284 or RAM 282."). As is shown in Fig. 9, RAM 282 and the command processor 960 are both located within the video processor 280. RX-0383C at Q184; *see* RX-0324 (Fandrianto) at Fig. 9, 4:46-53, 12:64-13:11. In turn, the video processor 280 decodes video data by executing the stored software to perform video decompression operations required by different standards. RX-0383C at Q184; *see* RX-0324 (Fandrianto) at 4:46-53, 12:48-63. As discussed for Reader, above, loading different standard based instructions into the video processor is configuration, and not the "path selection" of Sullivan. *See* JX-0001 ('844 Patent) at 8:36-48.

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Thus, each of the three hardware accelerators disclosed by Fandrianto is internally programmable according to the protocol being employed in the bit stream. In sum, the RISC processor programs the internal registers of the H.221/BCH decoder. RX-0383C at Q186. The registers inform the H.221/BCH decoder's decoding operations, such as supplying templates indicating the formats of bytes in the bit stream that the decoder will parse and/or process. *Id.* Regarding the Huffman codec, the RISC processor changes lookup tables in the internal memory of the Huffman codec to decode video encoded according to different standards. *Id.* Finally, regarding the video processor, the RISC processor loads software into internal memory of the video processor. *Id.* The video processor executes the software to perform video decompression according to different standards or processes. *Id.*

Complainant's Construction: For the reasons stated above, each of the hardware accelerators satisfies Complaint's construction—plain and ordinary meaning. RX-0383C at Q187.

Resps. Br. at 90-92 (footnote omitted).

Broadcom's rebuttal and the administrative law judge's analysis are divided into separate sections for the video processor, H.221/BCH decoder, and Huffman codec.

(1) The video processor

Broadcom's entire argument with respect to the video processor is:

Also, under either Respondents' or Broadcom's proposed claim constructions, Fandrianto's video processor is not "configurable to perform the decoding function according to a plurality of decoding methods" because the video processor only includes the software for decoding a single video standard at any given time and thus is not "configurable to perform the decoding function according to a plurality of decoding methods" as claimed in the '844 Patent. *Id.* at Q/A 129.

Broadcom Br. at 211.

The administrative law judge has determined that respondents have shown, through clear and convincing evidence that the video processor is internally programmable by the processor to

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perform its decoding function according to a plurality of decoding methods. *See* RX-0383C

(Stevenson WS) at Q/A 184. Fandrianto explains:

Video processor 280 compresses or decompresses video data by executing software stored in on-chip RAM 282 and ROM 284. RISC processor 220 loads the software for video processor 280, from a host device or EPROM 158, into RAM 282 via portal circuit 250 and a DMA controller 296. An external memory 140 provides a frame buffer for data being compressed or decompressed. In one embodiment of the invention, memory 140 is a 2 Mbyte DRAM.

...

Video processor 280 is a programmable signal processor which implements video coding and decoding procedures such as motion estimation, loop filters, discrete cosine transforms (DCTs), inverse DCTs, and quantization, inverse quantization, and zig-zag scanning as may be required by a software selected video protocol. In particular, video processor 280 can execute software which performs video compression and decompression operations required by the MPEG, JPEG and H.261 standards as well as proprietary video compression processes. . . .

...

FIG. 9 shows a block diagram of an embodiment of video processor 280. Video processor 280 executes software which is stored in on-chip ROM 284 and RAM 282. On-chip ROM 284 is a 2 K.times.32 bit non-volatile memory containing subroutine commonly executed video processor 280. On-chip SRAM 282 allows RISC processor 220 to download new subroutines for video processor 280. RISC processor 220 activates video processor 280 by writing to a command processor 960 which selects a subroutine from ROM 284 or RAM 282. Command processor 960 contains a queue for a sequence of subroutines to be executed by video processor 280. A RISC core 940 and a sequencer 970 decode microcode instructions from the selected subroutine and control a data path 970 which implements the microcode instructions. RISC core 940 and data path 950 run until the subroutine is complete, then a next subroutine is performed.

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RX-0324 at 4:46-53, 12:48-57, 12:64-13:11. Thus, Fandrianto discloses that its video processor is internally programmable by the RISC processor to perform decoding according to the MPEG, JPEG, and H.261 standards.

Dr. Acton testified that:

... Fandrianto never states that the RISC processor must inform the video processor of the particular encoding standard. The RISC processor does not need to inform the video processor of the video's encoding standard, *because the system is set-up to decode a single standard at any given time*. Accordingly, at any particular time, Fandrianto's video processor is not configurable to perform the decoding function according to a plurality of decoding methods as it is limited to the decoding functions and methods stored in memory. . .

CX-0579C (Acton RWS) at Q/A 129 (emphasis added). Dr. Acton's testimony is not persuasive because claim 1 does not require the hardware accelerator to be configured to decode multiple standards "at any given time."

(2) H.221/BCH decoder

Broadcom's entire argument with respect to the H.221/BCH decoder is:

Dr. Stevenson points to "bit stream parser 510" (a sub-component of H.221/BCH decoder) as a structure that performs a decoding function. But Dr. Acton testified that the bit stream parser 510 does not perform a decoding function. Dr. Acton also testified that the "bit stream parser 510" only separates different data types, such as, video and audio data (*Id. at Q/A 125*), which the '844 Patent specification describes as processing the digital media data stream and not as a decoding function (JX-0001 ('844 Patent) at 4:3-7). To the extent that Dr. Stevenson tries to argue that the H.221/BCH decoder's other components, which are the "H.261 frame alignment decoder 520" and "BCH error detector 530," disclose the limitations of claim 1, he would be wrong, because these components are dedicated to performing operations based on only the H.261 standard and, thus, are not configurable as required by claim 1. *See CX-0579C (Acton WS) at Q/A 125.*

Broadcom Br. at 211-12.

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The administrative law judge has determined that respondents have shown, through clear and convincing evidence that the H.221 decoder is internally programmable by the processor to perform its decoding function according to a plurality of decoding methods. *See* RX-0383C (Stevenson WS) at Q/A 184. Fandrianto explains:

Registers 514A and 514B contain templates which indicate formats of bytes in the bit stream. In one embodiment of the invention, each bit in the bit stream corresponds to two bits in a template, and the two bits indicate whether the corresponding bit from the bit stream is video, audio, format, or user data. Two bits equal to 00b, 01b, 10b, or 11b respectively indicate a corresponding bit in the bit stream is video data, audio data, format data, or user data for RISC processor 220. RISC processor 220 changes templates 514A and 514B according to the protocol being employed in the bit stream. Bit stream parser 510 is particularly suited for H.221 but can also be applied in decoding bit streams according to other protocols.

RX-0324 at 9:42-54.

Dr. Acton testifies, in part, that:

Under either Respondents' or Broadcom's proposed claim constructions, it is my opinion that Fandrianto's "H.261 compliant H.221/BCH bit stream parser/multiplexer" is not "a hardware accelerator . . . adapted to perform a decoding function on a digital media data stream," because the "bit stream parser 510" only separates different data types, such as, video and audio data, and does not perform any decoding, that is, decompression, functions. . . .

CX-0579C (Acton RWS) at Q/A 125. Dr. Acton reaches this conclusion by construing "decoding" to exclude the separation of audio and video:

The '844 patent does not describe separating the audio and video as a decoding function, such as those listed at 4:55-65: "Fundamental functions exist that are common to most or all of these formats. Such functions include, for example, programmable variable-length decoding (VLD), arithmetic decoding (AC), inverse quantization (IQ), inverse discrete cosine transform (IDCT), pixel filtering (PF), motion compensation (MC), and de-blocking/de-ringing (loop filtering or postprocessing). . . .

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According to the present invention, these functions are accelerated by hardware accelerators.”

Id. (Q/A 125). Thus, Dr. Acton’s testimony is not persuasive, as it limits the term “decoding” to examples provided in the specification in order to avoid invalidity.

(3) The Huffman codec

Broadcom’s entire argument with respect to the Huffman codec is:

Fandrianto’s Huffman decoder is not “configurable to perform the decoding function according to a plurality of decoding methods” because it only includes the relevant decoding table for a single standard at any given time and is not “configurable to perform the decoding function according to a plurality of decoding methods” as claimed in the ‘844 Patent. *See* CX-0579C (Acton WS) at Q/A 126-127. Fandrianto’s description of the Huffman codec makes clear that the Huffman decoder section performs its operations without ever being informed of the video data’s particular encoding standard. *Id.* at Q/A 127. Dr. Acton testified that a hardware component that performs the same operation/method regardless of encoding standard cannot be said to be configurable to perform different decoding methods. *Id.* Additionally, the Huffman decoder is not “internally programmable by the processor,” which is required by Respondents’ proposed claim construction. *Id.*

Broadcom Br. at 212.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Fandrianto’s Huffman decoder is internally programmable by the RISC processor to perform its decoding function according to a plurality of decoding methods. *See* CX-0579C (Acton RWS) at Q/A 127. Dr. Stevenson testified as follows:

Q183. Does Fandrianto also disclose limitation 1[d] with respect to the Huffman decoder?

A183. Yes. The Huffman codec uses look-up tables 716 and 726 to implement decoding. [*See* RX-0324 (Fandrianto) at 11:40-47]. In particular, as shown in Fig. 7, look up table 716 is contained in

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memory located within the Huffman decoder 710. [See RX-0324 (Fandrianto) at Fig. 7, 11:40-47]. The look-up tables can be modified to address changes in encoding standards - a POSITA would have understood that different encoding standards utilize different Huffman tables. *Id.* In addition, the RISC processor can write to VCP registers distributed in the Huffman decoder. [See RX-0324 (Fandrianto) at 4:21-44, 5:17-20, 9:13-22].

RX-0383C (Stevenson WS) at Q/A 183. The passages of Fandrianto that Dr. Stevenson cites, however, do not clearly and convincingly show that the RISC processor programs the Huffman decoder. *See* CX-0579C (Acton RWS) at Q/A 127 (“... the Huffman decoder section performs its operations without ever being informed of the video data’s particular encoding standard by the RISC processor, or by any signal or information from the RISC processor.”).

Accordingly, the administrative law judge finds that respondents have not shown, through clear and convincing evidence, that Fandrianto’s Huffman codec is a configurable accelerator that satisfies this limitation.

In summary, the administrative law judge has determined that Fandrianto discloses subject matter that shows limitation [D] was known based upon Fandrianto’s video processor and H.221 decoder, but not the Huffman codec.

2. Claim 2

Respondents argue:

Fandrianto discloses claim 2 for the same reasons that Fandrianto discloses element 1[d] RX-0383C at Q188; RDX-0008.00027.

Resps. Br. at 92.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-16 (there is no argument for claim 2); Broadcom Reply, Section III(D) (same).

The administrative law judge previously determined that Fandrianto anticipates claim 1. The administrative law judge determines that respondents have shown, through clear and

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convincing evidence, that Fandrianto anticipates claim 2 based upon the same evidence and analysis relied upon in discussing claim 1. *See* RX-0383C (Stevenson WS) at Q/A 188.

3. Claim 3

Respondents argue:

Limitation 3[a]: Fandrianto discloses “a plurality of hardware accelerators coupled to the processor.” RX-0383C at Q189; RDX-0008.00027-00028. The H.221/BCH decoder, Huffman codec, and video processor are each a hardware accelerator coupled to the RISC processor. *Id.* Thus, the combination of these accelerators is a plurality of hardware accelerators coupled to the processor. *Id.*

Alternatively, multiple H.221/BCH decoders, Huffman codecs, and/or video processors could be coupled in parallel to increase throughput and performance. RX-0383C.0047-0048 (Stevenson) Q189. This would have been obvious to one of ordinary skill and would have been within their knowledge. *Id.*

Limitation 3[b]: Fandrianto discloses limitation 3[b] for the same reasons it discloses limitations 1[c] and 3[a]. RX-0383C at Q190.

Limitation 3[c]: Fandrianto discloses limitation 3[c] for the same reasons it discloses limitations 1[d] and 3[a]. RX-0383C at Q191.

Resps. Br. at 92-93.

Broadcom argues:

For the reasons discussed with respect to claim 1, Respondents have not shown by clear and convincing evidence that Fandrianto anticipates or renders obvious “a plurality of hardware accelerators coupled to the processor, each accelerator adapted to perform a decoding function on the video data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods” because (1) Fandrianto’s video processor is not a “hardware accelerator”; (2) Fandrianto’s video processor is not a hardware accelerator “configurable to perform [its] associated decoding functions according to a plurality of decoding methods”; (3) Fandrianto’s bit stream processor is not a hardware accelerator “adapted to perform a decoding function on the video data stream”; (4) Fandrianto’s bit stream processor is not a hardware accelerator “configurable to perform their associated decoding functions according to a

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plurality of decoding methods”; and (5) Fandrianto’s Huffman codec is not a hardware accelerator “configurable to perform their associated decoding functions according to a plurality of decoding methods.” [CX-0579C (Acton RWS)] at Q/A 122-129.

Broadcom Br. at 213.

The administrative law judge previously determined that Fandrianto’s video processor and H.221 decoder are hardware accelerators (per limitation [B]) that are configurable (per limitation [D]) and coupled to the RISC processor. Fandrianto’s video processor and H.221 decoder, in turn, constitute the “plurality of hardware accelerators coupled to the processor” as claim 3 requires. *See* RX-0383C (Stevenson WS) at Q/A 189-91. Fandrianto discloses limitations 3[b] and 3[c] for the same reasons it discloses limitations 1[a] and 1[c]. *Id.* Accordingly, the administrative law judge determines that respondents have shown, through clear and convincing evidence, that Fandrianto anticipates claim 3.

4. Claim 4

Respondents’ entire argument is:

Fandrianto discloses claim 4 for the same reasons it discloses claims 1 and 3. RX-0383C at Q192; RDX-0008.28.

Resps. Br. at 93.

Broadcom argues:

Claim 4 is not invalid in view of the asserted prior art for the same reasons provided for claim 3. [CX-0579C (Acton RWS)] at Q/A 134-135.

Broadcom Br. at 215.

The administrative law judge previously determined Fandrianto anticipates claim 3. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 4 based

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upon the same evidence and analysis relied upon in discussing claims 1 and 3. *See* RX-0383C (Stevenson WS) at Q/A 192.

5. Claim 5

Respondents argue:

Limitation 5[a]: Fandrianto discloses “the processor is adapted to perform decoding functions on a digital media data stream.” RX-0383C at Q193; RDX-0008.00028-00032. Fandrianto discloses that the RISC processor executes software for decoding of video signals. RX-0383C at Q193; RX-0324 (Fandrianto) at 6:45-49. For example, the Fandrianto discloses that the RISC processor and associated hardware “perform bit stream parsing (**decoding**) or construction (encoding), control audio processing and output, and transfer (**decoding**) or receive (encoding) video data to the video processor.” RX-0383C at Q193; RX-0324 (Fandrianto) at 1:47-62 (emphasis added). Thus, Fandrianto discloses that the RISC processor performing decoding functions, such as parsing. Dr. Acton also opined that parsing is decoding. RX-0383C.0048 (citing Dr. Acton Opening Report at ¶ 118-119).

Limitation 5[b]: Fandrianto discloses limitation 5[b] for the same reasons it discloses limitation 1[c]. RX-0383C.0048 (Stevenson) Q195.

Limitation 5[c]: Fandrianto discloses limitation 5[c] for the same reasons it discloses limitation 1[d]. RX-0383C.0048 (Stevenson) Q196.

Resps. Br. at 93.

Broadcom argues:

Fandrianto does not disclose or render obvious claim 5’s requirement that “the processor is adapted to perform decoding functions on a digital media data stream” because Fandrianto’s RISC processor does not perform any decoding functions. [CX-0579C (Acton RWS)] at Q/A 136-137. Fandrianto explains that the “RISC processor 220 supervises hardware resources” and does not perform any decoding functions. *Id.* at Q/A 137 (citing JX-0001 (‘844 Patent) at 4:21-24 and 5:14-16). While Fandrianto also states that “RISC processor 220 executes software for coding and decoding of audio and video signals” (RX-0324 (Fandrianto) at 6:45-49 and 13:1-11), Dr. Acton testified that the software’s

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decoding function are actual being performed in the video processor and not in the RISC processor. *See* CX-0579C (Acton WS) at Q/A 137.

Broadcom Br. at 214-15.

Having considered the parties' arguments, the administrative law judge has determined that Fandrianto discloses a processor that can perform decoding, per claim 5. *See* RX-0383C (Stevenson WS) at Q/A 193. In particular, Fandrianto explains that "RISC processor 220 executes software for coding and decoding of audio and video signals[.]" *Id.*; RX-0324 at 6:45-59. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 5.

6. Claim 6

Respondents argue:

Fandrianto discloses claim 6 for the same reasons it discloses limitation 1[d]. RX-0383C.0049 (Stevenson) Q197; RDX-0008.00032-00033.

Resps. Br. at 93-94.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-16 (there is no argument for claim 6); Broadcom Reply, Section III(D) (same).

The administrative law judge previously determined Fandrianto anticipates claim 1. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 6 based upon the same evidence and analysis relied upon in discussing claim 1. *See* RX-0383C (Stevenson WS) at Q/A 197.

7. Claim 7

Claim 7 follows:

7. The digital media decoding system of claim 1 wherein the processor is adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded.

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JX-0001 at 20:48-51.

Respondents argue:

Fandrianto discloses claim 7 for the same reasons it discloses limitation 1[d]. RX-0383C.0049 (Stevenson) Q198; RDX-0008.00033.

Resps. Br. at 93-94.

Broadcom argues:

Fandrianto does not disclose or render obvious “the processor is adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded” or “the processor is adapted to configure each of the accelerators to perform the decoding function according to a format of the media data to be decoded” because Fandrianto does not disclose that the RISC processor configures the video processor or the Huffman codec. *Id.* at Q/A 140-141, 154-155.

Broadcom Br. at 215.

The administrative law judge previously determined that Fandrianto’s video processor and H.221 decoder are hardware accelerators (per limitation [B]) that are configurable (per limitation [D]) and coupled to the RISC processor. Fandrianto’s video processor and H.221 decoder, in turn, constitute the “the processor . . . adapted to configure the accelerator to perform the decoding function according to a format of the media data to be decoded” as claim 7 requires. *See* RX-0383C (Stevenson WS) at Q/A 198. Dr. Acton’s testimony does not discuss the video processor or H.221 decoder. *See* CX-0579C (Acton RWS) at Q/A 140-41. Accordingly, the administrative law judge determines that respondents have shown, through clear and convincing evidence, that Fandrianto anticipates claim 7.

8. Claim 8

Respondents argue:

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Limitation 8[a]: Fandrianto discloses limitation 8[a] for the same reasons it discloses limitation 1[d]. RX-0383C at Q199; RDX-0008.00033-00034. Each accelerator includes registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator. RX-0383C at Q199. The video processor includes a RISC core 940 that decodes microcode instructions from the selected subroutine, Huffman codec has a control circuit coupled to the look up table memory, and H.221/BCH decoder includes bit sorter 513 coupled to the templates in the registers. *Id.*; *see* RX-0324 (Fandrianto) at Fig. 5, Fig. 9, 9:23-67, 12:63-13:11.

Limitation 8[b]: Fandrianto discloses limitation 8[b] for the same reasons it discloses limitations 1[d] and 8[a]. RX-0383C at Q200.

Resps. Br. at 94.

Broadcom argues “Claim 8 is not invalid in view of the asserted prior art for the same reasons provided for claim 7.” Broadcom Br. at 215.

The administrative law judge previously determined Fandrianto anticipates claim 7. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 8 based upon the same evidence and analysis relied upon in discussing claims 1 and 7. *See* RX-0383C (Stevenson WS) at Q/A 199-200.

9. Claim 9

Respondents argue:

Limitation 9[a]: The MSP-1EX appendix discloses limitation 9[a] for the same reasons it discloses limitation 1[pre]. RX-0383C at Q201; RDX-0008.00034-00036.

Limitation 9[b]: The MSP-1EX appendix discloses limitation 9[b] for the same reasons it discloses limitation 1[c]. RX-0383C at Q202.

Resps. Br. at 94.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 210-16 (there is no argument for claim 9); Broadcom Reply, Section III(D) (same).

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The administrative law judge previously determined Fandrianto anticipates claim 1. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 9 based upon the same evidence and analysis relied upon in discussing claim 1. *See* RX-0383C (Stevenson WS) at Q/A 201-02.

10. Claim 10

Respondents argue:

Fandrianto discloses claim 10. RX-0383C at Q203; RDX-0008.00036-00037. With the exception of being dependent on claim 9 and including the term “video,” claim 10 is identical to claim 3. Thus, for the same reasons that Fandrianto discloses claims 1, 3, and 9, it also discloses claim 10. RX-0383C.0049 at Q203.

Resps. Br. at 94.

Broadcom argues that “Claim 10 is not invalid in view of the asserted prior art for the same reasons provided for claims 3 and 9.” Broadcom Br. at 215.

The administrative law judge previously determined Fandrianto anticipates claims 1, 3, and 9. Accordingly, the administrative law judge determines that Fandrianto anticipates claim 10 based upon the same evidence and analysis relied upon in discussing claims 1, 3, and 9. *See* RX-0383C (Stevenson WS) at Q/A 203.

11. Claim 11

Respondents argue:

Fandrianto discloses claim 11. RX-0383C at Q204; RDX-0008.00037-00040.

Limitation 11[a]: *See* claims 1, 3, and 10. RX-0383C at Q204; RX-0324 (Fandrianto) at 11:40-47.

Limitation 11[b]: *See* claims 1, 3, and 10. RX-0383C at Q205; RX-0324 (Fandrianto) at 12:48-57.

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Limitation 11[c]: *See* claims 1, 3, and 10. RX-0383C. at Q206; RX-0324 (Fandrianto) at 12:48-57.

Limitation 11[d]: *See* claims 1, 3, and 10. RX-0383C at Q207; RX-0324 (Fandrianto) at 12:48-57, 16:33-40, 17:8-30.

Limitation 11[e]: *See* claims 1, 3, and 10. RX-0383C at Q208. The video processor performs motion estimation. *Id.*; *see* RX-0324 (Fandrianto) at 12:48-57. Motion estimation is used for motion compensation. RX-0383C.0050 at Q208. Dr. Acton admits this. CX-0003C.0007 (Acton) at Q21. Alternatively, limitation 11[e] would have been obvious to one of ordinary skill based on these disclosures. RX-0383C at Q208.

Resps. Br. at 95.⁵⁰

Broadcom argues:

Fandrianto does not describe any “pixel filter” functionality. *Id.* at Q/A 150-151. Dr. Stevenson only cites to various portions of Fandrianto that mention “filter” in general. *Id.* at Q/A 151. The ‘844 Patent’s “pixel filter” is not just a general filter: “The pixel filter 310 performs the interpolation necessary when a reference block is translated (motion-compensated) by a vector that cannot be represented by an integer number of whole-pixel locations.” *Id.* (citing JX-0001 (‘844 Patent) at 11:16-19). Dr. Acton testified that even if all of the components cited by Dr. Stevenson are configurable hardware accelerators, none of them explicitly or inherently include a pixel filter. *Id.*

Broadcom Br. at 215.⁵¹

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Fandrianto discloses “a pixel filter adapted to perform pixel filtering on the data stream,” as claim 11 requires. In particular, the evidence that Dr. Stevenson cites (*i.e.*, RX-0324 (Fandrianto) at

⁵⁰ Limitation 11[D] is “a pixel filter adapted to perform pixel filtering on the data stream[.]” RX-0383C (Stevenson WS) at Q/A 152.

⁵¹ Broadcom’s Reply does not specifically address claim 11.

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12:48-57, 16:33-40, 17:8-30) does not clearly disclose a pixel filter. Accordingly, the administrative law judge has determined that Fandrianto does not anticipate claim 11.

12. Claim 12

For claim 12, which depends from claim 11, respondents argue:

See claims 1, 3, and 10. RX-0383C at Q209; RX-0324 (Fandrianto) at 12:48-57, 16:33-40, 17:8-30, Table B8.

Resps. Br. at 95.

Broadcom argues that “Claims 12 and 13 are not invalid in view of the asserted prior art for the same reasons provided for claims 9, 10, and 11. [CX-0579C (Acton RWS)] at Q/A 152-153.” Broadcom Br. at 216.

The administrative law judge previously determined that respondents have not shown that Fandrianto anticipates claim 11, which requires a pixel filter. Accordingly, the administrative law judge finds that respondents have not shown Fandrianto anticipates claim 12 based on its dependency from claim 11.

13. Claim 13

For claim 13, respondents argue:

See claims 1, 3, 10 and 11. RX-0383C.51 (Stevenson) Q210; RDX-0008.0041.

Resps. Br. at 95.

Broadcom argues that “Claims 12 and 13 are not invalid in view of the asserted prior art for the same reasons provided for claims 9, 10, and 11. [CX-0579C (Acton RWS)] at Q/A 152-153.” Broadcom Br. at 216.

The administrative law judge previously determined that respondents have not shown that Fandrianto anticipates claim 11. Accordingly, the administrative law judge finds that

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respondents have not shown Fandrianto anticipates claim 13 based on its dependency from claim 11.

H. Anticipation – Diaz

Broadcom argues that “Respondents have not shown by clear and convincing evidence that claims 1-7, 9-11, and 13 of the ‘844 are invalid in view” of U.S. Patent No. 5,920,353 (“Diaz”) (RX-0323). Broadcom Br. at 216.

Respondents did not present any arguments based on Diaz, even though Dr. Stevenson opined that “the Diaz patent anticipates claims 1-7, 9-11, and 13 of the ‘844 patent[.]” *See generally* Resps. Br., Section IV(E); Resps. Reply, Section II(D); Joint Outline at 5; RX-0383C (Stevenson WS) at Q/A 216.

Accordingly, the administrative law judge finds that respondents have failed to show that Diaz anticipates any claims of the ‘844 Patent. *See* CX-0579C (Acton RWS) at Q/A 156-85.

I. Anticipation – Bakhmutsky

Broadcom argues “Respondents have not shown by clear and convincing evidence that claim 1 of the ‘844 Patent is invalid in view” of U.S. Patent No. 5,990,812 (“Bakhmutsky”) (RX-0322). Broadcom Br. at 222.

Respondents did not present any arguments based on Bakhmutsky, even though Dr. Stevenson opined that “the Bakhmutsky patent anticipates claims [*sic*] 1 of the ‘844 patent[.]” *See generally* Resps. Br., Section IV(E); Resps. Reply, Section II(D); Joint Outline at 5; RX-0383C (Stevenson WS) at Q/A 249.

Accordingly, the administrative law judge finds that respondents have failed to show that Bakhmutsky anticipates any claims of the ‘844 Patent. *See* CX-0579C (Acton RWS) at Q/A 186-191.

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J. Anticipation – Quasar Chip

Respondents argue:

The Quasar chips relevant to the '844 Patent include the Quasar EM8300 ([

J. During the hearing, Sigma admitted evidence conclusively establishing that both the EM8300 and the EM8475 Quasar chips constitute prior art to the '844 Patent.

Resps. Br. at 63. Respondents further argue:

Specifically, the sworn testimony of Sigma Engineer, Mr. Ignaszewski, confirms both chips were in use and publicly available prior to 2002. Mr. Ignaszewski (who has been employed by Sigma for over 20 years) worked extensively with the EM8300 chip in 1997 and 1998, and gained intimate knowledge of the design, function, and operation of the chip through his work on the chip's software. RX-0668C at Q5, 13-15, 29. According to his undisputed testimony, the EM8300 chip was publicly shown in 1998 at the Comdex trade show in Las Vegas, which he personally attended to answer technical questions from customers regarding the chip. *Id.* at Q16-18, 21. The EM8300 chip was sold as part of the Quasar product that included the printed circuit board and other components prior to the year 2000. *Id.* at Q16, 21. The EM8300 Sigma product, introduced in evidence as RPX-0005, also has a copyright date of 1998 on its printed circuit board. Mr. Ignaszewski likewise confirmed the EM8475—a successor to the EM8300 chip—was publicly available and in use no later than the fall of 2001. RX-0668C at Q34, 40-41. Similarly, the EM8475 Sigma product, introduced in evidence as RPX-0008, also illustrates the copyright date of 2001 on its printed circuit board. Because both chips were on sale and available to the public more than one year before the priority date for the '844 Patent, they qualify as prior art under at least 35 U.S.C. §§ 102(b) and/or 103(a). RX-0383C at Q258.

Id. at 96-97.

Broadcom argues, in part:

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Respondents fail to show by clear and convincing evidence that what they term the “Quasar Chip,” including both the “Quasar Chip” references and “Quasar Chip” system, anticipate and/or render obvious claims 1-4 and 6-10 of the ‘844 Patent, or that the “Quasar Chip” in combination with Fandrianto invalidates claims 1-4 and 6-10 of the ‘844 Patent. This is because the only “Quasar Chip” evidence Respondents have presented consists of four non-public documents that are internally inconsistent; untested demonstratives; and inventor testimony that is not only uncorroborated, but in fact inconsistent with the documentary evidence—and accordingly should be given no weight, if not excluded outright.

During discovery, Respondents produced four references. These four references consist of (1) “Quasar Chip Huffman,” which is RX-0325, (2) “Quasar Chip Motion,” which is RX-0326, (3) “EM8300 Block Diagram,” which is RX-0327, and (4) “EM8475/EM8476 Datasheet,” which is RX-0328 (collectively, the “Quasar Chip references”). The “Quasar Chip” references, however, fail to anticipate and/or render obvious claims 1-4 and 6-10 of the ‘844 Patent. Not only are these references not prior art because they were not publically available prior to the ‘844 Patent’s priority date, but they also all fail to disclose all of the recited limitations of claims 1-4 and 6-10. Thus, Respondents’ anticipation argument based on these references fails.

Broadcom Br. at 223-24.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8300 or EM8475 Quasar chips are prior art. Respondents rely on Mr. Michael Ignaszewski’s witness statement (RX-0668C), the EM8300 Sigma product (RPX-0005) that respondents argue has “a copyright date of 1998 on its printed circuit board,” and the EM8475 Sigma product (RPX-00008) that respondents argue “copyright date of 2001 on its printed circuit board.” Resps. Br. at 95-96.

Respondents have not shown that either the EM8300 or EM8475 was the subject of a commercial offer of sale or in public use. In particular, Mr. Ignaszewski’s unsupported

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testimony regarding what was on sale 16-20 years ago, *see, e.g.*, RX-0668C (Ignaszewski WS) at Q/A 16-18, 21, 40, 52-53 is not reliable and does not show that the products were on sale or publicly used. For example, Mr. Ignaszewski's testimony about what he remembers seeing 20 years ago at a trade show in Las Vegas is not a sound foundation from which to conclude the whether the Quasar chips are prior art. *Id.* at Q/A 18. Similarly, Mr. Ignaszewski's testimony about working on products in his "small apartment in New York City" in 2001 is not a sound foundation from which to conclude that the EM8475 was publicly used or sold. *See, e.g.*, RX-0668C (Ignaszewski WS) at Q/A 40. Similarly, respondents' reliance on the 1998 and 2001 copyright dates does not show, through clear and convincing evidence, that the Quasar chips were the subject of a commercial offer of sale or in public use. Finally, the administrative law judge notes that respondents do not cite documents typically used to establish a commercial sale or public use (*e.g.*, sales orders or receipts, product catalogs, brochures, flyers, or advertisements) to support their contention that the Quasar chips are prior art.

Accordingly, respondents have not shown, through clear and convincing evidence, that the EM8300 or EM8475 are prior art to the '844 Patent.

In the event that the Quasar chips are determined to be prior art, respondents have argued that the chips, as discussed in RX-0325, RX-0326, RX-0327, and RX-0328, anticipate claims 1-4 and 6-10 of the '844 patent.

1. Claim 1

a) *[Preamble]: A digital media decoding system comprising:*

Respondents argue:

The EM8300 and EM8475 Quasar Chips disclose "[

].

RX-0383C at Q262; RX-0325C.00001; RX-0328C.00001.

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Resps. Br. at 101.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 228 (arguing that “none of the ‘Quasar Chip’ references disclose “a processor adapted to control a decoding process.”); Broadcom Reply, Section III(D).

The evidence and argument cited in respondents’ brief shows that the Quasar chips are digital media decoding systems as described in the preamble. *See, e.g.*, RX-0383C (Stevenson) Q/A 262. Accordingly, the administrative law judge has determined that the Quasar chips satisfy the preamble.

b) Limitation [A]: a processor adapted to control a decoding process; and

Respondents argue:

The Quasar documentation discloses a [

]” *Id.* at 307-310. These contentions are false and are premised on ignoring the testimony of Mr. Ignaszewski.

Specifically, Dr. Stevenson testified that the Quasar documentation discloses a [

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]. See
RX-0668C at Q22-31, 34-46; RX-325C and RX-0327C at 2; Tr.
(Ignaszewski) at 435:12-24, 442:5-15, 443:24-444:6, 447:16-25,
477:23-478:13, 482:4-489:6. Accordingly, this limitation is met.

Resps. Br. at 101-02.

Broadcom argues, in part:

For example, none of the “Quasar Chip” references disclose “[

]” *Id.*

Broadcom Br. at 228-29. Broadcom also argues that “Dr. Stevenson presents no evidence that supports his assertion that the ‘[].” *Id.* at 229.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the Quasar chip

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includes a processor adapted to control a decoding process. In Q/A 263—Dr. Stevenson’s entire testimony on this limitation—Dr. Stevenson testified as follows:

Q263. How does the Quasar Chip disclose the limitation “a processor adapted to control a decoding process”?

A263. I refer to this limitation as 1[a]. The Quasar Chip references disclose a [

...]”).

It is my opinion that the Quasar Chip alone or in combination discloses this limitation under Complainant’s proposed constructions.

RX-0383C (Stevenson WS) at Q/A 263.

RX-0325, which is entitled “Huffman Decoder,” explains that “[

]”

RX-0325 at 1.

RX-0327 shows [

RX-0327 at 2.

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RX-0327 does not show a [

.⁵²

J. *See also* CX-0579C (Acton RWS) at Q/A 202.

Furthermore, as Dr. Stevenson's testimony does not discuss the EM8475 chip, *see* RX-0383C (Stevenson WS) at Q/A 263, respondents have not shown that this chip includes a processor adapted to control a decoding process.

Accordingly, respondents have not shown that the Quasar chips satisfy limitation [A].

c) ***Limitation [B]: a hardware accelerator coupled to the processor and***

Respondents' entire argument is:

The EM8300 and EM8475 Quasar chips disclose "[

⁵² Mr. Ignaszewski's testimony at the hearing that "RISC CPU" "should have been called RISC with DSP extension" is not persuasive, especially in view of substantial documentary evidence to the contrary. Ignaszewski Tr. 435; *see also id.* at 426-427.

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] This admitted evidence confirms this element is satisfied.

Resps. Br. at 102.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 228 (arguing that “none of the ‘Quasar Chip’ references disclose “a processor adapted to control a decoding process.”); Broadcom Reply, Section III(D).

Assuming the Quasar chips include the requisite processor, the evidence and argument cited in respondents’ brief shows that the Quasar chips include a hardware accelerator, as described in claim 1. *See, e.g.*, RX-0383C (Stevenson) Q/A 264. Accordingly, the administrative law judge has determined that the Quasar chips include hardware accelerators that show the subject matter of this limitation was previously known.

d) Limitation [C]: adapted to perform a decoding function on a digital media data stream,

Respondents’ entire anticipation argument is:

The EM8300 and EM8475 Quasar chips discloses “[

] RX-0383C at Q266-68.

Resps. Br. at 102-03.

Dr. Stevenson testified as follows:

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Q265. How does the Quasar Chip disclose the limitation “a hardware accelerator . . . adapted to perform a decoding function on a digital media data stream”?

A265. I refer to this limitation as 1[c]. The Quasar Chip discloses
“[

].

RX-0383C (Stevenson WS) at Q/A 265. In Q/A 264, Dr. Stevenson testified:

Q264. How does the Quasar Chip disclose the limitation “a hardware accelerator coupled to the processor”?

A264. I refer to this limitation as 1[b]. The Quasar Chip discloses
[

].

Id. at Q/A 264. Mr. Ignaszewski testified as follows:

[

]

RX-0668C (Ignaszewski WS) at Q/A 22.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 228 (arguing that “none of the ‘Quasar Chip’ references disclose “a processor adapted to control a decoding process.”); Broadcom Reply, Section III(D).

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Assuming the Quasar chips include the requisite hardware accelerator, the evidence and argument cited in respondents' brief shows that the hardware accelerators ([] are adapted to perform a decoding function, as described in claim 1. *See, e.g.*, RX-0383C (Stevenson) Q/A 264-65. Accordingly, the administrative law judge has determined that the Quasar chips include hardware accelerators that show the subject matter of this limitation was previously known.

- e) Limitation [D]: wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods.*

Respondents' entire argument is:

The EM8300 and EM8475 Quasar chips discloses "[

]” *Id.*; RX-0325C.00009-10;
RX-0326C.00003.

Resps. Br. at 103.

Dr. Stevenson's testimony on this limitation follows:

Q269. How does the Quasar Chip disclose the limitation “wherein the accelerator is configurable to perform the decoding function according to a plurality of decoding methods”?

A269. I refer to this limitation as 1[d]. The Quasar Chip discloses “[

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] . It is my opinion that the Quasar Chip discloses this limitation under Complainant's proposed constructions.

RX-0383C (Stevenson WS) at Q/A 269.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 228 (arguing that "none of the 'Quasar Chip' references disclose "a processor adapted to control a decoding process."); Broadcom Reply, Section III(D); *see also* CX-0579C (Acton RWS) at Q/A 201-08 (Dr. Acton does not clearly rebut RX-0383C (Stevenson WS) at Q/A 269).

Assuming the Quasar chips include the requisite hardware accelerator, the evidence and argument cited in respondents' brief shows that the hardware accelerators ([
]) are adapted to perform a decoding function, as described in claim 1. *See, e.g.*, RX-0383C (Stevenson) Q/A 264-65. Accordingly, the administrative law judge has determined that the Quasar chips include hardware accelerators that satisfy this limitation.

2. Claim 2

Respondents argue:

The EM8300 and EM8475 Quasar chips meet claim 2 for the same reasons as claim 1, disclosing that the Quasar Chip can decode a variety of standards ([
]). RX-0383C at Q270; RX-0325C.00011-16.

Resps. Br. at 103-04.

Broadcom argues: "Claims 2-4 and 6-10 are not invalid in view of the asserted prior art for the same reasons provided for claim 1. [CX-0579C (Acton RWS)] at Q/A 192-223."

Broadcom Br. at 241; *see also* CX-0579C (Acton RWS)] at Q/A 209 ("It is my opinion that

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Quasar Chip does not disclose claim 2 for the same reasons that I discussed with respect to claim 1.”).

The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claim 2 based on its dependency from claim 1.

3. Claim 3

Respondents argue that the Quasar chips anticipate claim 3 for the same reasons they anticipate claim 1. *See* Resps. Br. at 104.

Broadcom argues: “Claims 2-4 and 6-10 are not invalid in view of the asserted prior art for the same reasons provided for claim 1. [CX-0579C (Acton RWS)] at Q/A 192-223.” Broadcom Br. at 241.

The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claim 3 based on its dependency from claim 1.

4. Claim 4

Respondents argue “The EM8300 and EM8475 Quasar chips meet claim 4 for the same reasons that claims 1, 2, and 3 are met. RX-0383C at Q273.” Resps. Br. at 104.

Broadcom argues: “Claim 4 is not invalid in view of the asserted prior art for the same reasons provided for claim 3. [CX-0579C (Acton RWS)] at Q/A 212-213.” Broadcom Br. at 241.

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The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claim 4 based on its dependency from claim 1.

5. Claims 6 and 7

Respondents argue “The EM8300 and EM8475 Quasar chips meet claims 6 and 7 (“wherein the processor is adapted to configure the accelerator to perform the decoding function”) for the same reasons that claims 1[c and d] are met. RX-0383C at Q274-75.” Resps. Br. at 104-05.

Broadcom argues: “Claims 2-4 and 6-10 are not invalid in view of the asserted prior art for the same reasons provided for claim 1. [CX-0579C (Acton RWS)] at Q/A 192-223.” Broadcom Br. at 241.

The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claims 6 and 7 based on their dependency from claim 1.

6. Claim 8

Respondents argue that the Quasar chips anticipate claim 8 for the same reasons they anticipate claims 1 and 7. *See* Resps. Br. at 105.

Broadcom argues: “Claim 8 is not invalid in view of the asserted prior art for the same reasons provided for claim 7. [CX-0579C (Acton RWS)] at Q/A 218-219.” Broadcom Br. at 241.

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The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1 and 7. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claim 8 based on its dependency from claims 1 and 7.

7. Claim 9

Respondents argue that the Quasar chips anticipate claim 9 for the same reasons they anticipate claim 1. *See* Resps. Br. at 105.

Broadcom argues: “Claims 2-4 and 6-10 are not invalid in view of the asserted prior art for the same reasons provided for claim 1. [CX-0579C (Acton RWS)] at Q/A 192-223.” Broadcom Br. at 241.

The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1. Accordingly, the administrative law judge finds that respondents have not shown that the Quasar Chip anticipates claim 9 based on its dependency from claim 1.

8. Claim 10

Respondents argue that the Quasar chips anticipate claim 10 for the same reasons they anticipate claims 1 and 3. *See* Resps. Br. at 105-06.

Broadcom argues: “Claim 10 is not invalid in view of the asserted prior art for the same reasons provided for claims 3 and 9. [CX-0579C (Acton RWS)] at Q/A 222-223.” Broadcom Br. at 241.

The administrative law judge previously determined that respondents have not shown that the Quasar Chip anticipates claim 1, 3, and 9. Accordingly, the administrative law judge finds

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that respondents have not shown that the Quasar Chip anticipates claim 10 based on its dependency from claims 1 and 9.

K. Obviousness – Reader Alone

Respondents argue that “Reader (the main Reader patent specification (RX-0317) with its MSP-1EX Appendices A and B (RX-0318)) anticipates and/or renders obvious claims 1-13 of the ‘844 Patent.” Resps. Br. at 63. Respondents’ brief, which blends anticipation and obviousness, apparently only discusses obviousness based on “Reader alone” for claims 3, 5, and 8.

1. Claim 1

The administrative law judge previously determined that Reader anticipates claim 1. If it is later determined that Reader does not anticipate claim 1, the administrative law judge would find that respondents have not shown that claim 1 is obvious based on Reader alone, as discussed below.

Respondents argue: “**Reader** (the main Reader patent specification (RX-0317) with its MSP-1EX Appendices A and B (RX-0318)) anticipates and/or **renders obvious** claims 1-13 of the ‘844 Patent.” Resps. Br. at 63 (emphasis added).

Respondents have blended their anticipation and obviousness arguments and do not discuss obviousness for each limitation. For example, in discussing limitation 1[D], respondents argue:

To the extent the Reader’s vector processor does not satisfy limitation 1[d] under Respondents’ construction, however, one of ordinary skill would have been motivated to look to the disclosures of the configurable “BP_Mode” register of Reader’s bitstream processor as described above to supplement the disclosures of the registers in the vector processor to arrive at limitation 1[d]. RX-0383C (Stevenson) Q110. In particular, it would have been obvious to one of ordinary skill that the vector processor could

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contain a register, similar to the BP_Mode register (*e.g.*, VP_Mode), that could be set by the scalar processor to indicate the standard format to the vector processor. *Id.* Reader already discloses “register-to-register” communications between the scalar and vector processors, as shown in Fig. 11. *Id.*; RX-0317 (‘073 Reader Patent) at Fig. 11; 2:17-18. Thus, the “standard format” information could be sent to the vector processor through such communications. *Id.* It is a relatively straight forward design choice to provide information to a coprocessor through registers, just as it is done for the bit stream processor. *Id.* Because the technique was used for the bitstream processor, one of ordinary skill would recognize that it could also be used for the vector processor. *Id.* Thus, based on Reader’s own disclosures, it would be obvious to one of ordinary skill that the vector processor could be configured with a “VP_Mode” register.

Resps. Br. at 73.

Dr. Stevenson testified as follows:

Q110. Did you form any other opinions concerning whether Reader discloses limitation 1[d] with respect to the vector processor?

A110. Yes. To the extent the vector processor does not satisfy this limitation, in my opinion, a POSITA would have been motivated to use the teachings of the configurable BP_Mode register of the bitstream processor of Reader to supplement the teachings of the registers of the vector processor. In particular, it would have been obvious to a POSITA that the vector processor could contain a register, similar to the BP_Mode register, that could be set by the scalar processor to indicate the standard format to the vector processor. Reader already discloses “register-to-register” communications between the scalar and vector processor, as shown in Fig. 11. Thus, the “standard format” information could be sent to the vector processor through such communications. Indeed, this is likely what is already occurring in the MSP-1EX system. It is a relatively straight forward design choice to provide information to a coprocessor through registers, just as it is done for the bit stream processor. Because the technique was used for the bitstream processor, in my opinion, a POSITA would recognize that it could also be used for the vector processor.

RX-0383C at Q/A 110.

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Respondents have not provided sufficient “suggestion or motivation to modify the teachings of that reference to the claimed invention in order to support the obviousness conclusion.” *SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1356 (Fed. Cir. 2000). Dr. Stevenson’s opinion that “one of ordinary skill would have been motivated to look to the disclosures of the configurable “BP_Mode” register . . . *to supplement the disclosures* of the registers in the vector processor *to arrive at limitation 1[d]*” (emphasis added) is improper hindsight—persons of ordinary skill (*e.g.*, engineers) do not modify designs to supplement prior art disclosures to arrive at specific limitations of asserted claims. *See Cheese Sys., Inc. v. Tetra Pak Cheese & Powder Sys., Inc.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (“Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’”).

Accordingly, the administrative law judge has determined that respondents have not shown claim 1 would have been obvious in light of Reader alone.

2. Claim 3

Respondents argue:

Alternatively, Reader and/or Reader-Fandrianto renders limitation 3[a] obvious. RX-0383C.0032 (Stevenson) Q117. To the extent either the bitstream processor or the vector processor is not found to be the claimed hardware accelerator, one of ordinary skill would have known that multiple instances of a bitstream or vector processor could be coupled in parallel to increase throughput by operate on successive blocks of data. *Id.* For instance, multiple parallel processors could increase throughput for run-length decoding because it is independent from one data block to the next. *Id.* This would have been obvious to one of ordinary skill based on the disclosures of Reader and within the knowledge of one of ordinary skill. *Id.*

Resps. Br. at 75.

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The administrative law judge previously determined that respondents have not shown that the vector processor is configurable. Dr. Stevenson testified:

Q117. Does Reader disclose “a plurality of hardware accelerators coupled to the processor”?

A117. Yes. I refer to this limitation as 3[a]. Reader alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Regarding 3[a], as I discussed for limitation 1[b], Reader discloses a bitstream processor and a vector processor that are both hardware accelerators coupled to the scalar processor. Thus, the combination of these accelerators is a plurality of hardware accelerators coupled to the processor. Alternatively, in my opinion, a POSITA would have known that multiple bitstream and/or vector processors could be coupled in parallel to increase throughput and performance. For instance, run-length decoding by the bitstream processor could be handled by parallel hardware (multiple bitstream processors) because run-length decoding is independent from one data block to the next, so the parallel processors could operate on successive blocks to increase throughput and performance. This would have been obvious to a POSITA and would have been within the knowledge of a POSITA. Further, to the extent Reader does not anticipate this limitation, it would have been obvious to modify Reader with the teachings of Baily to arrive at a plurality of hardware accelerators coupled to the processor.

RX-0383 (Stevenson WS) at Q/A 117.

The administrative law judge previously determined that respondents have not shown, through clear and convincing evidence, that both the vector and bitstream processors are configurable. In addition, Dr. Stevenson’s testimony that claim 3 is obvious in light of “Reader alone or in combination with the knowledge of a POSITA” does not address this deficiency. Further, Dr. Stevenson’s testimony regarding what “a POSITA would have known” is unsupported and deficient. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (The Federal Circuit has “repeatedly warn[ed] that references to “common sense”—whether to supply a motivation to combine or a missing limitation—cannot be used as a

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wholesale substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified.”); *see also In re Zurko*, 258 F.3d 1379, 1385 (Fed. Cir. 2001) (“deficiencies of the cited references cannot be remedied by [an agency’s] general conclusions about what is ‘basic knowledge’ or ‘common sense’ to one of ordinary skill in the art.”).⁵³ Accordingly, respondents have not shown that claim 3 would have been obvious over “Reader alone or in combination with the knowledge of a POSITA.”

3. Claim 5

The administrative law judge previously determined that Reader anticipates claim 5. If it is later determined that Reader does not anticipate claim 5, the administrative law judge would find that respondents have not shown that claim 5 is obvious based on Reader alone, as discussed below.

Respondents argue:

Reader and/or Reader-Fandrianto disclose “the processor is adapted to perform decoding functions on a digital media data stream.” RX-0383C Q129; RDX-0007.0115-0121.

Resps. Br. at 75.

Dr. Stevenson testified that “Reader alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation.” RX-0383C (Stevenson WS) at Q/A 129. His subsequent testimony, however, does not address obviousness. Accordingly, the administrative law judge finds that respondents have failed to show claim 5 would have been obvious based upon Reader alone.

⁵³ Respondents also have not shown why a person of ordinary skill would modify Reader to the extent the modification would “increase the complexity, cost, and die size of Reader’s system by including a plurality of vector or bitstream processors.” CX-0579C (Acton RWS) at Q/A 67.

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4. Claim 8

The administrative law judge previously determined that Reader anticipates claim 8. If it is later determined that Reader does not anticipate claim 8, the administrative law judge would find that respondents have not shown that claim 8 is obvious based on Reader alone, as discussed below.

Respondents argue:

Reader and/or Reader-Fandrianto disclose “the accelerator includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator.” RX-0383C (Stevenson) Q138; RDX-0007.0122-0123.

Resps. Br. at 78.

Dr. Stevenson testified that “Reader alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation for the same reasons it discloses limitation 1[d].” RX-0383C (Stevenson WS) at Q/A 138. His subsequent testimony, however, does not address obviousness. Accordingly, the administrative law judge finds that respondents have failed to show claim 8 would have been obvious based upon Reader alone.

L. Obviousness – Reader in view of Fandrianto

Respondents argue “Reader in view of Fandrianto renders obvious claims 1-13.” Resps. Br. at 63. Respondents’ brief, which blends anticipation and obviousness, apparently only discusses obviousness based on “Reader-Fandrianto” for claims 3, 5, 8, 11-13.

1. Claim 3

Respondents argue:

Alternatively, Reader and/or Reader-Fandrianto renders limitation 3[a] obvious. RX-0383C.0032 (Stevenson) Q117. . . .

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Resps. Br. at 75.

The cited testimony, however, does not discuss Fandrianto. *See* RX-0383C (Stevenson WS) at Q/A 117. Accordingly, the administrative law judge finds that respondents have failed to show claim 3 would have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

2. Claim 5

Respondents argue:

Reader and/or Reader-Fandrianto disclose “the processor is adapted to perform decoding functions on a digital media data stream.” RX-0383C Q129; RDX-0007.0115-0121. . . .

Resps. Br. at 77.

The cited testimony, however, does not discuss Fandrianto. *See* RX-0383C (Stevenson WS) at Q/A 129. Accordingly, the administrative law judge finds that respondents have failed to show claim 5 would have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

3. Claim 8

Respondents argue:

Reader and/or Reader-Fandrianto disclose “the accelerator includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator.” RX-0383C (Stevenson) Q138; RDX-0007.0122-0123. . . .

Resps. Br. at 78.

The cited testimony, however, does not discuss Fandrianto. *See* RX-0383C (Stevenson WS) at Q/A 138. Accordingly, the administrative law judge finds that respondents have failed to show claim 8 would have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

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4. Claim 11

The administrative law judge previously determined that Reader does not anticipate claim 11 and that Fandrianto does not disclose the claimed pixel filter. If it is later determined that Fandrianto discloses the claimed pixel filter, the administrative law judge would find that respondents have not shown that claim 11 is obvious based on Reader and Fandrianto, as discussed below.

Respondents argue:

To the extent any of the forgoing invalidity grounds from claims 1, 3 and 10 do not invalidate limitation 11[d], it would have been obvious to modify any one of them with Fandrianto to arrive at a pixel filter adapted to perform pixel filtering on the data stream. RX-0383C (Stevenson) Q152; RX-0324 (Fandrianto).

Resps. Br. at 79.

Broadcom argues that Fandrianto does not disclose the claimed pixel filter. *See* Broadcom Br. at 215.

Having considered the parties' arguments, and assuming that Fandrianto discloses the claimed pixel filter, the administrative law judge has determined that respondents have not shown that claim 11 would have been obvious based on Reader and Fandrianto because one of ordinary skill in the art would not modify Reader in light of Fandrianto. In particular, Dr. Stevenson testified as follows:

Q152. Does Reader disclose “a pixel filter adapted to perform pixel filtering on the data stream”?

A152. Yes. I refer to this limitation as 11[d]. . . . To the extent Reader does not anticipate this limitation, it would have been obvious to modify Reader with Fandrianto *to arrive at a pixel filter adapted to perform pixel filtering on the data stream*. As I stated previously, Fandrianto is in the same field of endeavor as Reader, namely video decoding. . . . Reader describes a system for multi-standard decoding. In my opinion, a POSITA would have

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been motivated to look to the teachings of similar technology. The similar architectures between the two references would enable one of implement the functionality of Fandrianto in the system of Reader. In my opinion, a POSITA looking to improve upon the system of Reader would consider Fandrianto. Fandrianto also provides explicit motivation to add a deblocking filter to the functional block of Reader—to “reduce blocking artifacts often visible at low bit rates.” [See RX0254 (Fandrianto) at 16:33-40]. In my opinion, a POSITA would have therefore been motivated to add the smoothing and de-blocking filters of Fandrianto to the system of Reader, and adding such filters *would have had a reasonable expectation of success, because such filters constituted a well-known improvement in the art.*

RX-0383C (Stevenson WS) at Q/A 152 (emphasis added).

Dr. Stevenson’s testimony begins with the opinion that a person of ordinary skill would modify Reader “to arrive” at the contested aspect of claim 11 (“a pixel filter adapted to perform pixel filtering on the data stream”), which is improper. Further, Dr. Stevenson’s opinion that adding Fandrianto’s filter to Reader “would have had a reasonable expectation of success, because such filters constituted a well-known improvement in the art” is conclusory and unsupported. See CX-0579C (Acton RWS) at Q/A 109 (“Given the complexity of this technology and the systems used to decode video, a POSA would not presume that there would an expectation of success when modifying a video decoder system simple because the alleged improvement was known.”).⁵⁴

Accordingly, the administrative law judge has determined that respondents have not shown that a person of ordinary skill in the art would combine or modify the references in the manner suggested. Thus, the administrative law judge finds that claim 11 would not have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

⁵⁴ Further, Dr. Stevenson has not established that the filters described in Fandrianto were common or well-known at the time of the invention.

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5. Claim 12

For claim 12, which depends from claim 11, Respondents argue:

To the extent any of the forgoing invalidity grounds from claims 1, 10 and 11 do not anticipate claim 12, it would have been obvious to modify each of them with the deblocking filter of Fandrianto to arrive at claim 12 for the same reasons it would have been obvious to modify Reader with Fandrianto to meet limitation 11[d]. RX-0383C (Stevenson) Q156.”

Resps. Br. at 80.

Broadcom argues that “Claims 12 and 13 are not invalid in view of the asserted prior art for the same reasons provided for claims 9, 10, and 11. [CX-0579C (Acton RWS)] at Q/A 112-115.].” Broadcom Br. at 210.

The administrative law judge previously determined that Reader and Fandrianto do not disclose subject matter corresponding to limitation 11[d]. Accordingly, the administrative law judge finds that claim 12 would not have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

6. Claim 13

Respondents’ entire argument is: “*See* claims 1, 3, 10 and 11. RX-0383C.0041 (Stevenson) Q158.” Resps. Br. at 80.

The administrative law judge previously determined that Reader and Fandrianto do not disclose subject matter corresponding to limitation 11[d]. Accordingly, the administrative law judge finds that claim 13 would not have been obvious based upon the disclosures and teachings of Reader and Fandrianto.

M. Obviousness – Reader in view of Fandrianto and/or Bailey

Respondents argue “Reader in view of Fandrianto renders obvious claims 1-13. [RX-0383C (Stevenson) Q/A 72]. Reader in view of Fandrianto and/or Bailey renders obvious

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claims 3-4 and 10-14. *Id.*” Resps. Br. at 63. Respondents’ brief, which blends anticipation and obviousness, apparently only discusses obviousness based on “Reader and/or Reader-Fandrianto in view of Bailey” for claim 3. *Id.* at 75-77.

The administrative law judge previously determined that Reader anticipates claim 3. If it is later determined that Reader does not anticipate claim 3, the administrative law judge would find that respondents have not shown that claim 3 is obvious based on “Reader and/or Reader-Fandrianto in view of Bailey” for the following reasons.

Respondents argue:

To the extent Reader and/or Reader-Fandrianto do not disclose limitation 3[a], however, Reader and/or Reader-Fandrianto in view of Bailey renders this limitation obvious. RX-0383C (Stevenson) Q117 and Q121; RX-0259 (Bailey). As seen in Figure 2, Bailey discloses a programmable system that includes one or more vision processors (“VP”) connected to a vision controller (“VC”). RX-0383C (Stevenson) Q121; RX-0259 (Bailey) at Fig. 2; Pg. 35. Like Reader, Bailey programs its system to perform decoding operations in accordance with different video standards (*i.e.*, H.261, MPEG and JPEG) for a variety of multimedia applications, such as “video conferencing.” RX-0383C (Stevenson) Q121; RX-0259.0003 (Bailey). Bailey discloses that the VC is the “smart microcontroller” that can “perform coder decoding, supervise decompression via the VP, perform postprocessing, and generate digital pixel output ...” RX-0383C (Stevenson) Q121; RX-0259.0004 (Bailey). Thus, Bailey discloses a system that performs analogous functions for use in the same video decoding field as Reader, and one of ordinary skill reading one reference would have been motivated to look to the other for further disclosures. RX-0383C (Stevenson) Q121.

Resps. Br. at 75-76.

Broadcom argues:

Reader (the Patent alone or in combination with the appendices) or Reader in combination with Bailey does not disclose or renders obvious claims 3 and 10, which require a “plurality of hardware accelerators coupled to the processor, ... wherein each of the accelerators are configurable to perform their associated decoding

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functions according to a plurality of decoding methods.” *Id.* at Q/A 66-75, 100-101. The vector processor is not a configurable hardware accelerator and, thus, Reader does not disclose or render obvious a plurality of configurable hardware accelerators. *Id.* at Q/A 67. As discussed above for claim 1, the bit stream processor is not a configurable hardware accelerator and, thus, Reader does not disclose or render obvious a plurality of configurable hardware accelerators. *Id.* at 73; *see e.g.*, RX-0317 (Reader) at 1:42-56; 4:6-17; 4:13, Fig. 3; RX-0319 (MSP-1EX Appendix) at A-124.

Respondents proposed combination of Reader with Bailey fails to render obvious claims 3 and 10 because a POSA would not combine the references. CX-0579C (Acton WS) at Q/A 69. Dr. Stevenson’s proposed combination of Reader and Bailey fails to provide any discussion that there would be an expectation of success in modifying Reader in combination with Bailey. *Id.* Dr. Acton testified that a POSA would not presume that there would be an expectation of success when modifying a video decoder system simply because the alleged improvement was known because of the complexity of this technology and the systems used to decode video. *Id.*

Broadcom Br. at 206-07.

Having considered the parties’ arguments, the administrative law judge has determined that Bailey discloses a plurality of hardware accelerators coupled to a processor, as claim 3 requires. *See* RX-0383C (Stevenson WS) at Q/A 121; RX-0259 at Fig. 2, p. 35. Respondents have not shown, however, that a person of ordinary skill in the art would have modified Reader in view of Bailey in the manner that respondents suggest. *See* CX-0579C (Acton RWS) at Q/A 69. In particular, Dr. Stevenson’s testimony is conclusory and does not account for the increase in cost, size, and complexity associated with adding multiple bitstream processors. *Id.* Accordingly, the administrative law judge finds that claim 3 would not have been obvious based upon the disclosures and teachings of on “Reader and/or Reader-Fandrianto in view of Bailey.”

N. Obviousness – Reader in view of the MSP-1EX appendix

Respondents argue:

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To the extent the main body of the Reader patent specification and its MSP-1EX appendix (A and B) are considered separate references, the MSP-1EX appendix individually contains disclosures that are sufficient to invalidate claims 1-13 of the '844 Patent under 102(b) and 103(a). RX-0383C (Stevenson) Q75. Thus, the MSP-1EX appendix anticipates and/or renders obvious, alone or in combination, claims 1-13 of the '844 Patent. RX-0383C (Stevenson) Q68; RDX-0007. The MSP-1EX appendix in view of Fandrianto renders obvious claims 1-13. RX-0383C (Stevenson) Q72. The MSP-1EX appendix in view of Fandrianto and/or Bailey renders obvious claims 3-4 and 10-14. *Id.*

Resps. Br. at 80-81.

Broadcom argues:

Regardless, even if the Appendices are considered as part of the Reader Patent, or combined with Reader, for all the reasons discussed above, Reader would still not anticipate and/or render obvious claim 1 because the vector processor is neither a hardware accelerator nor configurable and the bitstream processor is not a hardware accelerator.

Broadcom Br. at 206.

The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

O. Obviousness – Reader in view of the MSP-1EX appendix and Fandrianto

The Joint Outline lists “The Reader specification in view of the MSP-1EX appendix and Fandrianto (claims 1-13)” as an issue to be decided. Joint Outline at 5.

The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

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P. Obviousness – Reader in view of the MSP-1EX appendix and Fandrianto and/or Bailey

The Joint Outline lists “The Reader specification in view of the MSP-1EX appendix and Fandrianto (claims 1-13)” as an issue to be decided. Joint Outline at 5.

The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

Q. Obviousness – MSP-1EX appendix

The Joint Outline lists “Reader’s MSP-1EX appendix (claims 1-13)” as a “Validity” issue to be decided. Joint Outline at 5.

The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

R. Obviousness – MSP-1EX appendix in view of Fandrianto

The Joint Outline lists “The MSP-1EX appendix in view of Fandrianto (claims 1-13)” as an issue to be decided. Joint Outline at 5.

The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

S. Obviousness – MSP-1EX appendix in view of Fandrianto and/or Bailey

The Joint Outline lists “The MSP-1EX appendix in view of Fandrianto and/or Bailey (claims 3-4 and 10-14)” as an issue to be decided. Joint Outline at 5.

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The administrative law judge previously determined that the MSP-1EX appendix (RX-0318) is part of Reader. Accordingly, there is no need to consider the appendix as a separate document for obviousness purposes.

T. Obviousness – Fandrianto Alone

Respondents argue “*Fandrianto* anticipates and/or *renders obvious* claims 1-13 of the ‘844 Patent under all constructions.” Resps. Br. at 85 (emphasis added). Respondents’ brief, which blends anticipation and obviousness, apparently only discusses obviousness based on “Fandrianto alone” for claims 3 and 11.

1. Claim 3

Respondents argue:

Limitation 3[a]: Fandrianto discloses “a plurality of hardware accelerators coupled to the processor.” RX-0383C at Q189; RDX-0008.00027-00028. The H.221/BCH decoder, Huffman codec, and video processor are each a hardware accelerator coupled to the RISC processor. *Id.* Thus, the combination of these accelerators is a plurality of hardware accelerators coupled to the processor. *Id.*

Alternatively, multiple H.221/BCH decoders, Huffman codecs, and/or video processors could be coupled in parallel to increase throughput and performance. RX-0383C.0047-0048 (Stevenson) Q189. This would have been obvious to one of ordinary skill and would have been within their knowledge. *Id.*

Resps. Br. at 92.

The administrative law judge previously determined that Fandrianto’s video processor and H.221 decoder are hardware accelerators that are configurable and coupled to the RISC processor. Fandrianto’s video processor and H.221 decoder, in turn, constitute the “plurality of hardware accelerators coupled to the processor” as claim 3 requires. *See* RX-0383C (Stevenson WS) at Q/A 189-91. If Fandrianto does not disclose “limitation 3[a],” then the administrative law judge would find that Dr. Stevenson’s testimony that claim 3 is obvious in light of

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“Fandrianto alone or in combination with the knowledge of a POSITA” (RX-0383C (Stevenson WS) at Q/A 189) does not cure this deficiency. In particular, Dr. Stevenson’s testimony regarding what “a POSITA would have known” is unsupported and deficient. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (The Federal Circuit has “repeatedly warn[ed] that references to “common sense”—whether to supply a motivation to combine or a missing limitation—cannot be used as a wholesale substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified.”); *see also In re Zurko*, 258 F.3d 1379, 1385 (Fed. Cir. 2001) (“deficiencies of the cited references cannot be remedied by [an agency’s] general conclusions about what is ‘basic knowledge’ or ‘common sense’ to one of ordinary skill in the art.”). Accordingly, respondents have not shown that claim 3 would have been obvious over “Fandrianto alone or in combination with the knowledge of a POSITA.”

2. Claim 11

Respondents have argued:

Fandrianto discloses claim 11. RX-0383C at Q204; RDX-0008.00037-00040.

...

Limitation 11[e]: *See* claims 1, 3, and 10. RX-0383C at Q208. The video processor performs motion estimation. *Id.*; *see* RX-0324 (Fandrianto) at 12:48-57. Motion estimation is used for motion compensation. RX-0383C.0050 at Q208. Dr. Acton admits this. CX-0003C.0007 (Acton) at Q21. ***Alternatively, limitation 11[e] would have been obvious to one of ordinary skill based on these disclosures. RX-0383C at Q208.***

Resps. Br. at 95 (emphasis added).

Dr. Stevenson’s testimony follows:

Q208. Does Fandrianto disclose limitation 11[e]?

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A208. Yes. Fandrianto alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious limitation 11[e]. Fandrianto discloses that the video processor performs motion estimation. [See RX-0324 (Fandrianto) at 12:48-57]. Motion estimation is used in motion compensation. Thus, Fandrianto discloses limitation 11[e] for the same reasons it discloses limitation 1[c] and claims 9 and 10. *Alternatively, limitation 11[e] would have been obvious to a POSITA based on these disclosures.*

RX-0383C (Stevenson WS) at Q/A 208 (emphasis added).

The cited testimony is conclusory and does not explain how “a motion compensator adapted to perform motion compensation on the data stream” (*i.e.*, limitation 11[e]) would have been obvious based on Fandrianto. Accordingly, the administrative law judge finds that respondents have failed to show claim 11 would have been obvious based upon Fandrianto alone.

U. Obviousness – Diaz et al.

The Joint Outline lists “(1) Diaz, (2) Diaz in view of Purcell, (3) Diaz in view of Fandrianto, and (4) Diaz in view of Fandrianto and Purcell” as separate “Validity” issues to be decided. *See* Joint Outline at 5. Respondents have not presented any arguments concerning Diaz. *Id.*

Accordingly, the administrative law judge finds that respondents have failed to show that the asserted claims would have been obvious in light of Diaz or any combinations of prior art including Diaz.

V. Obviousness – Bakhmutsky

The Joint Outline lists “Bakhmutsky” as a “Validity” issue to be decided. *See* Joint Outline at 5. Respondents have not presented any arguments concerning Bakhmutsky. *Id.*

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Accordingly, the administrative law judge finds that respondents have failed to show that the asserted claims would have been obvious in light of Bakhmutsky.

W. Obviousness – Quasar Chip Alone

Respondents argue:

The EM8300 and EM8475 Quasar chips anticipate (*or render obvious if combined*) claims 1-4 and 6-10 of the '844 Patent under Complainant's proposed claim constructions. RX-0383C at Q261; *see* RDX-0012. Alternatively, they render obvious claims 1-4 and 6-10 of the '844 Patent under Complainant's proposed claim constructions. RX-0383C at Q261; *see* RDX-0012.

Resps. Br. at 100 (emphasis added). Respondents' brief, which blends anticipation and obviousness, apparently only discusses obviousness based the Quasar chips for claim 1 only. *Id.* at 102-03.

In the testimony respondents cite, Dr. Stevenson opined:

Q261. What conclusions did you reach about the validity of claims 1-4 and 6-10 of the '844 patent in view of the Quasar Chip references?

A261. In my opinion, the Quasar Chip anticipates (or renders obvious if the Quasar Chip references are considered to be independent references used in combination) claims 1-4 and 6-10 of the '844 patent under Complainant's proposed claim constructions. *See* RDX-0012. Alternatively, it is my opinion that the Quasar renders obvious claims 1-4 and 6-10 of the '844 patent under Complainant's proposed claim constructions. *See* RDX-0012. It is also my opinion that the Quasar Chip in view of Fandrianto [RX-0324] renders obvious claims 1-4 and 6-10 of the '844 patent under either party's claim constructions of "digital media data stream." *See* RDX-0012. To the extent that the parties' claim construction disputes for a particular term affect my analysis, I analyzed those distinctions and factored those effects into my opinion.

RX-0383C (Stevenson WS) at Q/A 261.

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This testimony does not show that the asserted claims would have been obvious based on the Quasar Chip alone because it does not explain which limitations the Quasar Chips does not disclose or how the Quasar Chips would be modified. In other words, respondents have not analyzed “the differences between the claimed invention and the prior art” as 35 U.S.C. § 103 requires. *Graham v. John Deere*, 383 U.S. at 17 (“Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved.”). Accordingly, the administrative law judge finds that respondents have failed to show that the asserted claims would have been obvious based upon the Quasar Chip alone.

X. Obviousness – Quasar Chip in view of Fandrianto

The Joint Outline lists “Quasar Chip System in view of Fandrianto (claims 1-4 and 6-10)” as a validity issue to be determined. Joint Outline at 5.

Respondents argue:

These Quasar chips also render obvious claims 1-4 and 6-10 of the ‘844 Patent in view of Fandrianto [RX-0324] under either party’s claim constructions of “digital media data stream.” RX-0383C at Q261; RDX-0012.

Resps. Br. at 100-101. Respondents’ brief, which blends anticipation and obviousness, apparently only discusses obviousness based the Quasar chips and Fandrianto for claim 1—specifically limitation 1[c]—only. *Id.* at 102-03. Respondents argue:

Limitation 1[c]: The EM8300 and EM8475 Quasar chips discloses “[

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], Fandrianto utilizes a RISC processor. *Id.* at Q268; RX-0324 at Fig. 2, 4:64-5:10, 9:13-22. The RISC processor is coupled to a bitstream H.221/BCH decoder to separate audio and video data. RX-383C at Q268; RX-0324 at 4:64-5:10. One of ordinary skill would understand that a stream that contains video and audio data would be a transport stream, such as the Transport Stream of MPEG-2 systems. RX-383C at Q268. Further, one of ordinary skill would have been motivated to look to the disclosures of similar technology. *Id.* The similar architectures between these references would enable one of implement the functionality of Fandrianto in the system of EM8300 and EM8475 Quasar chips. *Id.* For example, one could implement the functionality of Fandrianto's RISC processor with [

]. *Id.* The resulting system would have the desirable quality of being able to process additional types of streams. *Id.*

Id.

Broadcom argues that the Quasar Chip in view of Fandrianto does not render claim 1 obvious. Broadcom Br. at 233-34.

The administrative law judge previously determined that the Quasar Chips disclose limitation 1[C]. In the event that it is later determined that the Quasar Chips do not disclose the limitation, the administrative law judge would find that the combination of the Quasar Chips and Fandrianto does not disclose the limitation.

In particular, having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that claim 1 would have been obvious based on the Quasar Chip and Fandrianto.

Dr. Stevenson has not shown how a stream from Fandrianto would operate as a transport stream within the framework outlined in the '844 Patent. *See* CX-0579C (Acton WS) at Q/A

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205 (“simply pointing to Fandrianto’s disclosure of a stream that is audio and video data does not disclose to a POSA that the stream is a “transport stream.””); *see also Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App’x 755, 758 (Fed. Cir. 2015) (“combinations that change the ‘basic principles under which the [prior art] was designed to operate,’ . . . may fail to support a conclusion of obviousness.”). Further, Dr. Stevenson has not explained that “implement[ing] the functionality of Fandrianto’s RISC processor []” would have been a straightforward task for a person of ordinary skill or that such a substitution, combination, or modification would have had a reasonable expectation of success. *See* RX-0383C (Stevenson WS) at Q/A 268 (Dr. Stevenson does not provided the required analysis). Accordingly, the administrative law judge finds that respondents have not shown that claim 1 would have been obvious based on the Quasar Chip and Fandrianto.

Further, as respondents have not presented an obviousness argument for claims 2-4 and 6-10, the administrative law judge finds that respondents have not shown that these claims would have been obvious based on the Quasar Chip and Fandrianto.

Y. Obviousness – Quasar Chip References

The Joint Outline lists “Quasar Chip References (claims 1-4 and 6-10)” and “Quasar Chip References in view of Fandrianto (claims 1-4 and 6-10).” Joint Outline at 5. The administrative law judge previously determined that the Quasar Chips are not prior art (respondents did not show that the EM8300 or EM8475 was the subject of a commercial offer of sale or in public use) and that the Quasar Chips, as discussed in RX-0325, RX-0326, RX-0327, and RX-0328, do not anticipate the asserted claims. *See* § V(J), *supra*.

The above obviousness determinations made for the “Quasar Chip System” are not changed based on the descriptions provided in RX-0325, RX-0326, RX-0327, and RX-0328.

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Accordingly, the administrative law judge finds that respondents have not shown that claims 1-4 and 6-10 would have been obvious based on the Quasar Chip alone (inclusive of the references) and/or the Quasar Chip (inclusive of the references) and Fandrianto.

Z. Obviousness – Secondary Considerations

Respondents' entire argument is:

Broadcom has not provided evidence of secondary considerations supporting non-obviousness of the '844 Patent. Respondents agree that no secondary considerations exist.

Resps. Br. at 109; *see also* Resps. Reply at 51 ("Broadcom has not provided evidence of secondary considerations supporting non-obviousness of the '844 Patent. Respondents agree that no secondary considerations exist.").

Broadcom has not clearly argued that secondary considerations support a non-obviousness finding. *See generally* Broadcom Br., Section V(A)(6) (*e.g.*, commercial success, unexpected results, long-felt need, failure of others, etc. are not discussed); Broadcom Reply, Section III(D).

Accordingly, the administrative law judge has determined that, with respect to all of the obviousness arguments respondents have raised, no evidence of secondary considerations supports a non-obviousness finding.

VI. U.S. PATENT NO. 7,590,059

A. Overview of the '059 Patent

The '059 Patent (JX-0002), entitled "Multistandard video decoder," issued on September 15, 2009. The application that would issue as the '059 Patent, Application No. 11/000,731, was filed on December 1, 2004 and claims priority to Provisional Application 60/573,357 (filed on May 21, 2004). The '059 Patent discloses a method for processing an encoded video stream.

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B. Claim Construction

1. Level of Ordinary Skill in the Art

Broadcom's expert, Dr. Acton, testified regarding the level of ordinary skill in the art for the '844 and '059 Patents. *See, e.g.*, CX-0003C (Acton WS) at Q/A 60-61.

Respondents' expert, Dr. Stevenson, testified as follows:

Q309. Do you have an opinion on the level of ordinary skill in the art of the '059 patent?

A309. Yes.

Q310. What is your opinion about the level of ordinary skill in the art for the '059 patent?

A310. In my opinion, a POSITA in the field of art of the '059 patent would have had a combination of education and experience in engineering and communications systems. This typically would consist of at least a Master's degree in Electrical Engineering, Computer Science, or Computer Engineering with at least two to three years of experience in development and programming relating to video digital signal processing, or an equivalent degree and/or experience. The POSITA would be familiar with the design of programmable real-time media processors. Superior education would compensate for a deficiency in experience, and vice-versa.

...

Q312. Did you consider the perspective of this POSITA in arriving at your expert opinions?

A312. Yes. In arriving at my expert opinions regarding the '059 patent, I have considered the issues from the perspective of this POSITA, at the timeframe of the alleged invention of the subject matter of the '059 patent. I have also considered the issues from the perspective of Complainant's definition of a person of ordinary skill in the art at the timeframe of the alleged invention of the '059 patent.

RX-0383C (Stevenson WS) at Q/A 309-10, 312. Dr. Stevenson's answer is substantively identical to his corresponding opinion for the '844 Patent. *Compare id.* at Q/A 310 *with id.* at Q/A 47.

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With respect to the '844 and '059 Patents, Broadcom states: “[t]he differences between the levels of ordinary skill in the art proposed by Broadcom and Respondents are minimal and do not effect analyses in this Investigation.” Broadcom Reply at 2, n.2.

As with the '844 Patent, the administrative law judge has determined that a person of ordinary skill in the art would have a master's degree in electrical engineering, computer science, or computer engineering with two to three years of experience in development and programming relating to video digital signal processing, or an equivalent degree and/or experience. RX-0383C (Stevenson WS) at Q/A 309-12. Dr. Acton's opinions do not change under this level of ordinary skill, *see* CX-0003C (Acton WS) at Q/A 61, and the differences between the levels of skill proposed by Broadcom and respondents are not material.

2. Agreed Construction

The parties “agree that ‘identifier’ means ‘an indication of a video encoding type distinct from a start code.’” Resps. Br. at 119; Broadcom Br. at 246.

3. Disputed Constructions

The parties dispute the following terms and phrases from the claims:

- Whether the preamble is limiting;
- “computer-readable storage”
- “receiving on said chip” and “. . . on said chip”
- “packetized data within the encoded video stream”
- “start code”

Joint Outline at 5; Broadcom Br. at 243-47; Resps. Br. at 110-19.

Claims 11 and 12, with the disputed terms and phrases emphasized, follow:

11. A *computer-readable storage* having stored thereon, a computer program having at least one code section for processing

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an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:

receiving on a chip, packetized data within the encoded video stream;

determining *on said chip*, an *identifier* within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;

selecting *on said chip*, a decoding process from a plurality of decoding processes based on said determined identifier; and

decoding *on said chip*, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.

12. The computer-readable storage according to claim 11, comprising code for determining on said chip, a *start code* within said received packetized data that separates packets within the encoded video stream.

JX-0002 at 20:15-34 (emphasis added).

a) Whether the preamble is limiting

The preamble is:

A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising

JX-0002 at 20:15-19.

Broadcom's entire opening argument is:

The parties dispute the proper construction of certain terms of the '059 Patent (JX-0002) and whether the preamble is limiting. The preamble is not limiting and in the context of the claim and the '059 Patent's specification, all of the disputed terms would have a clear meaning to POSA and do not need to be separately defined. CX-0003C (Acton WS) at Q/A 67-73.

Broadcom Br. at 243.

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Respondents argue that the preamble is limiting “because it provides the antecedent basis for the ‘encoded video stream[,]’” and “because it recites a ‘computer-readable storage’ with a specific ‘computer program’ that ‘perform[s] [the] steps’ recited by the claim, whereas the other independent claims (claims 1 and 21) recite a method and system without such specificity, respectively.” Resps. Br. at 110-11.

Broadcom replies:

Respondents argue the preamble is limiting. But a preamble is not limiting if the patentee has defined a complete invention in the claim and the preamble is only used to state a purpose or intended use. *See, e.g., Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002); *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1375-76 (Fed. Cir. 2001). That is the case here. As discussed above, the body of claim 11 is structurally complete, reciting four steps that occur on a chip – a receiving step, a determining step, a selecting step, and a decoding step. *See* JX-0002 (‘059 Patent) at cl. 11. Thus the body of the claim language defines a complete invention.

Respondents, however, argue that the preamble is limiting because its recitation of a “computer-readable storage” that stores a “computer program” that can be executed by a machine, resulting in the performance of the four steps gives “life, meaning, and vitality” to the claim because the other independent claims’ preambles do not include such specificity. RPostHB at 110-111. But, even though it may be more detailed than the preambles for independent claims 1 and 21, claim 11’s preamble does not recite essential structure or steps and instead simply provides a possible intended use for the invention. Thus, Respondents’ argument that the preamble is limiting because it the term “computer-readable storage” gives “life, meaning, and vitality” to claim 11 falls flat.

Respondents’ only other argument that the preamble is limiting is based on the assertion that it provides antecedent basis for the term “encoded video stream.” But antecedent basis is not always necessary and that fact alone does not make the preamble limiting. CRCCB at 13-14. For example, antecedent basis may not be necessary if “the claim drafters did not rely on the preamble language to define or refine the scope of the asserted claims.” *See Am. Med. Systems, Inc. v. Biolitec, Inc.*, 618 F.3d 1354, 1359 (Fed. Cir. 2010) (finding the preamble’s use of the generic term “tissue”

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did not “provide any ‘context essential to understand[ing]’ the meaning of ‘the tissue’ in the body of each claim”). And even if the term “encoded video stream” provided necessary antecedent basis that does not “necessarily convert the entire preamble into a limitation.” *TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323 (Fed. Cir. 2015).

Here, the term “encoded video stream” is not defined in the preamble, provides no essential context to understanding the meaning of the term in the body of the claim, and does not further limit the claim. Instead, it serves only to describe the intended use – decoding an encoded video stream. *See, e.g.*, JX-0002 (‘059 Patent) at Abstract, 2:38-39. Thus, it should not be found to be limiting.

Broadcom Reply at 71-73 (footnote omitted).

Having considered the parties’ arguments, the administrative law judge has determined that the preamble is limiting. Apart from the preambles, claims 1 and 11 are identical. *Compare* JX-0002 at 19:30-44 *with id.* at 20:15-30. Thus, the preamble of claim 11 is necessary for it to have meaning. *See Eaton Corp. v. Rockwell Intern. Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003). The preamble of claim 11 contains several and particular requirements for the computer-readable storage. Further, the preamble serves as the antecedent basis for the term “encoded video stream,” which appears in the body of the claim. In addition, Broadcom later relies on the language “executable by a machine” to argue that claim 11 is not indefinite. *See, e.g.*, Broadcom Br. at 244-25; CX-0003C (Acton WS) at Q/A 68. Accordingly, the preamble is limiting. *See id.*

b) “computer-readable storage”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning (<i>e.g.</i> , a computer program running non-transitory code)	transitory and non-transitory computer-readable storage

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See Broadcom Br. at 243; Resps. Br. at 111 (respondents note that their “proposed construction requires that this claim term can encompass both transitory and non-transitory storage—and not that a computer-readable storage needs to simultaneously be transitory storage and non-transitory storage”).

Broadcom argues:

This term does not need to be construed, as it is clear and would have a well-understood meaning to a POSA. CX-0003C (Acton WS) at Q/A 67. Respondents disagree, and ask the ALJ to construe the claim as “transitory and nontransitory computer-readable storage.” ROCCB at 40-42. As explained in COCCB, however, Respondents’ construction is simply an attempt to introduce the word “transitory” into the term, which, if included, would render the claims susceptible to invalidity under 35 U.S.C. § 101. COCCB at 14. Contrary to Respondents’ assertions, however, the ‘059 Patent does not define “computer-readable storage” and does not even suggest that transitory signals are contemplated. For example, words often associated with transitory signals, such as “wave” or any variation thereof, do not appear in the specification.

Additionally, while Respondents rely on the Examiner’s review of related patents, this reliance is misplaced, and Respondents seemingly ignore the prosecution of the ‘059 patent, where claim 11 was amended during prosecution to ensure that the claims *did not* encounter a 35 U.S.C. § 101 problem. CRCCB at 14; JX-0005 (‘059 Prosecution History) at BCM00059337, BCM00059397. Specifically, claim 11 was amended to claim “computer-readable storage” rather than “machine-readable storage” based on the Examiner’s suggestion in order to avoid “encounter[ing] a 101 problem.” *Id.*

The term “computer-readable storage” does not encompass transmitted signals and should be given its plain and ordinary meaning, which, as explained in CRCCB, is a computer program running non-transitory code.

Broadcom Br. at 243-44.

Respondents argue:

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Respondents propose that the term “computer-readable storage” in claim 11 should be construed, consistent with its plain meaning in view of the ‘059 Patent, as transitory and non-transitory computer-readable storage. RX-0383C (Stevenson) Q279. Although Complainant proposes plain and ordinary meaning for this term, it disagrees with Respondents’ proposal and seeks to exclude transitory media. In doing so, Complainant’s proposal impermissibly fails to capture all the preferred embodiments disclosed in the ‘059 Patent. *Id.* at Q298; *On-Line Tech. v. Bodenseewerk Perkin-Elmer*, 386 F.3d 1133, 1138 (Fed. Cir. 2004). Further, Complainant’s “plain and ordinary meaning” construction is inconsistent with how a person of ordinary skill would understand the term as used in the context of the ‘059 Patent.

As a threshold matter, the term “computer readable storage” includes both transitory and non-transitory media, unless the specification suggests otherwise. *Ex parte Mewherter*, No. 2012-007692, at 13 (B.P.A.I. May 8, 2013) (holding that “machine readable storage medium” includes a transitory medium such as a signal, absent any teaching to the contrary in the specification). Nothing in the ‘059 Patent limits the scope of this term; rather, the specification embraces both transitory and non-transitory media, as explained below. RX-0383C at Q297.

Claim 11 recites a “computer-readable storage having stored thereon, a computer program . . . for processing an encoded video stream” As such, the claimed “computer-readable storage” must store the “computer program.” As recognized in *Mewherter*, it is well-known in the art that transitory media such as a signal is capable of storing computer-readable information. *See, e.g., Ex parte Mewherter* at 7-12. Consistent with this understanding, the specification broadly defines “computer program” to include both non-transitory and transitory expressions of instructions. RX-0383C at Q297; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (“A patentee is free to be his own lexicographer.”). The patentee chose to broadly define “computer program” to include “. . . any expression . . . of a set of instructions . . . to perform a particular function . . . [regardless of] material form.” JX-0002 (‘059 Patent) at 19:8-14; RX-0383C at Q297. Thus, the expression of instructions making up the computer program includes transmitted signals. And the claimed “computer-readable storage” that stores that signal includes propagating electromagnetic waves in space (*e.g.*, satellite signals), which could store the information to be read by the computer. *Ex parte*

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Mewherter, No. 2012-007692, at 13 (B.P.A.I. May 8, 2013); RX-0383C at Q279.

That the claimed “computer-readable storage” includes transitory storage was confirmed during prosecution of related application, RX-1043 (U.S. Patent App. No. 12/560,231 (the “‘231 App.”)). The ‘231 App. is a continuation of the ‘059 Patent and shares a common specification with it. During prosecution of the ‘231 App., a proposed claim 42 was drafted nearly identical to claim 11 of the ‘059 Patent. *See* RX-1043.0003-4 (‘231 App.). Similar to claim 11, claim 42 was directed to a “computer-readable storage, having stored thereon a computer program . . . for processing video . . .” *Id.* The Examiner of the ‘231 App. found that the scope of claim 42 encompassed transitory embodiments. In support, the Examiner relied on the same definition of “computer program” in the ‘231 App. that is found in the ‘059 Patent. *See* RX-1043.0126-7. And, to overcome a related rejection, the Examiner “recommend[ed] adding the phrase ‘**non-transitory**’” to claim 42. *Id.* (emphasis added). The applicant made the recommended amendment, and the claim issued.

Similar to pre-amendment claim 42, claim 11 of the ‘059 Patent should be construed to cover the **full scope** of disclosed embodiments absent express disclaimer by the patentee. *See Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003) (“unless otherwise compelled . . . the same claim term in the same patent or related patents carries the same construed meaning.”); *In re Rambus Inc.*, 694 F.3d 42, 47 (Fed. Cir. 2012) (“To the extent Rambus wanted to limit the memory device to a single chip component, it could have expressly done so. It did not, and this Court will not do so here.”); *see also id.* at 48 (applying doctrine of claim differentiation between patent and related patents to support broader construction of claim term). Unlike amended claim 42 of the ‘231 App., the applicant chose not to amend claim 11 to narrow its scope to cover **only** non-transitory embodiments.

Resps. Br. at 111-13.

Having considered the parties’ arguments, the administrative law judge construes “computer-readable storage” to mean “non-transitory computer-readable storage.”

Respondents’ proposed construction, in their estimation, encompasses patent-eligible and ineligible subject matter. *See* Resps. Br. at 141-42 (arguing that the claims are invalid because

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they cover “transitory memory”). Respondents’ expert points to the following section of the specification, which discusses a computer program:

The invention may also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which when loaded in a computer system is able to carry out these methods. Computer program in the present context may mean, for example, any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following: a) conversion to another language, code or notation; b) reproduction in a different material form. However, other meanings of computer program within the understanding of those skilled in the art are also contemplated by the present invention.

JX-0002 at 19:8-17. The specification (excluding the claims), however, does not discuss “computer-readable” storage.⁵⁵ Respondents have not sufficiently explained why the phrase “computer-readable storage” (which the patent office suggested the applicant use) covers transitory storage and must be construed to cover what, in their view, is patent-ineligible subject matter. Further, the prosecution history does not support their construction, as the patent office recommended an amendment to avoid a § 101 problem and because the amendment is not specific as to whether it also encompasses transitory media.

Broadcom’s proposed construction—which its brief limits to non-transitory computer-readable storage—accords with the prosecution history and does not conflict with anything in the specification. *See* CX-0003C (Acton WS) at Q/A 67.

c) “receiving on a chip” and “. . . on said chip”

⁵⁵ On July 23, 2008, the applicant amended the claims from “machine-readable storage” to “computer-readable storage” in response to an examiner’s objection. *See* JX-0005 at 107 (the examiner stated that “A simple reason for [amending the claims] is that the ‘machine’ has a tendency to refer to non-processing capable device, in which case the claims would encounter a 101 problem.”), 167 (amending claim 11).

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The parties dispute whether claim 11 is indefinite based on the “receiving on a chip” and “on said chip” phrases. Respondents’ brief states that “Sigma contends that the term is indefinite under 35 U.S.C. § 112, second paragraph[.]” Resps. Br. at 113. Broadcom “denies that the term is indefinite under 35 U.S.C. § 112, second paragraph.” Broadcom Br. at 244.

Sigma argues, in part:

These terms are indefinite because: (1) it is not reasonably certain whether “a chip” is required to infringe claims 11-20, and (2) a “code section” cannot perform the claimed method steps, such as receiving data, on a chip. Claims 11-20 are directed to a computer-readable storage that stores a computer program. JX-0002 (’059 Patent) at 19:8-14; 20:15-20. They are not, however, directed to a system, method, or apparatus. *Id.*, compare claims 11-20 with claims 1-10, 21-30. Despite this fact, limitations in claims 11-20 contain “a chip,” which serves as the situs for performance of claimed steps. *Id.* For example, claim 11 recites:

11. A computer-readable storage having stored thereon, a **computer program having at least one code section** for processing an encoded video stream, the at least one code section being executable by a machine **to perform steps comprising:**

receiving on a chip, packetized data within the encoded video stream . . .

Id. at 20:15-20 (emphases added). As such, claims 11-20 are directed to (1) a code section of a computer program “being executable by a machine to perform steps” of a method and (2) a chip where the steps are performed. Such mixed method/apparatus claiming runs afoul of *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). A patent claim may not simultaneously cover an apparatus and a method of using the apparatus because the scope of such a claim cannot be reasonably ascertained. *Id.* Indeed, the scope of claim 11-20 is unascertainable because one of ordinary skill would not understand whether infringement requires the “chip” or whether only a “computer-readable storage”—divorced from the chip—could infringe, as long as the claimed steps could be capable of being performed on the chip if the code section were to be executed. Moreover, one cannot determine the scope also because “computer program” is defined in the specification to include transitory

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embodiments (*see* D.ii.b), which would not be tied to any physical location (*e.g.*, a chip). *Id.*

Resps. Br. at 113-14.

Broadcom argues:

These phrases are clear and would have conveyed well-understood meanings to a POSA. CX-0003C (Acton WS) at Q/A 68. Sigma argues that these phrases are indefinite because Sigma's attorneys are not reasonably sure whether "a chip" is required to infringe claims 11-20 and because a "code section" cannot perform the claimed method steps. ROCCB at 93-94. No other Respondent, however, makes this argument, and as explained in CRCCB, Sigma's arguments are without merit. CRCCB at 17-18. First, claim 11 is an apparatus claim that includes a chip. A POSA would understand the claimed machine would include a chip that would perform the identified steps. CX-0003C (Acton WS) at Q/A 68. Second, it is the chip that is performing the steps based on the code being executed on the claimed machine. Additionally, almost every figure in the '059 Patent depicts a video decoder, which is often referred to as a "processing block," and at least one processor or CPU. *Id.* at Q/A 49. In the specification discussing each of Figures 3A through 8, the processor or processors are described as being adapted to control the decoding process by sending instructions to other components on the SoC, either directly or indirectly, informing them how to process and decode the received encoded video stream. *Id.* Thus, the '059 Patent is clear that the processor itself, or the code, does not necessarily have to perform each recited step. *Id.*

Accordingly, a POSA would have a clear understanding of these terms' meanings when read in light of the specification and the prosecution history, and Sigma's indefiniteness argument should be rejected.

Broadcom Br. at 244-45.

In reply, respondents argue that claim 11 is not an apparatus claim, by pointing to claim 21, which clearly is an apparatus claim. Resps. Reply at 52. Respondents add "Broadcom also fails to explain how the scope of claims 11-20 is reasonably certain . . . and the claims are invalid for this reason as well." *Id.* at 53.

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Broadcom replies that “claim 11 is clear that each of the steps is occurring on a chip and that the steps’ occurrence is based on code being executed on the chip.” Broadcom Reply at 74.

Having considered the parties arguments, the administrative law judge has determined that claim 11, and the phrase “receiving on a chip . . .” and the subsequent “on said chip” references are not indefinite. Claim 11 is directed to a computer-readable storage that has code stored on it. *See* JX-0002 at 20:15-19 (preamble). The code must be able to perform the claimed steps when it is executed by a machine. *See* JX-0002 at 20:18-31 (preamble and subsequent steps). In addition, Dr. Acton testified that one of ordinary skill in the art would understand the claim, *see* CX-0003C (Acton WS) at Q/A 68 (“[T]hese phrases are clear and would have conveyed well understood meanings to a POSA at the time of the invention. In my opinion as these terms are used in the claims of the patent a POSA would have known what these terms refer to.”), while respondents did not cite or adduce any expert testimony on this point. In sum, the claim language is not ambiguous, nor does it mix claim a mixed method and apparatus. Respondents have not shown claim 11 is indefinite.

Accordingly, the administrative law judge will afford the phrases “receiving on a chip” and “on said chip” their plain and ordinary meaning.

d) “packetized data within the encoded video stream”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	a packetized elementary video stream

See Broadcom Br. at 245; Resps. Br. at 115.

Broadcom argues, in part:

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This term does not need to be construed, as it is clear and would have a well-understood meaning to a POSA. CX-0003C (Acton WS) at Q/A 69. A POSA would have understood that “packetized data within the encoded video stream” is a broad term and that an encoded video stream can include several types of packets, such as “transport stream packets,” “program stream packets,” and “Packetized Elementary Stream (PES) packets.” *Id.* For example, Sigma’s expert, Dr. Stevenson, admitted that a transport stream is an encoded video stream that includes video data and is packetized. Tr. (Stevenson) at 655:4-15.

Despite this admission, Respondents “narrowly construe[]” this term to be limited to “a packetized elementary video stream,” in an improper attempt to read out stream types, like transport streams, that Dr. Stevenson admitted fall under this term. ROCCB at 96-100; Tr. (Stevenson) at 656:10-16; RX-1079C (Stevenson WS) at Q/A 116. Respondents’ proposed construction, however, is incorrect and should be rejected. CRCCB at 19-21; CX-0003C (Acton WS) at Q/A 70.

Broadcom Br. at 245-46.

Respondents argue:

There is no dispute that the ‘059 Patent repeatedly and consistently describes the encoded video stream received in claim 11 as an elementary video stream. *E.g.*, JX-0002, at Figures 3a, 4a, 4b, 5-9. The ‘059 Patent speaks only in terms of packetized elementary video streams. *E.g.*, *id.* at 4:34-47, 5:6-9, 5:34-38, 6:9-20, 16:63-65, 17:47-50, 18:31-35, Figures 3a, 4a, 4b, 5-8. The sole inventor’s testimony is in accord; he acknowledged that his “invention” was all about receiving and analyzing an “elementary video stream.” RX-0670C at 117:7-24, 118:6-20. Nor is there any dispute that, consistent with the plain claim language, the elementary video stream received is a video stream that is encoded and consists of packetized data. RX-1083C (Bovik) Q217; CX-0062.18 (MPEG-2 Systems) at 2.1.30 (definition).

Notwithstanding this evidence, Broadcom refuses to accept the construction advanced by Respondents—“a packetized elementary video stream”—that is indisputably consistent with the record. Instead, Broadcom advocates the opposite. Broadcom urges the Court to adopt an undefined construction of “plain and ordinary meaning” so that its experts can advance an interpretation that reads out the term “video” and contradicts all of the record evidence, including its own inventor. Broadcom’s experts contend

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that the plain and ordinary meaning also includes a transport stream or program stream because it encompasses “transport stream packets” and “program stream packets.” CX-0003C (Acton) QA9. That interpretation is without merit. The terms “transport stream” and “program stream” appear nowhere in the ‘059 Patent, are different from an encoded video stream, may not include video, and were not contemplated by the inventor. *See* RX-1083C (Bovik) Q/A 215-18; RX-0670C at 43:20-45:12, 48:18-49:5; Tr. (Acton) at 144:7-17. The technology the inventor developed could not even work with a transport stream. RX-0670C at 43:20-45:12. The Court should reject Broadcom’s unsupported approach and instead adopt Respondents’ construction.

Resps. Br. at 115. Respondents further argue that Broadcom is attempting to broaden the meaning of the phrase. *Id.* at 116.

The administrative law judge has determined that the term “packetized data within the encoded video stream” should be construed according to its plain and ordinary meaning and that further construction of this term is not necessary. The term is not limited according to any particular type of stream, even though a person of ordinary skill in the art was aware that many types of streams existed when the ‘371 Application was filed in December 2004. *See* CX-0579C (Acton RWS) at Q/A 226 (“[A] POSA would understand that other stream types, such as transport streams, are also basic elements of standards since the mid-1990s, including several MPEG standards, such as those recited in the ‘059 patent.”); *see also* CX-0062 at .0007-8; CX-0003C (Acton WS) at Q/A 69-70; RX-0670C (Gordon Dep. Tr.) at 48-49. Furthermore, the ‘059 Patent distinguishes between “encoded video stream” and “elementary” streams. For example, in describing a start code, the patent explains that encoded video stream includes information beyond a packetized elementary video stream:

The start code 101 may comprise a plurality of bytes that may be arranged in a unique combination to signify the beginning of the encapsulated video payload 100 ***within an encoded video stream.*** For example, the start code 101 may comprise an exemplary byte

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sequence “00 00 01.” The start code suffix 103 may comprise one or more bytes located after the start code 101 within the encapsulated video payload 100. In one aspect of the invention, the start code suffix 103 may correspond to an encoding method utilized to *encode the elementary video stream* data 105 within the encapsulated video payload 100. For example, the start code suffix 103 may correspond to H.264, VC-1, MPEG-1, MPEG-2 and/or MPEG-4 as the encoding method utilized to encode the *elementary video stream data* 105. The start code 101 and the start code suffix 103 may be generated by the encoder prior to communicating the *encoded video stream* data to a video decoder.

JX-0002 at 5:17-33. Respondents’ proposed construction of “a packetized elementary video stream” is overly narrow, and does not account for the ‘059 Patent’s distinct treatment of the terms “encoded video stream” and “elementary video stream.”

Accordingly, the term “packetized data within the encoded video stream” is afforded its plain and ordinary meaning.

e) “start code”

The parties have proposed the following constructions:

Broadcom’s Proposed Construction	Respondents’ Proposed Construction
plain and ordinary meaning	a code distinct from the identifier that signifies the beginning of the encapsulated video payload

See Broadcom Br. at 247; Resps. Br. at 119.

Broadcom’s entire argument is:

This term does not need to be construed, as it is clear and would have a well-understood meaning to a POSA. CX-0003C (Acton WS) at Q/A 72. A POSA would have understood that a start code, as claimed in the ‘059 patent, consists of a number of bits, and that this number varies based on the standard being used for encoding. For example, MPEG-2’s start code is 32 bits while H.263’s start code is 17 bits. Tr. (Acton) at 876:19-877:1.

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Respondents, however, attempt to narrow the term “start code” by including unnecessary words in their construction. ROCCB at 105-106. But a POSA would have understood that a “start code” is simply that, a code of a varying number of bits that indicates the start of a packet, and Respondents’ construction should be rejected. CX-0003C (Acton WS) at Q/A 72.

Broadcom Br. at 247.

Respondents’ entire argument is:

Respondents propose a two-part construction for the term “start code”: (1) this term signifies the beginning of the encapsulated video payload; and (2) the start code is distinct from the identifier. Regarding (1), the ‘059 Patent’s specification discloses that the start code 101 identifies the start or beginning of the encapsulated video payload: “start code 101 may comprise a plurality of bytes that may be arranged in a unique combination to signify the beginning of the encapsulated video payload 100 within an encoded video stream.” RX-0383C at Q307; JX-0002.0017 (‘059 Pat) at 5:17-33 (emphasis added). As shown in Fig. 1, the encapsulated video payload begins with the start code bytes, labeled #101. *Id.* at Fig. 1. Regarding (2), Complainant has already agreed that an identifier is distinct from a start code for the construction of “identifier.”

Resps. Br. at 119.⁵⁶

The administrative law judge construes “start code” to mean “a code of a varying number of bits that indicates the start of a packet.” *See* Broadcom Br. at 247 (“a POSA would have understood that a ‘start code’ is simply that, a code of a varying number of bits that indicates the start of a packet[.]”). Broadcom’s proposed construction of “plain and ordinary meaning” does not provide a basis for understanding the term or their limits. The explanation in its brief, however, is informative and does not improperly expand or narrow the term. Respondents’ proposed construction, on the other hand, adds words that appear to limit the term based on the specification. *See* JX-0002 at 5:17-20 (“start code 101 may comprise a plurality of bytes that

⁵⁶ The parties agree that “identifier” means “an indication of a video encoding type distinct from a start code.” Resps. Br. at 119; Broadcom Br. at 246.

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may be arranged in a unique combination to signify the beginning of the encapsulated video payload 100 within an encoded video stream.”).

C. Whether Sigma Infringes the Asserted Claims

Broadcom asserts claims 11-20. *See* Broadcom Br. at 248. Claims 12-20 depend from claim 11. JX-0002 at 20:31-21:4.

1. Claim 11

Claims 11, which Broadcom divides into five limitations, follows:

11. [preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:

- [A] receiving on a chip, packetized data within the encoded video stream;
- [B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;
- [C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and
- [D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.

JX-0002 at 20:15-30.

- a) *[preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:*

Broadcom argues, in part:

To the extent [the preamble] is determined to be a limitation of the claim, the SX-6 SoC satisfies the preamble of claim 11. CX-0003C (Acton WS) at Q/A 182-86.

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Respondents suggest that the preamble is not met because the computer program stored on the computer-readable storage must be located on the SX-6 SoC in order for the SX-6 to infringe. RX-1079C (Stevenson WS) at Q/A 99-109. But, when the SX-6's code is executed by the [], the execution occurs on the chip itself. CX-0003C (Acton WS) at Q/A 183-186. And as Dr. Stevenson acknowledged during trial, [] on the SX-6 when the program is executed. Tr. (Stevenson) at 649:1-650:9 (citing CX-0350C.0095). Additionally, even if the computer program were not stored on the SX-6, the claim language is clear that the computer-readable storage does not need to be located on the chip, it only needs to execute code that causes the recited steps to occur on a chip. JX-0002 ('059 Patent) at cl. 11.

Further, the claims themselves only require that the computer program be executable to *perform* a series of steps. This is consistent with the '059 Patent's specification, which makes clear that, in what Dr. Stevenson acknowledges is the only discussion of "machine" in the '059 Patent, "[a]nother embodiment of the invention may provide a machine-readable storage, having stored thereon, a computer program having at least one code section executable by a machine, *thereby causing the machine to perform the steps* ... for processing an encoded video stream." JX-0002 ('059 Patent) at 3:7-11; RX-1079C at Q/A 108. As Dr. Stevenson admits, processors located on the SX-6, [

]. Tr. (Stevenson) at 605:3-611:18, 614:2-615:7; CX-0003 (Acton WS) at Q/A 182-205. Additionally, Dr. Stevenson acknowledged that during his deposition he testified that the []
].” Tr. (Stevenson) at 659:16-660:16.

Broadcom Br. at 248-50.

Sigma argues:

The SX6 does not comprise a “computer-readable storage having stored thereon, a computer program. . . .” Dr. Acton testified that “[]” that meets this limitation. Tr. (Acton) 127:24; CX-0003C at Q183. But the SX6 Reference Platform Block Diagram depicts [] as not part of the SX6. RX-0614C; RX1079C at Q99 (“[

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]”). During cross examination, Dr. Acton admitted that [] is not part of the SX6 itself. Tr. (Acton) 129:10-13, 128:4-8. That is why the claimed program does not (and cannot) exist on the SX6 when it is powered off. Tr. (Acton) 129:14-17. Therefore, the SX6 does not meet this limitation.

Resps. Br. at 134.

Broadcom replies:

During trial, Dr. Acton explained, and Dr. Stevenson admitted, that when the SX6 executes code parts of the computer program are moved into memory on the SX6. Tr. (Acton) at 232:12-233:17; Tr. (Stevenson) at 649:1-650:9 (citing CX-0350C.0095). This establishes that the SX6 comprises “computer-readable storage.” CPostHB at 248-250, 252. Thus, Sigma’s assertion that the SX6 does not comprise “computer-readable storage” because the storage is located off the SX6 chip is unfounded and fails. RPostHB at 134.

Broadcom Reply at 84.

Having considered the parties’ arguments, the administrative law judge has determined that Broadcom has not shown, by a preponderance of the evidence, that the SX-6 SoC includes computer-readable storage that has a computer program stored on it. In particular, the claimed computer program is stored on the [], not on the SX-6. *See* RX-1079C (Stevenson RWS) at Q/A 102; *see also* Acton Tr. 127-128 (testifying that the [] “actually stores the code” and that the [] are “external to the SX-6”).

Dr. Acton’s testimony argues that a code section is stored on the SX-6 SoC when it is executed. CX-0003C (Acton WS) at Q/A 183 (“[

]”). Dr. Acton, however, does not actually identify any memory on the chip. Likewise,

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Broadcom’s reliance on Dr. Stevenson’s testimony does not show that the chip includes memory for storing the program; Dr. Stevenson testified that “a portion of the code gets moved onto the RAM *for execution*.” Stevenson Tr. 650 (emphasis added).

Accordingly, Broadcom has not shown that the SX-6 SoC satisfies the preamble.

b) [A] receiving on a chip, packetized data within the encoded video stream;

Broadcom argues:

The evidence shows that the SX-6 SoC's [_____, _____], and thus this limitation is satisfied. CX-0003C (Acton WS) at Q/A 187-91. Sigma does not dispute that this claim limitation is met under Broadcom's construction.

Broadcom Br. at 250.

Sigma does not clearly rebut this argument. *See generally* Resps Br. at 134-37 (contesting the preamble and limitations [B] and [D]); Resps. Reply, Section III(B)(2).

The evidence and argument cited in Broadcom’s brief shows that the SX-6 SoC receives packetized data within an encoded video stream, as limitation [A] requires. *See, e.g.*, CX-0003C (Acton WS) at Q/A 187-91. Accordingly, the administrative law judge has determined that the SX-6 SoCs satisfy this limitation.

c) *[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;*

(1) Analysis of Broadcom's Argument

Broadcom argues:

The undisputed evidence shows that the SX-6 [] to determine the encoding format. Tr. (Acton) at 609:1-19; CX-0003C (Acton WS) at Q/A 192-95.

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Sigma does not dispute that this claim limitation is met under Broadcom's construction of "packetized data within the encoded video stream," which encompasses a transport stream.

Broadcom Br. at 250.

Sigma does not clearly rebut this argument under Broadcom's construction. *See generally* Resps Br. at 134-35 (contesting infringement when the term "packetized data within the encoded video stream" is "[p]roperly construed"); Resps. Reply, Section III(B)(2).

The evidence and argument cited in Broadcom's brief shows that, under Broadcom's construction, the SX-6 SoC determines an identifier within received packetized data as limitation [B] requires. *See, e.g.*, CX-0003C (Acton WS) at Q/A 192-95. Accordingly, the administrative law judge has determined that the SX-6 SoCs satisfy this limitation under Broadcom's construction.

(2) Analysis of Respondents' Argument

Broadcom argues:

Claim 11 further requires "determining on said chip, an identifier within said packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream." Sigma argues that the SX-6 does not infringe this limitation based on Respondents' attempt to limit the term "packetized data within the encoded video stream" to "a packetized elementary video stream," alleging that the SX-6's [] identifier (Tr. (Stevenson) at 609:1-9) is not within the "packetized elementary video stream." RX-1079C (Stevenson WS) at Q/A 116. However, the [] identifier is located in the packetized elementary video stream packet data when the incoming encoded video stream is a "program stream." CX-0003C (Acton WS) at Q/A 196. Specifically, when the packetized elementary video stream packet's header has a certain [

]” *Id.* Thus, the SX-6 SoC also infringes under Respondents' proposed claim construction.

Broadcom Br. at 253.

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Sigma's entire argument is:

Claim 11 requires "determining . . . an identifier within said received packetized data . . .," and "said received packetized data" is the "packetized data within the encoded video stream." Properly construed, "packetized data within the encoded video stream" is a "packetized elementary video stream." RX-0424; RX-1079C at Q116. Thus, the claim identifier must be found within a "packetized elementary video stream." Broadcom has identified the syntax [] as the alleged "identifier" in the SX6. CX-0003C.67 at Q 193; RX-1079C at Q173.

But, the syntax [] is not within a "packetized elementary video stream." Tr. (Acton) at 110:19-112:16; 150:12-15. Rather, it is in a transport stream. *Id.* Dr. Acton admitted this during cross examination. *Id.* While Broadcom asserts infringement even under Respondents' construction, [] is never found within a *video* elementary stream under any of Broadcom's theories, as discussed in § V.C.1.a.ii.(a) *supra*. CX-0003C at Q196; RX-1079C at Q117. Thus, the SX6 does not infringe this limitation.

Resps. Br. at 134-35.

If respondents' construction is adopted, the administrative law judge has determined that the SX-6 SoC does not satisfy limitation [B]. In the SX-6 SoC, the chip receives a transport stream, which does not necessarily include video data. *See* RX-1083C (Bovik WS) at Q/A 216-17 ("a transport stream does not necessarily include video data"); Acton Tr. 110-112; *see also* RX-1079C (Stevenson RWS) at Q/A 116, 173 ("... [] is not within a packetized elementary video stream. Rather, it is found in the transport stream. . . .").

Accordingly, the administrative law judge has determined that the SX-6 SoCs do not meet this limitation under respondents' construction.

- d) *[C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and*

Broadcom argues:

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Claim 11 further requires “selecting on said chip, a decoding process from a plurality of decoding processes based on said identifier.” The evidence shows that this limitation is satisfied because the SX-6 [] identifier to select a decoding process. CX-0003C (Acton WS) at Q/A 197-200. Sigma does not dispute that this claim limitation is met under Broadcom’s construction of “packetized data within the encoded video stream,” where [] in the transport stream satisfies claim element 11[b].

Broadcom Br. at 250.

Sigma does not clearly rebut this argument. *See generally* Resps Br. at 134-37 (contesting the preamble and limitations [B] and [D]); Resps. Reply, Section III(B)(2).

The evidence and argument cited in Broadcom’s brief shows that the SX-6 SoC selects a decoding process based on the identifier, as limitation [C] requires. *See, e.g.*, CX-0003C (Acton WS) at Q/A 197-200. Accordingly, the administrative law judge has determined that the SX-6 SoCs satisfy this limitation.

- e) ***[D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.***

Broadcom’s entire argument is:

Lastly, claim 11 requires “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.” Dr. Acton testified that the SX-6 also satisfies this limitation. CX-0003C (Acton WS) at Q/A 201-05.

Respondents assert that the SX-6 does not infringe because in the SX-6 decoding is done by the hardware, and thus it does not include a code section that performs decoding. RX-1079C (Stevenson WS) at Q/A 109-115. But, Dr. Stevenson testified that during his deposition he acknowledged that the [] can do “some software-based decoding.” Tr. (Stevenson) at 659:16-660:16. While this establishes infringement, Dr. Acton also explained that the SX-6’s processors orchestrate and control decoding by []

], which

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Respondents do not dispute. CX-0003C (Acton WS) at Q/A 201-05; RX-1079C (Stevenson WS) at Q/A 110, 113.

Broadcom Br. at 251.

Sigma argues, in part:

Claim 11 requires a “code section being executable by a machine to *perform* ... decoding ...” JX-0002 at claim 11 (emphasis added). For purposes of claim 1 of the ‘844 Patent, Broadcom alleges that the [] controls decoding. CX-0003C at Q155. In contrast, for claim 11 of the ‘059 Patent, Broadcom alleges the software executed by the [] decodes. *Id.* at Q183-205. Neither of [] processors, however, performs decoding. Rather, the decoding is performed in the []
[]. RX-1079C at Q109; RX-0613.00020, .28 ([

]). Indeed, nowhere does the SX6 execute computer code to perform decoding. RX-1079C at Q109.

The [] in the SX6 may orchestrate the overall decoding process, but *orchestration* of decoding is not the same as *performing* the decoding operations as required in claim 11 of the ‘059 Patent. RX-1079C at Q110. Broadcom refers to code that is run on the [] to support its infringement allegations. RX-1079C at Q111; CX-0003C at Q183-205. Its expert, Dr. Acton, asserts that the [] ... causes the SoCs video decoder to decode.” See CX-0003C at Q201-202. Dr. Acton thus is suggesting that the claim 11 is satisfied because there is a computer program executed by the [], which “causes” the video decoder to decode; *i.e.*, [

[]. RX-1079C at Q111-113. If the claim were written “causing decoding,” then Dr. Acton’s suggestion may have some merit – but the claim is not written in this manner. *Id.* In the SX6, non-processor circuitry in the [] performs the actual decoding—not the []
[]. RX-1079C at Q113; RDX-0059C ([]
[]); RX-0613C.00020, 28. Thus,

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neither the machine-executable code of the [] performs “decoding” of the received packetized data utilizing the selected decoding process, as recited by the claim. RX-1079C at Q113.

Resps. Br. at 135-36.

Broadcom replies:

Sigma’s remaining non-infringement arguments are based on its misunderstanding of the scope of the ‘059 Patent. While Sigma asserts that the SX6 cannot infringe because it does not use a software program to perform decoding, and does not have a processor that executes code to perform the recited steps of claim 11 (RPostHB at 135-137), neither of these are required by claim 11. Instead, claim 11 simply requires that the computer program be executable by a machine, resulting in the machine’s performance of the recited steps. CPostHB at 249. Additionally, and contrary to Sigma’s assertions, the machine is a chip. Tr. (Acton) at 230:4-11. And both Dr. Acton and Dr. Stevenson agree that the SX6 chip contains processors, which execute code that results in the machine, or chip, performing the recited steps. Tr. (Stevenson) at 605:3-611:18, 614:2-615:7; CX-0003 (Acton WS) at Q/A 182-205. Additionally, contrary to Respondents’ assertion that the SX6’s processors do not perform decoding (RPostHB at 136-137), Dr. Stevenson acknowledged at trial that during his deposition he testified that the [] can do “some software-based decoding.” Tr. (Stevenson) at 659:16-660:16. Sigma’s non-infringement arguments fall flat and the SX6 infringes claim 11.

Broadcom Reply at 85.

The administrative law judge has determined that Broadcom has not shown that the SX-6 decodes packetized data in an encoded video stream. Dr. Acton’s witness statement explains that “the SX6 source code operating on the [] which is controlling the decoding process that is used in the multi-standard video decoder” and that “the hardware decodes at least a portion of the packetized data in the encoded video stream.” CX-0003C (Acton WS) at Q/A 202. This, however, does not show that Sigma’s SX-6 SoC is “decoding on said chip,” as claim 11 requires. *See* RX-1079C (Stevenson RWS) at Q/A 109 (“the decoding is

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performed in the [], in hardware – not software – and this hardware is controlled by the [].”). Accordingly, the administrative law judge has determined that the SX-6 SoCs do not satisfy this limitation.

Thus, in sum, the administrative law judge has determined that the SX-6 does not infringe claim 11.

2. Claims 12-20

Broadcom’s entire argument is:

The evidence shows that the SX-6 infringes each of dependent claims 12-20 of the ‘059 patent when those claims are properly construed as Broadcom has proposed. CX-0003C (Acton WS) at Q/A 206-22. With respect to claims 12-20, Sigma does not present any non-infringement arguments other than the arguments presented for independent claim 11. Accordingly, if the SX-6 is found to infringe claim 11, it also infringes dependent claims 12-20.

Broadcom Br. at 251.

Sigma’s entire argument is:

Claims 12-20 depend from claim 11. The Sigma Accused SoCs do not infringe dependent claims 12-20 for the same reasons as claim 11. RX-1079C at Q119-136.

Resps. Br. at 137.

The administrative law judge has determined that Sigma’s SX-6 SoC does not infringe claim 11. Accordingly, the administrative law judge finds that the SX-6 SoC does not infringe claims 12-20 based on their dependency from claim 11. *See Ferring, supra*.

D. Whether VIZIO Infringes the Asserted Claims

Broadcom’s entire argument is:

The Accused VIZIO Products []. *See* Acc. Prods. Stmt. Specifically, the only accused VIZIO products at issue in this Investigation are the

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VIZIO products [] identified in Exhibit F to the Joint Statement Regarding Identification of Accused Products. As Dr. Acton testified, any consumer audiovisual product containing an accused SoC, [], which, as discussed above is representative of the [], infringes claims 11-20 of the '059 Patent. *See, e.g.*, CX-0003C at Q/A 10, 223.

Broadcom Br. at 254.

VIZIO argues that its products “do not infringe any claim of the '059 Patent at least [] does not infringe those claims.” Resps. Br. at 138.

VIZIO also argues that Broadcom has failed to show how the VIZIO products operate, and therefore cannot establish that its products ([]) infringe the asserted claims.

Id. (*e.g.*, “Broadcom has failed to provide any evidence or testing to show that capability or to establish the functionality of final code in the accused VIZIO products.”) VIZIO further argues:

In addition, similar to Broadcom’s failure of proof for its infringement opinions [], as Dr. Acton testified at the hearing, Broadcom also failed to identify a “computer readable storage” in VIZIO’s product that would satisfy claim 11. Rather, Dr. Acton confined his analysis []. Tr. (Acton) 129:18-22; 130:6-10 (“[My witness statement] doesn’t contain any additional information as to what’s in the VIZIO accused products, no.”); 133:1-4. And he explicitly admitted that he did not determine whether any software for the [] was ever loaded into memory of a VIZIO accused product. Tr. (Acton) 134:8-11; *see also* Tr. (Stevenson) 662:7-11-663:6; 666:22-24. As Dr. Stevenson testified, however, []. Tr. (Stevenson) 667:7-20. Thus, Broadcom has not shown the VIZIO products have the claimed “computer readable storage.”

Resps. Br. at 139.

Broadcom replies:

[] infringes '059 Patent claims 11-20. *See* CPostHB at 247-254. Accordingly, any VIZIO consumer audiovisual product [] infringes these claims. *See, e.g.*, CX-0003C (Acton WS) at Q/A 10, 223. And while

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VIZIO argues it does not infringe the '059 Patent due to Broadcom's lack of testing of VIZIO products, these arguments fall flat for the same reasons discussed above with respect to the '104 Patent.

Additionally, VIZIO's assertion that the VIZIO products do not infringe because Dr. Acton failed to identify a "computer readable storage" in VIZIO's product that would satisfy claim 11 is false. As Dr. Acton explicitly testified, and Dr. Stevenson agreed, [] includes a computer-readable storage. Tr. (Acton) at 232:12-233:17; Tr. (Stevenson) at 649:1-650:9.

Broadcom Reply at 86.

The administrative law judge has determined that VIZIO products [

] do not infringe claim 11 [

]. Additionally, the administrative law judge has determined that Broadcom has failed to show that the VIZIO products include computer-readable storage, as the preamble of claim 11 requires. *See* Acton Tr. 129-130 ("[My witness statement] doesn't contain any additional information as to what's in the VIZIO accused products, no."). The memory discussed at Acton Tr. 232-233 and Stevenson Tr. 649-650 shows that the [] memory, not on the []. Broadcom and Dr. Acton have not identified the [

] in VIZIO's products (assuming VIZIO's products include these components).

Accordingly, the administrative law judge finds that the VIZIO products do not infringe claim 11. Further, the administrative law judge finds that the VIZIO products do not infringe the dependent claims, claims 12-20, based on their dependency from claim 11. *See Ferring, supra.*

E. Whether Broadcom Practices Claims 11-20

Broadcom argues that the "Broadcom DI Products, as represented by the [], practice claims 11-20 of the '059 Patent (JX-0002)." Broadcom Br. at 267. Broadcom provides argument under its constructions and respondents' constructions. *Id.* at 267-272.

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1. Claim 11

- a) *[preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:*

Broadcom argues:

The preamble of claim 11 recites “A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising.” There is no dispute that the [] practices this claim limitation. CX-0003C (Acton WS) at Q/A 277-79.

Broadcom Br. at 268.

Respondents argue:

Limitation 11[p]: To the extent the preamble is limiting, the [] does not comprise a “computer-readable storage having stored thereon, a computer program. . . .” Dr. Acton opined that [] meets this limitation. CX-0003C.98 (Acton) Q278; Tr. (Acton) 113:24-114:4. But, as Dr. Acton admits, and [

] Tr. (Acton) 114:5-17; CX-0057C.0018. That program does not exist on the [] Tr. (Acton) 114:24-115:8. Therefore, the [] does not meet this limitation.

Resps. Br. at 140.

Broadcom replies:

Limitation 11[p]: Respondents did not contend that the [] failed to practice the preamble of claim 11 in their Pre-hearing Brief. RPreHB at 194. Thus, under Ground Rule 7 this argument is deemed withdrawn. Regardless, contrary to Respondents’ assertions, to the extent the preamble is limiting, the [] practices the preamble. CPostHB at 268. And, while the recited computer program may not be located on the [] until the TV is turned on and the decoding functions begin, that is all that is required of claim 11. There is no

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requirement that the [] be capable of performing the recited steps, and in fact it would be nonsensical for it to perform the recited steps while the TV is off.

Broadcom Reply at 86.

Respondents reply:

With respect to the preamble of claim 11, Broadcom's Post-Hearing Brief relies solely on Dr. Acton's witness statement, but disregards the fact that during cross examination Dr. Acton admitted that the []

[] Tr. (Acton) 113:24-114:11; *see also* CX-0057C.0018. Therefore, by his own admission, the [] does not meet this limitation.

Resps. Br. at 61.

The administrative law judge has determined that respondents have waived any argument concerned whether the [] practices the preamble. Respondents' pre-hearing brief is silent on the preamble. *See generally* Resps. Pre-Hr'g Br. at 194-97 (contesting limitations [B] and [C] only). Additionally, respondents failed to ascertain Dr. Stevenson's opinion with respect to the preamble. *See* RX-1079C (Stevenson RWS) at Q/A 168-183 (providing testimony on limitations [B] and [C] only). Ground Rule 7 requires the parties to set forth their contentions in their prehearing briefs. Order No. 4 (Ground Rules) at 10 ("Any contentions not set forth in detail as required therein shall be deemed abandoned or withdrawn, except for contentions of which a party is not aware and could not be aware in the exercise of reasonable diligence at the time of filing the prehearing statement."). Respondents were aware of the contention regarding the physical separation of the host chip and memory, as respondents offered this theory as to why the SX-6 SoC does not infringe claim 11. By failing to include this theory (with respect to the []) in their pre-hearing brief, respondents have waived it. Accordingly, the administrative law judge finds that the [] satisfies the preamble.

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- b) *[A] receiving on a chip, packetized data within the encoded video stream;*

Broadcom argues:

Claim 11 further requires “receiving on a chip, packetized data within the encoded video stream.” The parties do not dispute that the [] practices this claim limitation. CX-0003C (Acton WS) at Q/A 280.

Broadcom Br. at 269.

Sigma does not clearly rebut this argument. *See generally* Resps Br. at 140-41(contesting the preamble and limitations [B] and [C]); Resps. Reply, Section III(B)(2).

The evidence and argument cited in Broadcom’s brief shows that the [] receives packetized data within an encoded video stream, as limitation [A] requires. *See, e.g.*, CX-0003C (Acton WS) at Q/A 280-82. Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

- c) *[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;*

(1) Analysis of Broadcom’s Argument

Broadcom, under its construction, argues:

Claim 11 further requires “determining on said chip, an identifier within said packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream.” There is no dispute that the [] practices this claim limitation under the plain and ordinary meaning of “packetized data within the encoded video stream,” which encompasses a transport stream because the parties agree that the []
[]. CX-0003C at Q/A 283-85; RX-1079C (Stevenson WS) at Q/A 173.

Broadcom Br. at 269.

Respondents argue, in part:

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The [] SoC does not comprise limitation 11[b]. RX-1079C.0038 (Stevenson) Q173. As Broadcom's expert states, the [

]” RX-1079C.0039 (Stevenson) Q173; CX-0003C.0100 (Acton) Q284. But Dr. Acton admitted that [

] Tr. (Acton) 112:12-16, 150:12-15; *see also* RX-1079C.0039 (Stevenson) Q173. [

] RX-1079C.0039 (Stevenson) Q173. [

] SoC, therefore, is not a determination of “an identifier within said received packetized data” because [] is not *within a packetized elementary video stream. Id.*

...

Resps. Br. at 140-41 (emphasis added on arguments presented under respondents' construction).

In footnote 29, respondents add:

The plain and ordinary meaning (as proposed by Complainant) of the relevant disputed terms would match or closely align with constructions proposed by Respondents. RX-1079C (Stevenson) Q174. Thus, the domestic industry products would not practice this limitation under either construction. *Id.*

Id. at 140, n.29. Dr. Stevenson testified that “for the reasons I just stated [under Respondents' construction], Broadcom's domestic industry products would not practice this limitation under the plain and ordinary meaning.” RX-1079C (Stevenson RWS) at Q/A 174.

The administrative law judge has determined that, under Broadcom's construction, the [] determines an identifier within received packetized data as limitation [B] requires. *See, e.g.,* CX-0003C (Acton WS) at Q/A 283-85. Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

(2) Analysis of Respondents' Argument

Under respondents' construction, Broadcom argues:

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Respondents contend that the [] does not practice this limitation based on Respondents' attempt to limit the term "packetized data within the encoded video stream" to "a packetized elementary video stream," alleging that the [] does not include an identifier within the "packetized elementary video stream." RX-1079C (Stevenson WS) at Q/A 170-74. The evidence shows, however, that the [] practices this limitation under either claim construction because the []

[] CX-0003C (Acton WS) at Q/A 286.

Broadcom Br. at 271.

Respondents argue:

The [] SoC does not comprise limitation 11[b]. RX-1079C.0038 (Stevenson) Q173. As Broadcom's expert states, the []

[] as the claimed "identifier." RX-1079C.0039 (Stevenson) Q173; CX-0003C.0100 (Acton) Q284. But Dr. Acton admitted that [] cannot be *within a packetized elementary video stream packet*. Tr. (Acton) 112:12-16, 150:12-15; *see also* RX-1079C.0039 (Stevenson) Q173. Rather, it is found in the transport stream. RX-1079C.0039 (Stevenson) Q173. Parsing of []

[] SoC, therefore, is not a determination of "an identifier within said received packetized data" because [] is not *within a packetized elementary video stream*. *Id.*

Regarding the Broadcom's alternative theory for the [], Dr. Acton testified that it processes []

[]." RX-1079C.0039 (Stevenson) Q173; CX-0003C.000-101 (Acton) Q284. But, according to Dr. Acton, "stream_id" is part of a start code. Tr. (Acton) at 118:6-12, 120:22-121:1. Further, Dr. Acton states that [], but provides no indication of what those [] are, how they are used, or how they identify an encoding type. RX-1079C.0039 (Stevenson) Q173. Broadcom failed to prove its alternative theory.

Resps. Br. at 140-41 (emphasis added on arguments presented under respondents' construction).

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If respondents' construction is adopted, the administrative law judge has determined that the [] does not satisfy limitation [B]. In the [] (like the SX-6 SoC), the chip receives a []

Accordingly, the administrative law judge has determined that the [] does not meet this limitation under respondents' construction.

- d) *[C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and*

Broadcom argues:

Claim 11 further requires "selecting on said chip, a decoding process from a plurality of decoding processes based on said identifier." There is no dispute that the [] practices this limitation under Broadcom's constructions. Additionally, as Dr. Acton testified, the []

[] is based on the identified standard, regardless of how the standard is identified. CX-0003C (Acton WS) at Q/A 287-89.

Broadcom Br. at 269.

Respondents' entire argument is:

The purported [] of the [] SoC does not comprise limitation 11[c]. RX-1079C.0040 (Stevenson) Q175. Dr. admitted that he did not provide any evidence that the [] to select a decoding process. Tr. (Acton) 117:13-22; *see also* RX-1079C.0040 (Stevenson) Q175. Thus, the entirety of Dr. Acton's testimony for this limitation is limited to []." *Id.*; *see also* CX-0003C.0101-102 (Acton) Q288.

Resps. Br. at 141.

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Dr. Acton testified as follows:

Q287. Have you formed an opinion as to whether the [] SoC satisfies the “selecting on said chip a decoding process from a plurality of decoding processes based on said determined identifier” limitation of claim 11?

A. Claim 11 further requires “selecting on said chip a decoding process from a plurality of decoding processes based on said determined identifier.” This limitation is also satisfied Broadcom’s [] code, operating on the SOC’s [] selects on said chip, a decoding process from a plurality of decoding processes based on said determined identifier.

Q288. Please explain the bases for your opinion.

A. Broadcom’s [] code includes code that analyzes the [] in order to determine the encoding type associated with the packets in the [] For example the source code file [], which is CPX-044C-SC, selects a decoding process from a plurality of processes based on the identifier. Some examples of the decoding processes are MPEG 1, MPEG2, MPEG4, H.264, H.265, AVS, and VC-1.

As shown in [], which is CX-0051C, there are []

[] such that there is a different decoding process for each decoding standard.

The particular protocol specific decoding process is based on the identified standard passed down from the []

[]. Page 30 of the [], which is CX0149C, shows that the [], which is CX-0051C, explains that the []

[].” Page 58 further explains that the “[]

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].”

As shown in Figure 5 in the [] Page
15 of the []

].”

As shown in Figure 8 in the [] Pages 18
and 19 of the []

[] Specifically, the
[]

].”

Accordingly, the [] causes the
[] to “select[] on said chip a decoding process from a
plurality of decoding processes based on said determined
identifier.”

**Q289. Did you review anything other than the documents and
source code in rendering your opinion?**

A. Yes, I also read the transcript of Broadcom’s 30(b)(6) witness,
Mr. Timothy Hellman. Mr. Timothy Hellman confirmed that the
[] selects on said chip a decoding process from a
plurality of decoding processes based on said determined
identifier, which can be seen in his deposition transcript at 344:24-
355:12.

CX-0003C (Acton WS) at Q/A 287-89.

Dr. Stevenson testified as follows:

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Q175. What is your opinion on whether the [] comprises a computer program causing a machine to execute the step of “selecting . . . a decoding process from a plurality of decoding processes based on said determined identifier”?

A175. I refer to this limitation as 11[c]. The purported media probe of the [] SoC does not comprise limitation 11[c]. Dr. Acton has provided no opinion that the purported [] purportedly determined by it are ever used to select a decoding process. The entirety of Dr. Acton’s testimony for this limitation is cabined to [].” See CX-0003C-0101-0102. Thus, Dr. Acton has provided no support for the [“] satisfying limitation 1[c].

RX-1079C (Stevenson RWS) at Q/A 175.

Having considered the parties’ arguments, the administrative law judge has determined that the [] selects a decoding process based on the identifier, as limitation [C] requires. In particular, the evidence shows that the [] analyzes the [

[] based upon the identifier. See CX-0003C (Acton WS) at Q/A 288. Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

e) [D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.

Broadcom argues:

Lastly, claim 11 requires “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.” There is no dispute that the [] practices this limitation under Broadcom’s constructions. CX-0003C (Acton WS) at Q/A 290-91.

Broadcom Br. at 269-70.

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Sigma does not clearly rebut this argument. *See generally* Resps Br. at 140-41(contesting the preamble and limitations [B] and [C]); Resps. Reply, Section III(B)(2).

The evidence and argument cited in Broadcom's brief shows that the [] decodes the packetized data from the encoded video stream using the selected decoding process, as limitation [D] requires. *See, e.g.*, CX-0003C (Acton WS) at Q/A 290-91. Accordingly, the administrative law judge has determined that the [] satisfies this limitation.

Thus, in sum, the administrative law judge has determined that the [] practices claim 1.

2. Claims 12-20

Broadcom's entire argument is:

The evidence shows that the [] practices dependent claims 12-20 when those claims are properly construed as proposed by Broadcom. CX-0003C (Acton WS) at Q/A 292-303. With respect to claims 12-20, Respondents do not present any non-infringement contentions other than those presented for independent claim 11. Accordingly, if the [] is found to practice claim 11, it also practices dependent claims 12-20.

Broadcom Br. at 270.

Respondents' entire argument is:

[], or any other Broadcom SoC, does not practice dependent claims 12-20 of the '059 Patent at least for the reasons discussed with regard to claim 11, from which they depend.

Resps. Br. at 141.

The administrative law judge previously determined that the [] practices claim 11. Based on the parties' arguments, the administrative law judge finds that the [] also practices claims 12-20. *See* CX-0003C (Acton WS) at Q/A 292-303.

F. Patent Eligibility

Respondents argue that claims 11-20 are not eligible for patenting because they “cover transitory media” and, per *CLS Bank v. Alice*, “because they are: (1) directed to patent-ineligible subject matter (the abstract idea of using an identifier attached to information (*i.e.*, video data) to select a way to process the information (*i.e.*, a decoding process)); and (2) lack an inventive concept and are performed in a generic video decoding environment.” Resps. Br. at 141-142.

1. Transitory Media

Respondents argue, in part:

When claims are broad enough to cover transitory memory, the law is clear—the claims are invalid. *See In re Nuijten*, 500 F.3d 1346, 1356-57 (Fed. Cir. 2007). Claims 11-20 of the ‘059 Patent cover transitory computer readable storage. The asserted claims recite “computer-readable storage” but do not in any limit the storage to non-transitory elements. Further, asserted claims do not specify any physical memory structure, nor do the dependent claims add any such physical limitations. The asserted claims require only that the computer readable medium store “a computer program having at least one code section for processing an encoded video stream . . .” Therefore, any means of computer readable storage will suffice for all of the claims at issue. So long as some object or medium stores the computer program, it falls within that claim’s scope regardless of its physical form. Indeed, Broadcom points to the transmission of the program onto volatile memory of certain accused products as satisfying the asserted claims. Tr. (Acton) at 232:12-233:17 (“[T]he MIPS moves the code from flash to the on chip RAM.”). In sum, some form of storage is required, but any form will do, so long as a recipient computer can read the program from the storage medium. Thus, guided by the specification, one of ordinary skill would readily understand that transitory forms of storage, such as a satellite signals, would not fall outside of the scope claims. *See* RX-0383C.0074-0075 (Stevenson) Q297.

Resps. Br. at 141-42.

The administrative law judge construed “computer-readable storage” to mean “non-transitory computer-readable storage.” *See* § VI(B)(3)(b), *supra*. Respondents’ arguments

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that the asserted claims are ineligible (under *Nuijten*) for claiming transitory computer-readable are presented under their proposed construction. *See* Resps. Br. at 111 (“Respondents propose that the term “computer-readable storage” in claim 11 should be construed, consistent with its plain meaning in view of the ‘059 Patent, as transitory and non-transitory computer-readable storage.”). The administrative law judge finds that respondents have not shown the asserted claims are patent-ineligible when they cover non-transitory computer-readable storage only.

2. *Alice* Eligibility

Respondents’ entire argument is:

Based on the evidence presented in the hearing, claims 11-20 of the ‘059 Patent are invalid because they are: (1) directed to patent-ineligible subject matter (the abstract idea of using an identifier attached to information (*i.e.*, video data) to select a way to process the information (*i.e.*, a decoding process)); and (2) lack an inventive concept and are performed in a generic video decoding environment. Further, nothing in the claims improves or changes the way a computer functions. Rather, as is demonstrated by the prior art, it was well-known before the ‘059 Patent to use an identifier to select a video decoding process. *See* § E.2, *infra*. Indeed, it was **standardized**.

Nowhere does the specification describe an “identifier” as something other than the conventional, well-understood elements within video streams as defined by encoding standards of the time, which the ‘059 Patent acknowledges were well-known. JX-0002 (‘059 Patent) at 2:15-18; 18:37-44, Fig. 9. This is confirmed by Broadcom’s assertion that the accused identifier is the “stream_type” syntax of the transport stream or MPEG-2 Systems. Tr. (Acton) at 110:17-12. Stream_type predates the ‘059 Patent by years. RX-0383C.0072-73 (“[i]n 2000, the stream_type of the MPEG-2 Systems standard specified ‘the type of the stream’ and included a value for ISO-IEC 11172-2 Video (MPEG-1 Video) of ‘0x01,’ a value for ISO-IEC 13818-2 (MPEG-2 Video) or MPEG-1 constrained parameter of ‘0x02,’ and a value for ISO-IEC 14496-2 (MPEG 4 Video) of ‘0x10’...”). Other identifiers, such as the identifier in Kovacevic, also predate the ‘059 Patent, as is discussed further below. *See* § E.2, *infra*.

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Moreover, the specification makes it clear that the invention may function on general purpose computer components and, therefore, only trivially moves the abstract idea into the computing realm. JX-0002 ('059 Patent) at 18:45-56 ("Any kind of computer system or other apparatus adapted for carrying out the methods described herein is suited."); *see Intellectual Ventures I LLC v. Symantec Corp.*, 838 F.3d 1307, 1318 (Fed. Cir. 2016); *In re TLI Communications LLC Patent Litigation*, 823 F.3d 607, 613 (Fed. Cir. 2016). None of the physical components recited in Claim 11 provide an inventive concept because each is a generic component used commonly in claims. *See Elec. Power Grp. LLC v. Alstom, S.A.*, 830 F.3d 1350, 1355 (Fed. Cir. 2016). It is undisputed that "computer-readable storage" and "a machine" are not inventive as used in the '059 Patent. JX-0002 ('059 Patent) at 18:57-19:17, 19:45-46. The same is true for the term "a chip," which the inventor of the '059 Patent admits is nothing more than a generic computer component. *See* RX-0670C at 127:3-7, 127:13-18.

Further, all of the additional limitations in the claims recite well-known, routine, and conventional functions. *See Content Extraction v. Wells Fargo Bank*, 776 F.3d 1343, 1349 (Fed. Cir. 2014). They do not add anything more beyond well-known, conventional activities, or recite standardized aspects of the relevant video encoding standards which are unrelated to the abstract idea. Thus, claims 11-20 are invalid.

Resps. Br. at 142-44 (emphasis in original).

Broadcom's post-hearing brief does not address respondents' *Alice* arguments. *See generally* Broadcom Br., Section V(B)(6); Joint Outline at 7 (relying on Order No. 36). In reply, Broadcom argues: "Despite having already lost this argument, Respondents again argue that claims 11-20 are unpatentable under *Alice*. RPostHB at 142-144. 'Respondents have not shown, as a matter of law, that claim 11 is directed to an abstract idea.' Order No. 36 at 5 (Dec. 1, 2017)." Broadcom Reply at 87.

In Order No. 36, the administrative law judge found:

[T]hat respondents have not shown, as a matter of law, that claim 11 is directed to an abstract idea, devoid of a concrete or tangible application. Rather, Claim 11 is tied to a tangible application—multi-standard decoding of video streams. This differs from other

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claims that have been found ineligible, such as those directed to pre-roll advertising or media categorization. *See, e.g., Ultramercial*, 772 F.3d at 715 (“The process of receiving copyrighted media, selecting an ad, offering the media in exchange for watching the selected ad, displaying the ad, allowing the consumer access to the media, and receiving payment from the sponsor of the ad all describe an abstract idea, devoid of a concrete or tangible application. . . . the concept embodied by the majority of the limitations describes only the abstract idea of showing an advertisement before delivering free content.”); *Certain Portable Electronic Devices and Components Thereof*, Inv. No. 337-TA-994, Initial Determination at 33-34 (Aug. 19, 2016) (finding claim directed toward a method of using categories to access media was patent-ineligible) (un-reviewed by 81 Fed. Reg. 66295 (Sep. 27, 2016)), *aff’d by Creative Tech. Ltd. V. U.S. Int’l Trade Comm’n*, 698 Fed. Appx. 1033 (Fed. Cir. 2017) (Rule 36 affirmance).

Order No. 36 at 5-6 (footnote omitted).^{57, 58}

Respondents’ post-hearing argument does not explain how claim 11 is directed toward an abstract idea. Indeed, respondents’ argument focuses on how the identifier lacks an inventive concept. *See* Resps. Br. at 142-44 (respondents do not include an abstract-idea argument); *see also* Resps. Reply, Section IV(D) (respondents do not present any eligibility challenges).⁵⁹ Accordingly, the administrative law judge has determined that respondents have not shown the asserted claims are ineligible under *Alice*.

⁵⁷ The administrative law judge finds that respondents have not met their burden regardless of whether the patent is presumed valid or if it is afforded no presumption of validity. *See* 35 U.S.C. § 282 (“A patent shall be presumed valid.”).

⁵⁸ In *Ultramercial v. Hulu*, the Federal Circuit found claim 1 of U.S. Patent No. 7,346,545 did not claim patent-eligible subject matter. 772 F.3d at 711-12. Claim 1 was directed toward a “method of distribution of products over the Internet via a facilitator[.]”

⁵⁹ If the patent claims an abstract idea, the court in the second step seeks to identify an “inventive concept” sufficient to ‘transform’ the claimed abstract idea into a patent-eligible application.” *Alice*, 134 S. Ct. at 2357.

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G. Anticipation – Kovacevic

Respondents argue that U.S. Patent Publication No. US 2005/0060420 (“Kovacevic”) (RX-0337) “anticipates claims 11-14 and 19 of the ‘059 Patent.” Resps. Br. at 146.

Respondents argue:

U.S. Patent Publication No. US 2005/0060420 (“Kovacevic”) was filed on Sept. 11, 2003 and was published on March 17, 2005. RX-0383C.0080-0081 (Stevenson) Q327; RX-0337 (Kovacevic). Kovacevic thus qualifies as prior art under 35 U.S.C. §§ 102(e) and 103(a).

Id. at 144.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 273-79 (discussing Kovacevic without disputing its prior-art status); Broadcom Reply, Section IV(D) (same).

Accordingly, the administrative law judge has determined that Kovacevic is prior art under 35 U.S.C. § 102(e).

1. Claim 11

- a) ***[preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:***

Respondents argue:

Kovacevic discloses limitation 11[pre]. RX-0383C.0082 (Stevenson) Q332; RDX-0013.00002-00004. Kovacevic discloses that its multimedia processing system uses a microcode engine, which includes a processor, for processing a video data stream. RX-0383C.0082 (Stevenson) Q332; RX-0337 (Kovacevic) at ¶ 0029. Stored microcode is executed by the processor of a transport stream demultiplexor to processes received video data packets. RX-0383C.0082 (Stevenson) Q332; *see* RX-0337 (Kovacevic) at ¶ 0029. Kovacevic also discloses a MIPS core processor. RX-0383C.0082 (Stevenson) Q332; *see* RX-0337 (Kovacevic) at ¶ 0032. The MIPS core also processes received

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data packets. RX-0383C.0082 (Stevenson) Q332; *see* RX-0337 (Kovacevic) at ¶ 0032. The processors execute the microcode to perform decoding. RX-0383C.0082 (Stevenson) Q332. Dr. Acton does not contest that Kovacevic discloses this limitation.

Alternatively, it would have also been obvious to one of ordinary skill that a computer-readable storage would store microcode, and the microcode would have a code section for processing an encoded video stream according to the methods described by Kovacevic. RX-0383C.0082 (Stevenson) Q332.

Resps. Br. at 147-48.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 274-76 (contesting limitations [B], [C], and [D]); Broadcom Reply, Section III(D) (contesting limitation [B]).

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Kovacevic discloses a computer-readable storage. In particular, Dr. Stevenson testified as follows:

Q332. Let's discuss the individual limitations of claims 11-20 of the '059 patent in comparison to the Kovacevic reference. Let's start with claim 11. Does Kovacevic disclose the limitation "a computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising"?

A332. Yes. Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Kovacevic discloses that the multimedia processing system makes use of a microcode engine, which includes a micro-programmable sequencer or microprocessor for processing the stream. [RX-0337 (Kovacevic) at ¶ 0029]. The stored microcode includes commands for the microprocessor, which is used to process received data packets. [See RX-0337 (Kovacevic) at ¶ 0029]. Kovacevic also discloses a MIPS core, which can be a RISC processor. [See RX-0337 (Kovacevic) at ¶ 0032]. The MIPS core is also used to process received data packets. [See RX-0337 (Kovacevic) at ¶ 0032]. *It would have been*

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obvious to a POSITA that computer code would be stored in computer readable memory.

RX-0383C (Stevenson WS) at Q/A 332 (emphasis added). Dr. Stevenson, however, has not identified a memory in Kovacevic that meets the requirements of the preamble (*i.e.*, requiring non-transitory computer-readable storage). Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Kovacevic discloses subject matter that satisfies the preamble.

b) [A] receiving on a chip, packetized data within the encoded video stream;

Respondents argue:

Kovacevic discloses “receiving on a chip, packetized data within the encoded video stream.” RX-0383C.0082 (Stevenson) Q333; RDX-0013.00005-00013. Kovacevic’s system can process MPEG-1 and MPEG-2 data. RX-0383C (Stevenson) Q333; *see* RX-0337 (Kovacevic) at ¶¶ 0060-65; *see* RX-0337 (Kovacevic) at ¶ 0004 and ¶ 0060. The data can include program and elementary streams, which are processed by the transport stream demultiplexer. RX-0383C (Stevenson) Q333; *see* RX-0337 (Kovacevic) at ¶ 0060-66. In particular, the program stream is organized into a collection of packs, which include a collection of video elementary stream packets that can be parsed from the program stream. RX-0383C (Stevenson) Q333; *see* RX-0337 (Kovacevic) at ¶ 0005.

Respondents’ Construction: In the discussion of Figure 11, microcode is executed by the transport stream demultiplexer to first parse the data stream based in part on a “pack start code,” which is a syntax of a program stream, then based in part on a “packet start code,” which in this embodiment is a syntax of an video elementary stream. RX-0383C.0083 (Stevenson) Q335; *see* RX-0337 (Kovacevic) at ¶¶ 0004-05, 0060-66. Thus, Kovacevic discloses receiving “packetized elementary video streams” by the transport stream demultiplexer. *Id.*

Complainant’s Construction: For these same reasons, Kovacevic also satisfies Complaint’s construction—plain and ordinary meaning. RX-0383C.0083 (Stevenson) Q336.

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Resps. Br. at 148-49.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 274-76 (contesting limitations [B], [C], and [D]); Broadcom Reply, Section III(D) (contesting limitation [B]).

The evidence and argument cited in respondents' brief shows that Kovacevic's system (*e.g.*, multimedia system **100**) receives packetized data within an encoded video stream, as limitation [A] requires. *See, e.g.*, RX-0383C (Stevenson WS) at Q/A 333-36. Accordingly, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Kovacevic discloses subject matter that satisfies this limitation.

- c) ***[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;***

Respondents argue:

Kovacevic discloses "determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream." RX-0383C.0083 (Stevenson) Q337; RDX-0013.00013-00028. In the embodiment associated with Fig. 11, Kovacevic discloses a system for determining whether an incoming data stream is MPEG-1 or MPEG-2 video based on an identifier called "next byte." RX-0383C.0083 (Stevenson) Q337; *see* RX-0337 (Kovacevic) at ¶ 0060.

During processing, the microcode executed by the transport stream demultiplexor analyzes elementary stream packets to determine whether the packets begin with a start code value of 0x000001 (step 745). RX-0383C (Stevenson) Q337; RX-0337 (Kovacevic) at ¶ 0063. If so, it optionally filters the packets based on stream_id (step 750) and then extracts the packet length (step 755 (Fig. 11)). RX-0383C (Stevenson) Q337; *see* RX-0337 (Kovacevic) at ¶ 0063; Fig. 11. After packet length extraction, it determines whether the "next byte" is of value "0xFF," which is hexadecimal for binary "1111 1111" (step 760). RX-0383C (Stevenson) Q337; RX-0337 (Kovacevic) at ¶¶ 0064-65. If so, it parses the received packet as an MPEG-1 packet (step 764). RX-0383C (Stevenson)

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Q337; *see* RX-0337 (Kovacevic) at ¶ 0065. Otherwise, it parses the packet as an MPEG-2 packet (step 762). RX-0383C (Stevenson) Q337; *see* RX-0337 (Kovacevic) at ¶¶ 0060-65. Therefore, next byte, with the values 0xFF or not 0xFF, is an identifier that Kovacevic uses to define the MPEG-1 or MPEG-2 encoding types, respectively, associated with the received packets in the video stream. RX-0383C (Stevenson) Q337-Q338.

Although “next byte” can identify both MPEG-1 and MPEG-2, all that claim 11 requires is an “identifier . . . that defines one of a plurality of encoding types . . .” JX-0002 (‘059 Patent) (emphasis added). Broadcom’s expert, Dr. Acton, admitted several times during the hearing that “next byte” can “identify” MPEG-1, which is one of the two decoding types (*i.e.*, MPEG-1 Video and MPEG-2 Video). Tr. (Acton) at 871:22-872:12 (“[Next byte] can identify MPEG-1 . . .”); 873:18-21; 879:12-16; RDX-0672. Thus, the “next byte” identifier of Kovacevic clearly satisfies claim 11.

Dr. Acton, however, at first argued that “next byte” could not be an identifier because it was “stream_id” and part of a start code (CX-0579 (Acton) Q231), but he was wrong. It is neither. RX-0383C.0084 (Stevenson) Q339. Indeed, at the hearing, Dr. Acton recanted and admitted that Dr. Stevenson’s interpretation of Kovacevic “sounded like a reasonable explanation” and that “next byte” was not part of the start code or stream_id. Tr. (Acton) at 870:9-871:24; RDX-0672. This is because, in the scenario of Fig. 11, the values of “next byte” follow the “packet length” bytes in the packet header, and the “packet length” bytes are in turn positioned after “stream_id” and the “packet start code” in the packet header. RX-0383C.0084 (Stevenson) Q339; *see* RX-0337 (Kovacevic) at Fig. 11, ¶¶ 0063-0065; RX-0096.0027 at Section 2.4.3.3 Packet Layer; RX-0099.00049-00051 at Table 2-21 – PES packet; *see* RDX-0672. Thus, the values of “next byte” are separated from the “stream_id” and the “packet start code” in the packet header at least by the “packet length” bytes. RX-0383C.0084 (Stevenson) Q339.

Resps. Br. at 149-50.

Broadcom argues:

Respondents’ expert, Dr. Stevenson, alleges that the “identifier” in Kovacevic is Kovacevic’s “next byte.” As Dr. Acton testified, however, Kovacevic’s “next byte” is not an identifier because, while Kovacevic does not explicitly define the “next byte,” it could

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be the `stream_id`, which is part of the start code. CX-0579C (Acton WS) at Q/A 231.

At trial, Dr. Stevenson expanded on his previous testimony and opined for the first time that Kovacevic's "next byte," which consists of eight ones, is the stuffing byte in MPEG-1. Tr. (Stevenson) at 721:11-722:1. Based on this clarification, and reviewing the MPEG-1 standard and Kovacevic, Dr. Acton later agreed that Dr. Stevenson's explanation seemed reasonable. Tr. (Acton) at 872:2-12. As Dr. Stevenson acknowledged, paragraph [0064] of Kovacevic explains that the value being looked for in the next byte is 0xFF, which equals eight ones. Tr. (Stevenson) at 717:21-24. In the MPEG-1 standard, the stuffing byte equals eight ones. *Id.* at 720:19-722:1. So Kovacevic uses the stuffing byte to identify MPEG-1. *Id.* at 722:2-23.

But, as Dr. Acton explained, while Kovacevic's "next byte" can identify MPEG-1, it is not actually able to identify a *plurality* of standards because if the seventh byte is anything other than eight ones Kovacevic calls it MPEG-2. Tr. (Acton) at 879:6-19. Thus, Kovacevic can only identify a single standard, MPEG-1. *Id.* Kovacevic does not identify MPEG-2, it simply calls everything that is not MPEG-1, MPEG-2. *Id.* This means that a stream encoded using any other standard, such as H.264 or VC-1 would default to MPEG-2. Additionally, in some cases Kovacevic's next byte would not even successfully identify MPEG-1 because in some instances the seventh byte in an MPEG-2 stream can be a padding byte, consisting of eight ones, which would result in Kovacevic erroneously determining that the received stream was encoded using MPEG-1. Tr. (Acton) at 873:21-874:7. Accordingly Kovacevic does not disclose the claimed "identifier."

Broadcom Br. at 274-75.

The parties agreed that "identifier" means "an indication of a video encoding type distinct from a start code." Resps. Br. at 119; Broadcom Br. at 246.

The administrative law judge has determined that respondents have not shown that Kovacevic discloses a chip equipped to determine an identifier that defines an encoding type, as limitation [B] requires. Dr. Stevenson testified that Kovacevic's system determines whether "an unknown incoming data stream is MPEG-1 or MPEG-2 video" by analyzing packets for a

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particular start code, *i.e.*, 0x000001. RX-0383C (Stevenson WS) at Q/A 337. If the system identifies that start code, it extracts the packet as an MPEG-1 packet. If the system identifies any other code, the system defaults to MPEG-2. *Id.* (“Otherwise, the system parses the packet as an MPEG-2 packet.”). Thus, according to Dr. Stevenson, Kovacevic’s system can only determine one video encoding type—MPEG-1. *Id.* This is not sufficient to show that Kovacevic is capable of ascertaining two video types. *See* CX-0579C (Acton RWS) at Q/A 230-33; Acton Tr. 873-874 (“If -- if we assumed that we could identify a red balloon and we assumed that all other balloons were green, could we identify a green balloon? Not really, because there might be some blue balloons in the world. And we wouldn’t really be identifying green balloons, we would just have an identifier for a red balloon.”). Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Kovacevic discloses subject matter that satisfies limitation [B].

d) [C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and

Respondents’ anticipation argument is:

Kovacevic discloses “selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier.” The system will choose which decoding scheme to use—MPEG-1 or MPEG-2—based on the value of “next byte.” RX-0383C.0084 (Stevenson) Q340; RDX-0013.00028-00032 *see* RX-0337 (Kovacevic) at ¶¶ 0063-0065. For example, “If it is determined the next byte has a value equal to hexadecimal value of 0xFF, it is determined the received packet is associated with MPEG-1 data,” and “the transport stream demultiplexor [will then] parse[] optional MPEG-1 header data associated with the received packet.” RX-0383C.0084 (Stevenson) Q340; RX-0337 (Kovacevic) at ¶ 0065. Similarly, the transport stream demultiplexor will parse an MPEG-2 header data if the value is not 0xFF. RX-0383C.0084 (Stevenson) Q340; *see* RX-0337 (Kovacevic) at ¶ 0065. This is selecting one of two possible decoding processes, MPEG-1 or MPEG-2 header parsing, based on the value of “next byte.” RX-0383C.0084 (Stevenson) Q340; *see*

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RX-0337 (Kovacevic) at Fig. 11. Broadcom's expert has opined that parsing the elementary stream is decoding. Tr. (Acton) at 124:8-21 ("So at this point, we're already into the elementary stream, which in this case is all video. And yes, **parsing is part of decoding.**") (emphasis added). And because the packet headers in Kovacevic are in the video elementary stream, Dr. Acton's testimony supports Dr. Stevenson's opinion that parsing of those packet headers is a decoding process. RX-0383C (Stevenson) Q335, Q34.

Dr. Acton argues that Kovacevic cannot select a decoding process because decoding has already begun. CX-0579C (Acton) at Q 233. But whether decoding has started is irrelevant. Claim 11 requires selection of a decoding process based on an identifier. It does not state selection of a decoding process before any decoding has begun. Decoding can start before it is necessary to determine which encoding type is being decoding. Indeed, this is exactly what Kovacevic discloses. See RX-0383C.0084 (Stevenson) Q340; RX-0337 (Kovacevic) at ¶ 0065 ("If it is determined the next byte has a value equal to hexadecimal value of 0xFF, it is determined the received packet is associated with MPEG-1 data," and "the transport stream demultiplexor [will then] parse[] optional MPEG-1 header data associated with the received packet.").

Resps. Br. at 150-51 (emphasis in original).

Broadcom argues:

Respondents also failed to show that Kovacevic discloses "selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier" because, as discussed above, Kovacevic does not disclose determining an identifier. Additionally, as Dr. Acton explained, after determining whether a PES packet is encoded as MPEG-1, Kovacevic simply discloses routing the packet payload data and provides no information about this routing step, let alone where the payload packet is routed, or that the routing is based on the identified encoding standard. CX-0579C (Acton WS) at Q/A 233.

Broadcom Br. at 275-76.

The administrative law judge has determined that Kovacevic does not disclose selecting a decoding process based on the identifier, as limitation [C] requires. In particular, as discussed with respect to limitation [B], Kovacevic does not disclose an identifier, and thus also does not

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disclose selecting a decoding process based on the identifier.⁶⁰ See CX-0579C (Acton RWS) at Q/A 233.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Kovacevic discloses subject matter that satisfies limitation [C].

- e) ***[D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.***

Respondents' anticipation argument is:

Kovacevic discloses this limitation. RX-0383C.0087 (Stevenson) Q347; RDX-0013.00049-00054. Kovacevic discloses that elementary stream packet headers are parsed according to MPEG-1 or MPEG-2 based on the protocol of the received input stream identified by "next byte." RX-0383C.0087 (Stevenson) Q347; see RX-0337 (Kovacevic) at Fig. 5, Fig. 11, ¶¶ 0004-05, 0025, 0065-66 (e.g., "[T]he transport stream demultiplexor *parses optional MPEG-2 header data.*"). As discussed for limitation 11[c], parsing elementary stream packet headers is a decoding process.

Resps. Br. at 155.

Broadcom argues:

Respondents further have not shown that Kovacevic discloses "decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process" because as discussed above, Kovacevic does not select a decoding process. Kovacevic also does not disclose any hardware or software used for decoding. Instead, Kovacevic simply shows that the data stream is sent to a decoding or display device, not that it is actually decoded. CX-0579C (Acton WS) at Q/A 238. Respondents have not established, by clear and convincing evidence, that Kovacevic discloses or renders obvious claim 11.

⁶⁰ If it is later determined that Kovacevic discloses an identifier per limitation [B], the administrative law judge would find that Kovacevic discloses selecting a decoding process based on the identifier, as limitation [C] requires. See RX-0383C (Stevenson WS) at Q/A 340.

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Broadcom Br. at 276.

The administrative law judge has determined that Kovacevic does not disclose decoding packetized data with the previously selected decoding process, as limitation [D] requires.

Kovacevic does not disclose the decoding limitation because it does not disclose limitation [C], which is where a decoding process is selected. *See* CX-0579C (Acton RWS) at Q/A 238.

Further, respondents have not identified, from Kovacevic, the relevant hardware or software used for decoding. Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that Kovacevic discloses subject matter that satisfies limitation [D].

2. Claim 12

Claim 12 follows:

12. The computer-readable storage according to claim 11, comprising code for determining on said chip, a start code within said received packetized data that separates packets within the encoded video stream.

JX-0002 at 20:31-34.

Respondents argue:

Kovacevic and/or Kovacevic-Chu disclose this limitation. RX-0383C (Stevenson) Q349; RDX-0013.71-74. They disclose a number of different start codes that are used to separate packets within the encoded video stream. For example, in discussing Fig. 11, the microcode executed by the transport stream demultiplexor determines “if a packet start code of a received packet is equal to a hexadecimal value of 0x000001.” RX-0383C (Stevenson) Q349; RX-0337 (Kovacevic) at ¶¶ 0029, 59, 63, Fig. 11.

Respondents’ Construction: Respondents’ claim construction requires that the start code be “distinct from the identifier.” In Kovacevic, the disclosed start code—0x000001—is distinct from the identifier—“next byte.” RX-0383C (Stevenson) Q351; RX-0337 (Kovacevic) at Fig. 11. As previously described, “next byte” is based on values that are separated from the start code in

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the packet header at least by the “packet length” bytes. RX-0383C (Stevenson) Q351; RX-0096.27; RX-0099.49-51.

Complainant’s Construction: For these same reasons, Complaint’s construction—plain and ordinary meaning—is satisfied. RX-0383C.0088 (Stevenson) Q352.

Resps. Br. at 155-56.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579 (Acton WS) at Q/A 243-271.

Broadcom Br. at 279.

The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 12 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 243-246 (“It is my opinion that Kovacevic does not disclose claim 12 for the same reasons that I discussed with respect to claim 11.”). Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 12.

3. Claim 13

Claim 13 follows:

13. The computer-readable storage according to claim 12, comprising code for matching a plurality of bytes within said received packetized data with a determined byte sequence.

JX-0002 at 20:35-37.

Respondents argue:

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Based on the knowledge of one ordinary skill at the time of the '059 Patent, Kovacevic and/or Kovacevic-Chu anticipate and/or render obvious claim 13. RX-0383C.0088 (Stevenson) Q353. Kovacevic discloses a number of different byte patterns that the system uses to identify specific portions of the received packetized data. RX-0383C.0088 (Stevenson) Q353; RDX-0013.00074-00077. For example, as described with respect to claim 12, the microcode executed by the transport stream demultiplexor searches the received bytes for a start code value of 0x000001. RX-0383C.0088 (Stevenson) Q353; *see* RX-0337 (Kovacevic) at RX-0337 (Kovacevic) at ¶¶ 0029, 0059, 0063, Fig. 11. If the bytes match that determined sequence, processing continues. *Id.* Kovacevic also discloses stuffing bytes. RX-0383C.0088 (Stevenson) Q353; *see* RX-0337 (Kovacevic) at ¶¶ 0064-65. One of ordinary skill would understand that stuffing bytes would have to have a predetermined value so that the system could properly recognize and remove them from the stream. RX-0383C (Stevenson) Q353.

Resps. Br. at 156.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579 (Acton WS) at Q/A 243-271.

Broadcom Br. at 279.

The entirety of Dr. Stevenson's testimony regarding claim 13 follows:

Q353. Does Kovacevic disclose claim 13?

A353. Yes. Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Kovacevic discloses a number of different byte patterns that the system uses to identify specific portions of the received packetized data. For example, as discussed with respect to claim 12, Kovacevic discloses that the system searches the received bytes for a start code value of 0x000001. [See RX-0337 (Kovacevic) at 63 & Fig. 11]. If the packet bytes match that determined sequence, processing continues. *Id.* Similarly, Kovacevic discloses stuffing bytes. [See RX-0337 (Kovacevic) at ¶¶ 0064-65]. A POSITA would understand that stuffing bytes

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would have to have a predetermined value so that the system could properly recognize and remove them from the packetized stream.

RX-0383C (Stevenson WS) at Q/A 353.

The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 13 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton WS) at Q/A 247-48 (“It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 13 for the same reasons that I discussed with respect to claims 11 and 12.”). In addition, Dr. Stevenson’s testimony is inconsistent with regard to which legal doctrine he intended to apply, and thus is not clear and convincing evidence.

Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 13.

4. Claim 14

Claim 14 follows:

14. The computer-readable storage according to claim 13, comprising code for removing said plurality of bytes from said received packetized data, if said plurality of bytes matches said determined byte sequence.

JX-0002 at 20:38-41.

Respondents’ anticipation argument follows:

Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 14 obvious. RX-0383C.0088 (Stevenson) Q354; RDX-0013.00077-00078. The microcode executed by the transport stream demultiplexor removes a plurality of bytes from the stream if they match the determined value discussed with respect to claim 13 above. RX-0383C.0088 (Stevenson) Q354; *see* RX-0337 (Kovacevic) at RX-0337 (Kovacevic) at ¶¶ 0029, 0059, 0063-0065, Fig. 11. For example, Kovacevic discloses stuffing bytes, which one of ordinary skill would understand could be removed.

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RX-0383C.0088 (Stevenson) Q354; *see* RX-0337 (Kovacevic) at ¶¶ 0064-65.

Resps. Br. at 156-57 (respondents subsequently present further obviousness arguments).

Broadcom argues:

Respondents have not shown that Kovacevic, alone or in combination with secondary references, discloses or renders obvious claim 14, which requires “code for removing said plurality of bytes from said received packetized data, if said plurality of bytes matches said determined byte sequence.” Dr. Acton testified Kovacevic does not disclose or render obvious claim 14 because Kovacevic discloses that stuffing data can be ignored, which is different from removing a plurality of bytes. CX-0579C (Acton WS) at Q/A 250.

Broadcom Br. at 276-77.

The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 14 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 250 (“It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 14 for the same reasons that I discussed with respect to claims 11-13.”). In addition, Kovacevic does not disclose removing a plurality of bytes from packetized data, as claim 14 requires. Paragraphs 29, 59, and 63-65 of Kovacevic do not discuss removing bytes. *See* RX-0337 at ¶¶ 29, 59, 63-65 (¶¶ 64-65 discuss ignoring stuffing data); CX-0579C (Acton RWS) at Q/A 250 (“Ignoring a stuffing byte, however, is not the same as removing a plurality of bytes.”). Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 14.

5. Claim 15

Claim 15 follows:

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15. The computer-readable storage according to claim 11, comprising code for decoding said at least a portion of said received packetized data utilizing one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process and/or a context adaptive binary arithmetic coding (CABAC) process, if said determined identifier corresponds to H.264 video encoding.

JX-0002 at 20:42-48.

Respondents argue, in part:

To the extent Kovacevic and/or Kovacevic-Chu do not anticipate and/or render obvious this limitation one of ordinary skill would have been motivated to modify those grounds to incorporate the disclosures of H.264 to render claim 15 obvious. RX-0383C.0090 (Stevenson) Q359; RDX-0013.00080-00094. . . .

Resps. Br. at 158.

Broadcom argues:

Respondents have not shown that Kovacevic, alone or in combination with secondary references, discloses or renders obvious claim 15, which requires “code for decoding said at least a portion of said received packetized data utilizing one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process and/or a context adaptive binary arithmetic coding (CABAC) process, if said determined identifier corresponds to H.264 video encoding.” Respondents have not shown that Kovacevic discloses using one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process, and/or a context adaptive binary arithmetic coding (CABAC) process for decoding at least a portion of the received packetized data because Kovacevic does not disclose decoding any portion of the packetized data. CX-0579C (Acton WS) at Q/A 255. Additionally, Respondents have not established by clear and convincing evidence that a POSA would be motivated to modify Kovacevic to process H.264 encoded video streams, or modify Kovacevic in view of the H.264 standard, because in paragraph [0066] Kovacevic explicitly states that it simply “exploit[s] similarities between MPEG-1 and MPEG-2 data to process both MPEG-1 and MPEG-2 data using a single methodology.” CX-0579C (Acton WS) at Q/A 257.

Broadcom Br. at 277.

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The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 15 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 254 (“It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 15 for the same reasons that I discussed with respect to claim 11.”). In addition, Kovacevic does not disclose use of the H.264 standard. *Id.* (“Kovacevic only discloses being able to determine, using start codes, whether an encoded video stream is encoded as MPEG-1 or MPEG-2, and not H.264.”). Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 15.

6. Claim 16

Claim 16 follows:

16. The computer-readable storage according to claim 11, comprising code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to VC-1 video encoding.

JX-0002 at 20:49-53.

Respondents have not argued that Kovacevic anticipates claim 16. *See* Resps. Br. at 160 (“Based on the knowledge of one ordinary skill at the time of the ‘059 Patent, Kovacevic and/or Kovacevic-Chu renders claim 16 obvious. RX-0383C (Stevenson) Q364; RDX-0013.94-102. One of skill would have known of the VC-1 standard, and that it includes fixed and variable length coding.”); *but see* Joint Outline at 6 (presenting “Kovacevic (claims 11-17 and 19)” as a “validity” issue to be determined).

Broadcom argues, in part:

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Respondents have not shown that Kovacevic, alone or in combination with secondary references, discloses or renders obvious claim 16, which requires “code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to VC-1 video encoding.” Additionally, Respondents have not established by clear and convincing evidence that a POSA would be motivated to modify Kovacevic to process VC-1 encoded video streams because, as discussed above, Kovacevic explicitly states at paragraph [0066] that it is directed to “exploiting similarities between MPEG-1 and MPEG-2 data.” CX-0579C (Acton WS) at Q/A 259.

Broadcom Br. at 277-78.

The administrative law judge finds that respondents has failed to show that Kovacevic anticipates claim 16 because respondents have not presented any argument or cited any evidence on this issue. Indeed, the testimony cited, Q/A 364, immediately presents an obviousness argument:

Q364. Does the Kovacevic reference disclose claim 16?

A364. Kovacevic may be modified/supplemented according to the knowledge of a POSITA in view of admitted prior art in the '059 patent to disclose this limitation. A POSITA would have found . . .

RX-0383C (Stevenson WS) at Q/A 364.

Accordingly, the administrative law judge determines that respondents have failed to show that Kovacevic anticipates claim 16.

7. Claim 17

Claim 17 follows:

17. The computer-readable storage according to claim 11, comprising code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to one or more of H.261, H.263, H.263+, MPEG-1, MPEG-2 and/or MPEG-4 video encoding.

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JX-0002 at 20:54-59.

Respondents' anticipation argument follows:

Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 17 obvious. RX-0383C.0092 (Stevenson) Q370; RDX-0013.00102-00124. Kovacevic discloses that the system microcode executed by the transport stream demultiplexor processes MPEG-2 Video packets. RX-0383C.0092 (Stevenson) Q374; *see* RX-0337 (Kovacevic) at ¶¶ 0029, 0059, 0065. One of ordinary skill would have understood that MPEG-2 Video incorporates both fixed and variable length coding processes. RX-0383C.0092 (Stevenson) Q374; *see* RX-0670.0143-0145 (Gordon) at 140:21-142-11; CX-0003C.0007 (Acton) at Q22. Thus, one of ordinary skill would have understood that decoding MPEG-2 Video packets utilizes FLC and VLC processes. RX-0383C.0092 (Stevenson) Q374.

Resps. Br. at 162.⁶¹

Broadcom argues:

Respondents have not shown that Kovacevic discloses or renders obvious claim 17, which requires "code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to one or more of H.261, H.263, H.263+, MPEG-1, MPEG-2 and/or MPEG-4 video encoding.". Additionally, Respondents have not established by clear and convincing evidence that Kovacevic discloses using one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process, and/or a context adaptive binary arithmetic coding (CABAC) process for decoding at least a portion of the received packetized data because Kovacevic does not disclose decoding the packetized data. CX-0579C (Acton WS) at Q/A 261.

Broadcom Br. at 278-79.

⁶¹ It is not clear whether respondents are actually arguing that Kovacevic anticipates claim 17. *See* Resps. Br. at 146 ("[The] Kovacevic reference anticipates claims 11-14 and 19 of the '059 Patent."); RX-0383C (Stevenson WS) at Q/A 330 ("In my opinion, the Kovacevic reference anticipates claims 11-14 and 19 of the '059 Patent under either party's claim constructions. Alternatively, it is my opinion that the Kovacevic reference renders obvious claims 11-20 of the '059 Patent under either party's constructions."); *but see* Joint Outline at 6 (presenting "Kovacevic (claims 11-17 and 19)" as a "validity" issue to be determined).

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The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 17 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 261 (“It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 17 for the same reasons that I discussed with respect to claim 11.”). In addition, Kovacevic does not disclose using one or more of a fixed length coding (FLC) process or a variable length coding (VLC) process for decoding at least a portion of the received packetized data because Kovacevic does not disclose decoding any portion of the packetized data. *Id.* Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 17.

8. Claim 19

Claim 19 follows:

19. The computer-readable storage according to claim 11, comprising code for generating a decoded video stream utilizing at least a portion of said decoded packetized data.

JX-0002 at 20:65-67.

Respondents argue:

Kovacevic and/or Kovacevic-Chu disclose claim 19. RX-0383C.0094 (Stevenson) Q376; RDX-0013.00137-00142. As discussed above, Kovacevic discloses that microcode executed by the transport stream demultiplexor processes and parsing data streams. RX-0383C.0094 (Stevenson) Q376; *see* RX-0337 (Kovacevic) at ¶¶ 0025, 0029, 0064-65. Broadcom’s expert has opined that parsing is decoding. Tr. (Acton) at 124:8-21; RX-0383C.0048 (Stevenson) Q376. Thus, Kovacevic’s parsing of “header data associated with the received packet” is decoding a video stream. *Id.* at 0094.

Resps. Br. at 164.

Broadcom argues:

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Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579 (Acton WS) at Q/A 243-271.

Broadcom Br. at 279.

The administrative law judge previously determined that Kovacevic does not anticipate claim 11. The administrative law judge finds that Kovacevic does not anticipate claim 19 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 267 (“It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 19 for the same reasons that I discussed with respect to claim 11.”). In addition, the portion of Kovacevic that Dr. Stevenson relies on (*i.e.*, ¶ 0025) does not explicitly disclose generating a decoded video stream utilizing at least a portion of said decoded packetized data. *See* RX-0383C (Stevenson WS) at Q/A 376 (citing RX-0337 (Kovacevic), ¶ 25 only). Paragraph 25 follows:

[0025] Referring now to FIG. 5, a block diagram illustrating a system for processing multimedia data is shown and referenced generally as multimedia system 100, according to one embodiment of the present invention. Multimedia system 100 processes multiplexed data streams from a plurality of multimedia sources, such as a multimedia tuner 110 and a multimedia device 117 for display on a display device 190. Multimedia system 100 includes a transport stream demultiplexor 130, a stream interface 140, a memory controller 150, memory 160, an overlay 170, and a microprocessor, such as a microprocessor without interlocked pipeline stages (MIPS) core 180.

RX-0337 (Kovacevic), ¶ 25. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that Kovacevic anticipates claim 19.

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H. Anticipation – Quasar Chip

Respondents argue: “The EM8550 Quasar chip anticipates or renders obvious claims 11-20 of the ‘059 Patent under Complainant’s proposed claim constructions.” Resps. Br. at 176.

Respondents further argue:

The EM8550 Quasar chip, which was introduced subsequent to the EM8300 and EM8475 Quasar chips, is the prior art that illustrates the invalidity of the ‘059 Patent claims. As with the EM8300 and EM8475 chips, the testimony of Sigma engineer Michael Ignaszewski confirms the EM8550 was known, on sale, in use, and/or described at least as early as 2004. RX-668C at Q/A 47-62. Because the EM8550 Quasar chip was publicly available before the priority date of the ‘059 Patent, it is prior art to the patent under at least 35 U.S.C. § 102(a) and/or 103(a). RX-668C at Q17-18, 34, 40-41, 47-62; RX-383C at Q432; *see also* § IV.E.6.a, *supra*.

Id. at 174.

In reply, Broadcom argues:

The Quasar Chips are not prior art: As was the case with the Quasar Chips asserted against the ‘844 Patent, Respondents have failed to establish by clear and convincing evidence that the EM8550 was “in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention” because their only evidence is the uncorroborated testimony of Mr. Ignaszewski. Mr. Ignaszewski, however, relies on two products containing chips other than the EM8550 as evidence of the EM8550’s public availability, no actual evidence for the EM8550 itself, and for all of the chips he relies on, he provides no evidence corroborating his testimony that any of these chips “were available before April 2004.” RX-0668C (Ignaszewski WS) at Q/A 42-67. As discussed above, however, this is insufficient to establish that the products were known, on sale, in use, and/or described prior to April 2004. *See supra* Section III.D.

Broadcom Reply at 89.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 Quasar chip is prior art. Respondents rely on Mr. Michael Ignaszewski’s witness statement

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(RX-0668C). Resps. Br. at 174 (citing RX-0668C (Ignaszewski WS) at Q/A 17-18, 34, 40-41, 47-62. Respondents, however, have not shown that the EM8550 was the subject of a commercial offer of sale or in public use. In particular, Mr. Ignaszewski's unsupported testimony regarding what was on sale roughly 14-16 years ago, *e.g.*, RX-0668C (Ignaszewski WS) at Q/A 52, 59-61 does not show that the products were on sale or publicly used. For example, Mr. Ignaszewski's testimony about a Christmas present from 2002 is not an adequate foundation from which to conclude the whether the 8550 chip is prior art. *Id.* at Q/A 52. Finally, the administrative law judge notes that respondents do not cite documents typically used to establish a commercial sale or public use (*e.g.*, sales orders or receipts, product catalogs, brochures, flyers, or advertisements) to support their contention that the 8550 chip is prior art.

Accordingly, respondents have not shown, through clear and convincing evidence, that the EM8550 is prior art to the '059 Patent.

In the event that the EM8550 is determined to be prior art, respondents have argued that the EM8550 chip, as discussed in RX-0329C, and its predecessor chips, the EM8300 and EM8475 (as discussed in RX-0325, RX-0326, RX-0327, and RX-0328), anticipate claims 11-20 of the '059 patent.

1. Claim 11

- a) *[preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:*

Respondents argue:

Under Respondents' construction, to the extent that the SX6 includes a "computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising," then so

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does the EM8550 Quasar chip. This is because [

RX-668C at Q64; RX-0383C at Q437; Tr. (Ignaszewski) at 482:4–
484:14, 489:1-2.

Resps. Br. at 177-78.

Broadcom argues:

Respondents have not shown that either the “Quasar Chip” references or “Quasar Chip” system disclose any of claim 11’s recited limitations. For example, to the extent the preamble is limiting, Respondents have not shown that the “Quasar Chip,” anticipates or renders obvious a computer program having at least one code section for processing an encoded video stream because [

]. CX-0579C (Acton WS) at Q/A 365.

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Broadcom Br. at 285-86.

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 discloses a computer-readable storage. *See, e.g.*, RX-0383C (Stevenson WS) at Q/A 437 (I

)). I

]. *Id.*; *see also* CX-0579C (Acton RWS) at Q/A 365.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 includes or discloses subject matter that satisfies the preamble.

b) *[A] receiving on a chip, packetized data within the encoded video stream;*

Respondents argue:

Under a construction where Sigma's accused SX6 infringes limitation 11[a] ("receiving on a chip, packetized data within the encoded video stream"), Sigma's EM8550 Quasar chip anticipates or renders obvious the '059 Patent for the same reasons. RX-0383C at Q438. The EM8550 in particular was a [

].] The EM8550, [

]. *Id.*;

RX-0668C at Q60.

Resps. Br. at 178.

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Broadcom argues:

Respondents also have not shown that the “Quasar Chip” references or “Quasar Chip” system disclose [

].

Broadcom Br. at 286.

Having considered the parties’ arguments, the administrative law judge has determined that the EM8550 (*i.e.*, the chip) [

]; RX-0329 at 8, 35-36, Fig. 34. Accordingly, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that the EM8550 includes or discloses subject matter that satisfies limitation [A].

- c) *[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;*

Respondents argue:

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The Quasar Chip discloses [

RX-0383C at Q439; RX-0668C at Q67; Tr. at 488-489.]

Resps. Br. at 178-79.

Broadcom argues:

Further, even if these limitations were met, Respondents have not shown by clear and convincing evidence that the “Quasar Chip” references or system disclose using an identifier to determine an encoding type because. [

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].

Broadcom Br. at 286-87.

Respondents have not shown, through clear and convincing evidence, that the EM8550 determines an identifier within the received packetized data, as limitation [B] requires. For example, Dr. Stevenson [

] *Id.* Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 includes or discloses subject matter that satisfies limitation [B].

d) *[C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and*

Respondents argue:

To the extent Broadcom's successfully argues that the processors in Sigma's Accused Products perform "selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier," then Sigma's EM8550/Quasar Chip anticipates or renders obvious the '059 Patent for the same reasons. RX-0383C at Q440. [

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]. RX-0668C at
Q67; Tr. (Ignaszewski) at 454:19-455:18, 488:14-490:4.

Resps. Br. at 179-80.

Broadcom argues:

Additionally, because Respondents have not shown that “Quasar Chip” discloses at least these limitations, Respondents have failed to establish that “Quasar Chip” discloses [

.].” CX-0579C
(Acton WS) at Q/A 360-373.

Broadcom Br. at 288.

Respondents have not shown, through clear and convincing evidence, that the EM8550 selects a decoding process based on the identifier, as limitation [C] requires. In particular, respondents (and Dr. Stevenson) have not shown how the EM8550 selects a decoding process. *See* CX-0579C (Acton RWS) at Q/A 370-71. Mr. Ignaszewski’s testimony on this point, RX-0668C (Ignaszewski WS) at Q/A 67, is uncorroborated insofar as how the EM8550 performs an activity correspond to “selecting on said chip.” Accordingly, the administrative law judge has

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determined that respondents have not shown, through clear and convincing evidence, that the EM8550 includes or discloses subject matter that satisfies limitation [C].

- e) *[D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.*

Respondents argue:

To the extent Broadcom successfully argues that the processors in Sigma's accused SX6 perform "decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process," then Sigma's EM8550 Quasar chip anticipates or renders obvious the '059 Patent for the same reasons. RX-0383C at Q441. This is because the EM8550 video decoder engine [

1.

Resps. Br. at 180-81.

Broadcom argues:

Additionally, because Respondents have not shown that "Quasar Chip" discloses at least these limitations, Respondents have failed to establish that "Quasar Chip" discloses [

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].” CX-0579C

(Acton WS) at Q/A 360-373.

Broadcom Br. at 288.

The administrative law judge has determined that respondents have not shown that the EM8550 decodes packetized data utilizing “said selected decoding process” because it does not satisfy limitation [C]. *See* CX-0579C (Acton RWS) at Q/A 373. Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 includes or discloses subject matter that satisfies limitation [D].

2. Claim 12

Respondents’ entire argument is:

The EM8550 Quasar chip meets claim 12 for the same reasons as claim 11. RX-0383C at Q442; Tr. (Ignaszewski) at 488-490. Additionally, the [

1.
Broadcom’s contention fails in view of the foregoing testimony.

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Resps. Br. at 181-82.

Broadcom's entire argument for claims 12-20 follows:

Respondents have not shown that claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that claim 11 is anticipated or rendered obvious by Respondents' asserted prior art. [CX-0579C (Acton WS)] at Q/A 376-401. Additionally, Respondents have not established for dependent claims 15, 16, 18, and/or 20 that it would be obvious to combine the "Quasar Chip" with any of the H.264 Standard, VC-1, and/or MPEG-2 Video. *Id.* at Q/A 387, 389, 395, 401.

Broadcom Br. at 288.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 includes [

] was used in the EM8550. *See* CX-0579C (Acton RWS) at Q/A 377.

Accordingly, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 12.

3. Claim 13

Respondents argue:

The EM8550 Quasar chip meets claim 13 for the same reasons as claims 11 and 12. RX-0383C at Q443. Additionally, [

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].

Resps. Br. at 182.

The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 13 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 381. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 13.

4. Claim 14

Respondents' entire argument is:

The EM8550 Quasar chip meets claim 14 for the same reasons as claims 11-13. RX-0383C at Q444.

Resps. Br. at 182.

The administrative law judge previously determined that the EM8550 does not anticipate claims 11-13. The administrative law judge finds that the EM8550 does not anticipate claim 14 based upon the same evidence and analysis relied upon in discussing claims 11-13. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 383. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 14.

5. Claim 15

Respondents argue:

The EM8550 Quasar chip meets claim 15 for the same reasons as claim 11. RX-0383C at Q445. [

]. *Id.*

Resps. Br. at 182-83.

The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 15 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 387. In addition, Dr. Stevenson has not explicitly identified where, when, or how the EM8550 (including the supporting documents) decodes according to

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the H.264 standard. *See generally* RX-0383C (Stevenson WS) at 445-50. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 15.

6. Claim 16

Respondents argue:

The EM8550 Quasar chip meets claim 16 for the same reasons as claims 11 and 15. RX-0383C at Q451. To the extent the EM8550 Quasar chip does not expressly disclose VC-1 video decoding, it would have obvious to modify the EM8550 for an after-arising standard in the same way that the subsequent versions of the earlier Quasar chips were actually modified to add new standards. *Id.*; *see* RX-0678.

Resps. Br. at 183. Respondents then discuss modifications and supplementing the Quasar Chip. *Id.* at 184.

The administrative law judge previously determined that the EM8550 does not anticipate claims 11 and 15. The administrative law judge finds that the EM8550 does not anticipate claim 16 based upon the same evidence and analysis relied upon in discussing claims 11 and 15. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 388-89. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 16.

7. Claim 17

Respondents' anticipation argument follows:

The EM8550 Quasar chip meets claim 17 for the same reasons as claim 11. RX-383C at Q452. RX-0325C discloses that the
[

]. *Id.*

Resps. Br. at 185.

The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 17 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 390-91. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 17.

8. Claim 18

Respondents' anticipation argument follows:

The EM8550 Quasar chip meets claim 18 for the same reasons as claim 11. RX-383C at Q453. Specifically, RX-0326C discloses that the EM8300 Quasar Chip's [

].

Resps. Br. at 185-86.

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The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 18 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 392-93. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 18.

9. Claim 19

Respondents argue:

The EM8550 Quasar chip meets claim 19 for the same reasons as claim 11. RX-383C at Q/A 459. This is because the EM8550 Quasar chip alone or in combination with the knowledge of one of ordinary skill at the time of the invention anticipates and/or renders obvious this limitation. *Id.* Claim 19 requires code for generating a decoded video stream utilizing at least a portion of the decoded packetized data. *Id.* As discussed above, the EM8550 Quasar chip discloses [

]. *Id.*

Resps. Br. at 186.

The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 19 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 396-97. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 19.

10. Claim 20

Respondents' anticipation argument follows:

The EM8550 Quasar chip meets claim 20 for the same reasons as claims 11 and 19. RX-383C at Q460. For example, RX-0329C

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discloses that the EM8550 Quasar chip [

] RX-383C at Q460; RX-0329C.00049.

Resps. Br. at 186-87.

The administrative law judge previously determined that the EM8550 does not anticipate claim 11. The administrative law judge finds that the EM8550 does not anticipate claim 20 based upon the same evidence and analysis relied upon in discussing claim 11. *See, e.g.*, CX-0579C (Acton RWS) at Q/A 398-99. Accordingly, the administrative law judge determines that respondents have not shown, through clear and convincing evidence, that the EM8550 anticipates claim 20.

I. Obviousness – Kovacevic Alone

In addition to anticipation, respondents further argue that “Kovacevic also renders obvious claims 11-20.” Resps. Br. at 146-47. However, respondents do not present a distinct obviousness argument based on Kovacevic alone (*see* Resps. Br. at 147-64); rather, respondents blend their obviousness argument with their anticipation argument, which is addressed above. *See* § VI(G), *supra*.

1. Claim 11

- a) *[preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:*

Respondents’ obviousness argument follows:

Alternatively, it would have also been obvious to one of ordinary skill that a computer-readable storage would store microcode, and

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the microcode would have a code section for processing an encoded video stream according to the methods described by Kovacevic. RX-0383C.0082 (Stevenson) Q332.

Resps. Br. at 148. Dr. Stevenson's testimony follows:

Q332. Let's discuss the individual limitations of claims 11-20 of the '059 patent in comparison to the Kovacevic reference. Let's start with claim 11. Does Kovacevic disclose the limitation "a computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising"?

A332. Yes. Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Kovacevic discloses that the multimedia processing system makes use of a microcode engine, which includes a micro-programmable sequencer or microprocessor for processing the stream. [RX-0337 (Kovacevic) at ¶ 0029]. The stored microcode includes commands for the microprocessor, which is used to process received data packets. [See RX-0337 (Kovacevic) at ¶ 0029]. Kovacevic also discloses a MIPS core, which can be a RISC processor. [See RX-0337 (Kovacevic) at ¶ 0032]. The MIPS core is also used to process received data packets. [See RX-0337 (Kovacevic) at ¶ 0032]. It would have been obvious to a POSITA that computer code would be stored in computer readable memory.

RX-0383C (Stevenson WS) at Q/A 332.

Neither Broadcom nor its expert, Dr. Acton, clearly rebuts this argument. *See generally* Broadcom Br. at 274-76 (contesting limitations [B], [C], and [D]); Broadcom Reply, Section III(D) (contesting limitation [B]); CX-0579C (Acton RWS) at Q/A 230-42 (Dr. Acton does not offer any opinions concerning the preamble).

The administrative law judge has determined that respondents have shown, through clear and convincing evidence, that a person of ordinary skill in the art would have understood that storing the code recited in the preamble in a separate memory or storage was an obvious variant of storing in an alternative location. *See* RX-0383C (Stevenson WS) at Q/A 332. Indeed, there

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is no substantive dispute that Kovacevic implements code that resides in memory, that memory is needed for the system to operate, or that one of ordinary skill (*e.g.*, an engineer with a master's degree and two to three years of experience in the development and programming relating to video digital signal processing) would have grasped this. *Id.* Likewise, a person of ordinary skill in the art would have understood that the memory can be separate from the chip used to perform the steps recited in the claim. Accordingly, the administrative law judge finds that the preamble would have been obvious in light of Kovacevic.

b) *[A] receiving on a chip, packetized data within the encoded video stream;*

The administrative law judge previously determined that Kovacevic discloses subject matter that satisfies this limitation. *See* § VI(G)(1)(b), *supra*.

c) *[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;*

Respondents' brief argues that Kovacevic discloses this limitation. *See* Resps. Br. at 149-50. Respondents' brief does not argue that this limitation would have been obvious in light of Kovacevic, even though Dr. Stevenson provided testimony on this point. *Id.*; RX-0383C (Stevenson WS) at Q/A 337 ("Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation.").

The administrative law judge previously determined that Kovacevic does not disclose subject matter that satisfies this limitation. *See* § VI(G)(1)(c), *supra*. Further, Dr. Stevenson's testimony does not sufficiently explain why this limitation would have been obvious in light of "Kovacevic alone." Accordingly, the administrative law judge has determined that this limitation would not have been obvious in light of Kovacevic alone.

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d) [C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and

Respondents' brief argues that Kovacevic discloses this limitation. *See* Resps. Br. at 150-55. Respondents' brief does not argue that this limitation would have been obvious in light of Kovacevic, even though Dr. Stevenson provided testimony on this point. *Id.*; RX-0383C (Stevenson WS) at Q/A 340 ("Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation.").

The administrative law judge previously determined that Kovacevic does not disclose subject matter that satisfies this limitation. *See* § VI(G)(1)(d), *supra*. Further, Dr. Stevenson's testimony does not sufficiently explain why this limitation would have been obvious in light of "Kovacevic alone." Accordingly, the administrative law judge has determined that this limitation would not have been obvious in light of Kovacevic alone.

e) [D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.

Respondents' brief argues that Kovacevic discloses this limitation. *See* Resps. Br. at 155. Respondents' brief does not argue that this limitation would have been obvious in light of Kovacevic, even though Dr. Stevenson provided testimony on this point. *Id.*; RX-0383C (Stevenson WS) at Q/A 347 ("Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation.").

The administrative law judge previously determined that Kovacevic does not disclose subject matter that satisfies this limitation. *See* § VI(G)(1)(e), *supra*. Further, Dr. Stevenson's testimony does not sufficiently explain why this limitation would have been obvious in light of "Kovacevic alone." Accordingly, the administrative law judge has determined that this limitation would not have been obvious in light of Kovacevic alone.

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2. Claims 12 and 19

Respondents' brief argues that Kovacevic discloses subject matter claimed in claims 12 and 19. *See* Resps. Br. at 155, 164. Respondents' brief does not argue that this limitation would have been obvious in light of Kovacevic alone, even though Dr. Stevenson provided testimony on this point. *Id.*; RX-0383C (Stevenson WS) at Q/A 349, 376 ("**Kovacevic alone** or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation." (emphasis added)).

The administrative law judge previously determined that Kovacevic does not disclose subject matter that satisfies claims 12 and 19. *See* § VI(G)(2) and VI(G)(8), *supra*. Further, Dr. Stevenson's testimony does not sufficiently explain why this limitation would have been obvious in light of "Kovacevic alone." Accordingly, the administrative law judge has determined that claims 12 and 19 would not have been obvious in light of Kovacevic alone.

3. Claims 13-18

Respondents' brief contains numerous ambiguous assertions of invalidity that involve Kovacevic. For example, respondents argue:

- Based on the knowledge of one ordinary skill at the time of the '059 Patent, Kovacevic and/or Kovacevic-Chu anticipate and/or render obvious claim 13.
- Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 14 obvious.
- To the extent Kovacevic and/or Kovacevic-Chu do not anticipate and/or render obvious this limitation one of ordinary skill would have been motivated to modify those grounds to incorporate the disclosures of H.264 to render claim 15 obvious.
- Based on the knowledge of one ordinary skill at the time of the '059 Patent, Kovacevic and/or Kovacevic-Chu renders claim 16 obvious.
- Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 17 obvious.
- Kovacevic and/or Kovacevic-Chu with MPEG-2 Video renders claim 18 obvious.

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See Resps. Br, Section (E)(2)(b).

Nevertheless, as with claims 11, 12, and 19, Dr. Stevenson's testimony with respect to claims 13-18 does not sufficiently explain why this limitation would have been obvious in light of "Kovacevic alone." Accordingly, the administrative law judge has determined that claims 13-18 would not have been obvious in light of Kovacevic alone.

J. Obviousness – Kovacevic in view of Chu

The Joint Outline identifies "Kovacevic in view of Chu (claims 11-17 and 19)" as a validity issue to be determined. Joint Outline at 7.⁶²

"Chu" is U.S. Patent No. 7,167,108 (RX-0268). Respondents argue:

U.S. Patent No. 7,167,108 ("Chu") qualifies as prior art under 35 U.S.C. §§ 102(a) and (e) because it was filed as a PCT application on November 26, 2003, published on June 17, 2004, and issued on January 23, 2007. RX-0383C.0084-0085 (Stevenson) Q343; RX-0268 (Chu).

Id. at 144.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 274-79 (discussing Chu without disputing its prior-art status); Broadcom Reply, Section IV(D) (same).

Accordingly, the administrative law judge has determined that Chu is prior art under 35 U.S.C. § 102(a) and § 102(e).

1. Claim 11

Respondents argue that "Kovacevic in view of Chu" render limitations [C] and [D] obvious. Resps. Br. at 152, 155.

a) Limitation [C]

⁶² Respondents' brief, however, also presents arguments involving "Kovacevic-Chu" for claims 18 and 20. Resps. Br. at 163-64. The Initial Determination addresses claims 11-20.

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Respondents argue, in part:

To the extent Kovacevic does not anticipate limitation 11[c], however, Kovacevic in view of Chu renders this limitation obvious. RX-0383C.0084-0086 (Stevenson) Q340; RDX-0013.00032-00039; RX-0268 (Chu). As seen in Figure 3, Chu discloses an apparatus “for switching between a plurality of bit stream decoders, [where] each decoder [is] adapted to decode bit streams having a unique format.” RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 1:47-49. Chu describes that the disclosed “apparatus comprises one or more format detectors which gather information only from the bit stream,” such as “frame information, the packet header information, and [] code word values in a portion of a coded content of the bit stream” that are “unique to the bit stream format.” RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 1:47-49, 1:59-66. Chu further describes that the “format detector output feeds logic, which is responsive to the detector output to determine a particular appropriate decoder among the plurality of decoders,” and that the “particular decoder determined by the logic may be responsive to the formatted bit stream to decode the formatted bit stream.” RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 1:51-56, 6:28-31. An individual decoder may be selected on the basis of a start code, packet header, or code word contained within the bit stream. RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 2:62-3:40. The “detected start code, packet header, or code word is sent by path 324 to the logic 360, which may uniquely determine which decoder 340, 342, 344 [] is appropriate for the format detected,” and “[o]nce logic 360 has determined the appropriate decoder, switch 330 directs the formatted data stream on line 303 to the selected decoder 340, 342, or 344,” which “produces decoded data 350, 352, or 354, respectively.” RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 6:34-46. Chu describes that its method is “adaptable, even as standards proliferate and confusion among the various standards increases, because any truly unique, new standard must be detectable by at least one of the methods provided.” RX-0383C.0085 (Stevenson) Q344; *see* RX-0268 (Chu) at 2:11-15.

Dr. Stevenson testified that one of ordinary skill would be motivated to combine Chu with Kovacevic. RX-0383C (Stevenson) Q345. Similar to the system of Chu, the system of Kovacevic is for “identifying properties of the multimedia data” from information gathered from the bit stream. RX-0383C (Stevenson) Q345; *see* RX-0337 (Kovacevic) at 0011 and 0024. Thus, both systems are intended to identify the format of a digital

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video data stream from one of several formats (e.g., MPEG formats) based on information contained in the bitstream itself. And both systems include circuitry for determining that format and circuitry for routing the identified stream to an appropriate destination and/or decoder. RX-0383C (Stevenson) Q345. Given that both references disclose systems that perform analogous functions, for use in the same field, one of ordinary skill reading one reference would have been motivated to look to the other for further disclosures. RX-0383C (Stevenson) Q345. . . .

Resps. Br. at 152-53.

Broadcom argues:

Respondents have also not shown that combining Kovacevic with Chu for the “selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier” or “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process” limitations cures Kovacevic’s deficiencies. As Dr. Acton explained, Respondents failed to provide sufficient motivation to combine Chu and Kovacevic, and even if such motivation existed, Chu does not cure Kovacevic’s lack of using an identifier to determine the encoding standard. CX-0579C (Acton RWS) at Q/A 236.

Broadcom Br. at 276.

The administrative law judge finds that respondents have not shown that Chu discloses selecting a decoding process on a chip based on an identifier. *See* CX-0579C (Acton RWS) at Q/A 236. Dr. Stevenson does not rely on Chu to supplement Kovacevic’s deficiencies with respect to the claimed identifier (limitation [B]). *Id.* In other words, Dr. Stevenson has not shown that Chu includes an identifier. *Id.* Further, although Chu discloses selecting a decoding process, it is not clear that a person of ordinary skill would modify Kovacevic’s “next byte” in view of Chu, as Chu and Kovacevic have different principles of operation that are incompatible. *Id.* Further, Dr. Stevenson’s motivation-to-combine analysis, RX-0383C (Stevenson WS) at Q/A

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346, does not identify any deficiency in Kovacevic, or any need to modify Kovacevic.⁶³ *See Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013) (“[W]e cannot simply assume that ‘an ordinary artisan would be awakened to modify prior art in such a way as to lead to an obviousness rejection.’”). Accordingly, the administrative law judge has determined that respondents have not shown that limitation [C] would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

b) Limitation [D]

Respondents argue:

To the extent Kovacevic does not anticipate this limitation, however, Dr. Stevenson testified that it would also have been obvious to modify Kovacevic with Chu. RX-0383C.0087 (Stevenson) Q347-348. And one of ordinary skill would have been motivated to do so for the same reasons described for limitation 11[c], above. RX-0383C.0087 (Stevenson) Q347-348; *see* RX-0268 (Chu) at 1:47-49, 1:59-66; RX-0337 (Kovacevic) at ¶ 0065. Chu discloses decoding based on a selected decoding process. RX-0383C.0087 (Stevenson) Q347; *see* RX-0268 (Chu) at 6:34-46 (“**Decoder 340, 342, or 344, as selected, produces decoded data 350, 352, or 354, respectively.**”) (emphasis added). As discussed for limitation 11[c], the algorithm of Kovacevic could be implemented with the switching logic and decoders of Chu to select an MPEG-1 or MPEG-2 decoder according to whether an MPEG-1 or MPEG-2 elementary stream is identified by “next byte.”

Resps. Br. at 155.

⁶³ Dr. Stevenson opines, “Combining Kovacevic’s system with Chu would apply a known technique (*e.g.*, using information in the data stream to identify a stream format and inform logic to select a decoding process) to a known device (*e.g.*, Kovacevic’s multimedia system) to yield predictable results, based on known design considerations (*e.g.*, the need for flexible decoder functionality and the ability to decode video streams that are encoded using any one of many known or a priori unknown encoding standards).” RX-0383C (Stevenson WS) at Q/A 346. This, however, does not explain why a person of ordinary skill in the art would modify Kovacevic.

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The administrative law judge finds that limitation [D] would not have been obvious based on Kovacevic and Chu for the same reasons provided in relation to limitation [C]. *See* CX-0579C (Acton RWS) at Q/A 235-40.

2. Claim 12

Respondents argue “Kovacevic and/or Kovacevic-Chu disclose this limitation.” Resps. Br. at 155 (citing RX-0383C (Stevenson WS) at Q/A 349, 351-52).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 349, 351-52. Accordingly, the administrative law judge finds that respondents have failed to show claim 12 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

3. Claim 13

Respondents argue “Based on the knowledge of one ordinary skill at the time of the ‘059 Patent, Kovacevic and/or Kovacevic-Chu anticipate and/or render obvious claim 13.” Resps. Br. at 156 (citing RX-0383C (Stevenson WS) at Q/A 353).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 353. Accordingly, the administrative law judge finds that respondents have failed to show claim 13 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

4. Claim 14

Respondents argue “Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 14 obvious.” Resps. Br. at 156-57 (citing RX-0383C (Stevenson WS) at Q/A 354, 358).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 354, 358. Accordingly, the administrative law judge finds that respondents have failed to

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show claim 14 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

5. Claim 15

Respondents argue “To the extent Kovacevic and/or Kovacevic-Chu do not anticipate and/or render obvious this limitation one of ordinary skill would have been motivated to modify those grounds to incorporate the disclosures of H.264 to render claim 15 obvious.” Resps. Br. at 158 (citing RX-0383C (Stevenson WS) at Q/A 359, 363).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 359, 363. Accordingly, the administrative law judge finds that respondents have failed to show claim 15 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

6. Claim 16

Respondents argue “Based on the knowledge of one ordinary skill at the time of the ‘059 Patent, Kovacevic and/or Kovacevic-Chu renders claim 16 obvious.” Resps. Br. at 160 (citing RX-0383C (Stevenson WS) at Q/A 364, 366).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 364, 366. Accordingly, the administrative law judge finds that respondents have failed to show claim 16 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

7. Claim 17

Respondents argue “Kovacevic and/or Kovacevic-Chu anticipate and/or render claim 17 obvious.” Resps. Br. at 162 (citing RX-0383C (Stevenson WS) at Q/A 370, 374).

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The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 370, 374. Accordingly, the administrative law judge finds that respondents have failed to show claim 17 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

8. Claim 18

Respondents argue “Kovacevic and/or Kovacevic-Chu with MPEG-2 Video renders claim 18 obvious.” Resps. Br. at 163 (citing RX-0383C (Stevenson WS) at Q/A 375).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 375. Accordingly, the administrative law judge finds that respondents have failed to show claim 18 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

9. Claim 19

Respondents argue “Kovacevic and/or Kovacevic-Chu disclose claim 19.” Resps. Br. at 164 (citing RX-0383C (Stevenson WS) at Q/A 376).

Dr. Stevenson testified as follows:

Q376. Does the Kovacevic reference disclose claim 19?

A376. Yes. Kovacevic alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Claim 19 requires code for generating a decoded video stream utilizing at least a portion of the decoded packetized data. As discussed above, Kovacevic discloses a system that can process multiplexed data streams for display on a display device. [See RX-0337 (Kovacevic) at ¶ 0025]. While Kovacevic’s parsing and selecting of a decoder disclose claim 19, Kovacevic may alternatively be modified according to Chu to generate a decoded video stream utilizing at least a portion of decoded packetized data. Chu discloses generation of a decoded stream, as discussed above with respect to claim 11. A POSITA would be motivated to combine Kovacevic and Chu for the same reasons also discussed with respect to claim 11.

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RX-0383C (Stevenson WS) at Q/A 376.

The administrative law judge previously determined that claim 11 would not have been obvious based on Kovacevic and Chu, because at best it relies on Chu's alleged generation of a decoded stream as argued in connection with claim 11. Dr. Stevenson's testimony at Q/A 376 is conclusory and does not further inform the analysis. Accordingly, the administrative law judge finds that respondents have failed to show claim 19 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

10. Claim 20

Respondents argue "Kovacevic and/or Kovacevic-Chu with H.264 renders claim 20 obvious." Resps. Br. at 164 (citing RX-0383C (Stevenson WS) at Q/A 377).

The cited testimony, however, does not address Chu. *See* RX-0383C (Stevenson WS) at Q/A 377. Accordingly, the administrative law judge finds that respondents have failed to show claim 20 would have been obvious based upon the disclosures and teachings of Kovacevic and Chu.

K. Obviousness – Kovacevic (or Kovacevic-Chu) in view of MPEG-2 References

1. Claim 14 – MPEG-2 Systems

For claim 14, respondents argue:

To the extent Kovacevic and/or Kovacevic-Chu do not anticipate and/or render obvious this limitation, one of ordinary skill would have been motivated to modify those invalidity grounds to incorporate the disclosures of the MPEG-2 Systems standard. RX-0383C.0089-0090 (Stevenson) Q354; RDX-0013.00077-00080; RX-0269 (MPEG-2 Systems). The combination with MPEG-2 Systems renders this claim obvious. RX-0383C.0089 (Stevenson) Q358. Kovacevic already discloses stuffing bytes associated with MPEG-2 data. RX-0383C.0089 (Stevenson) Q358; *see* RX-0337 (Kovacevic) at ¶ 0064. MPEG-2 Systems provides additional implementation details regarding the structure and removal of the stuffing bytes. RX-0383C.0089 (Stevenson)

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Q358. For example, MPEG-2 Systems describes multiple “stuffing byte[s]” that are “a fixed 8-bit value equal to ‘1111 1111’ that can be inserted by the encoder” and “discarded by the decoder.” RX-0383C.0089 (Stevenson) Q358; RX-0269.00049 (MPEG-2 Systems) at § 2.4.3.5; -00075 at § 2.5.3.4. It would have been obvious to modify Kovacevic’s stuffing byte processing according to the MPEG-2 Systems standard. RX-0383C.0089 (Stevenson) Q358. Indeed, Kovacevic specifically describes that standard. *Id.* Moreover, the stuffing byte of Kovacevic is named the same and performs the same function as the stuffing_byte of the MPEG-2 Systems standard. *Id.* In particular, one of ordinary skill would understand that the stuffing byte of Kovacevic is used to insert filler bits into the data stream to conform the data stream to a regular pattern, and such fill can be recognized and removed by the decoder. *Id.* Similarly, the stuffing byte of the MPEG-2 Systems standard is used for the same purpose. *Id.* It defines a specific byte (“1111 1111”) that can be inserted by the encoder and “discarded by the decoder.” RX-0269.00049 (MPEG-2 Systems) at § 2.4.3.5; -00075 at § 2.5.3.4. It would have been obvious to discard this byte by the decoder by matching it with a comparator and discarding bytes that match. RX-0383C.0089 (Stevenson) Q358. It would have also been obvious to one of ordinary skill to combine or supplement the descriptions of stuffing byte in Kovacevic with the disclosures of stuffing_byte in the MPEG-2 Systems standard. *Id.* Combining Kovacevic and/or Kovacevic-Chu with MPEG-2 Systems would apply a known technique (*e.g.*, using stuffing byte to harmonize data) to a known device (*e.g.*, Kovacevic multimedia system) to yield predictable results, based on known design considerations (*e.g.*, need for regular patterns of data). RX-0383C.0089-90 (Stevenson) Q358.

Resps. Br. at 158.⁶⁴

Broadcom argues:

Respondents have not shown that Kovacevic, alone or in combination with secondary references, discloses or renders obvious claim 14, which requires “code for removing said plurality of bytes from said received packetized data, if said plurality of bytes matches said determined byte sequence.” Dr. Acton testified

⁶⁴ Respondents argue that the MPEG-2 Systems standard (RX-0269, which is formally known as ISO/IEC 13818-1 or ITU-T H.222.0) “was published in December 2000” and is prior art under § 102(b). Broadcom does not clearly rebut this argument. Accordingly, the administrative law judge has determined that the MPEG-2 Systems standard is prior art under 35 U.S.C. § 102(b).

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Kovacevic does not disclose or render obvious claim 14 because Kovacevic discloses that stuffing data can be ignored, which is different from removing a plurality of bytes. CX-0579C (Acton WS) at Q/A 250.

Broadcom Br. at 276-77.

Having considered the parties' arguments, and assuming claims 11-13 would have been obvious, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that claim 14 also would have been obvious based on Kovacevic (or Kovacevic-Chu) in view of the MPEG-2 Systems (RX-0269). In particular, MPEG-2 Systems teaches that stuffing bytes can be "discarded by the decoder," which satisfies the requirements of claim 17. RX-0269 at 49, 75; RX-0383C (Stevenson WS) at Q/A 358. Further, Dr. Stevenson testified that a person of ordinary skill in the art would understand that the MPEG-2 Systems's teachings could be used in Kovacevic to harmonize data. *Id.* Dr. Acton's testimony, on the other hand, does not address Dr. Stevenson's "discarding" argument, nor does it fully explain the difference between ignoring and removing a plurality of bytes (in relation to claim 14). *See* CX-0579C (Acton RWS) at Q/A 250-52. Accordingly, assuming claims 11-13 would have been obvious, the administrative law judge finds that claim 14 also would have been obvious.

2. Claim 17 – MPEG-2 Video

Respondents argue:

Alternatively, one of ordinary skill would have also been motivated to modify Kovacevic and/or Kovacevic-Chu to incorporate the disclosures of the MPEG-2 Video standard, which were well known at the time of filing the '059 Patent, to render claim 17 obvious, because Kovacevic discloses the use of MPEG-2 video streams, and MPEG-2 Video provides additional details for decoding such streams, including FLC and VLC coding processes. RX-0383C (Stevenson) Q374. For example, Figure 7-1 discloses use of variable length decoding for MPEG-2 Video. *Id.*; *see* RX-0271.00074 (MPEG-2 Video) at Fig. 7-1; § 7.2. Similarly, Table B.12 describes the selection of variable length codes for

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DCT_DC_SIZE_LUMINANCE. RX-0383C (Stevenson) Q374; *see* RX-0271.00145 (MPEG-2 Video) at Table B.12. Combining Kovacevic's multimedia system with MPEG-2 Video decoding would apply a known technique (*e.g.*, MPEG-2 Video digital video decoding) to a known device (*e.g.*, Kovacevic's multimedia system) to yield predictable results, based on known design considerations (*e.g.*, the need of decoders to handle known video encoding standards). RX-0383C (Stevenson) Q374.

Resps. Br. at 162-63.⁶⁵

Broadcom argues:

Respondents have not shown that Kovacevic discloses or renders obvious claim 17, which requires "code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to one or more of H.261, H.263, H.263+, MPEG-1, MPEG-2 and/or MPEG-4 video encoding." Additionally, Respondents have not established by clear and convincing evidence that Kovacevic discloses using one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process, and/or a context adaptive binary arithmetic coding (CABAC) process for decoding at least a portion of the received packetized data because Kovacevic does not disclose decoding the packetized data. CX-0579C (Acton WS) at Q/A 261.

Broadcom Br. at 278-79.

Dr. Acton's testimony at Q/A 261 follows:

Q261. Please explain why you do not agree with Dr. Stevenson.

A. It is my opinion that Kovacevic, which is RX-0337, does not disclose claim 17 for the same reasons that I discussed with respect to claim 11. Additionally, as I explained, Kovacevic doesn't disclose using one or more of a fixed length coding (FLC) process or a variable length coding (VLC) process for decoding at least a portion of the received packetized data because, because as

⁶⁵ Respondents argue that the MPEG-2 Video standard (RX-0271, which is formally known as formally known as ISO/IEC 13818-2 and as ITU-T H.262) was "published in 1995" and is prior art under § 102(b). Broadcom does not clearly rebut this argument. Accordingly, the administrative law judge has determined that the MPEG-2 Video standard is prior art under 35 U.S.C. § 102(b).

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discussed above with respect to claim 11, Kovacevic does not disclose decoding any portion of the packetized data.

CX-0579C (Acton RWS) at Q/A 261.

Having considered the parties' arguments, and assuming claim 11 would have been obvious, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that claim 17 also would have been obvious based on Kovacevic (or Kovacevic-Chu) in view of the MPEG-2 Video standard (RX-0271). In particular, MPEG-2 Video teaches decoding using a FLC or VLC process according to a specific identifier, as claim 17 requires. RX-0271 at 74; RX-0383C (Stevenson WS) at Q/A 374. Further, Dr. Stevenson testified that a person of ordinary skill in the art would understand that the MPEG-2 Video's teachings could be used in Kovacevic to handle known video encoding standards. *Id.* Dr. Acton's testimony, on the other hand, does not substantively address MPEG-2 Video. *See* CX-0579C (Acton RWS) at Q/A 260-63. Accordingly, assuming claim 11 would have been obvious, the administrative law judge finds that claim 17 also would have been obvious.

3. Claim 18 – MPEG-2 Video

Respondents argue:

Kovacevic and/or Kovacevic-Chu with MPEG-2 Video renders claim 18 obvious. RX-0383C.0093 (Stevenson) Q375; RDX-0013.00124-00137. One of ordinary skill would have been motivated to combine Kovacevic and MPEG-2 Video to arrive at claim 18 for the same reasons as discussed with respect to Claim 17. RX-0383C.0093 (Stevenson) Q375. As discussed with respect to Claim 17, Kovacevic discloses the use and processing of MPEG-2 Video packets. RX-0383C.0093 (Stevenson) Q375. MPEG-2 Video discloses the use of prediction pixel information. RX-0383C.0093 (Stevenson) Q375. For example, MPEG-2 Video discloses that "Predictive Coded Pictures (P-Pictures) are ... generally used as a reference for further prediction." RX-0383C.0093 (Stevenson) Q375; *see* RX-0271.00008 (MPEG-2 Video) at Intro 4.1.1. Broadcom's expert also describes the motion compensation processes as standard video decoding processes.

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CX-0003C.0007 (Acton) Q21. Thus, the combination meets claim 18.

Resps. Br. at 163.

With respect to claim 18, Broadcom has argued:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579 (Acton WS) at Q/A 243-271.

Broadcom Br. at 279.

Having considered the parties' arguments, and assuming claim 11 would have been obvious, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that claim 18 also would have been obvious based on Kovacevic (or Kovacevic-Chu) in view of the MPEG-2 Video standard (RX-0271). In particular, MPEG-2 Video teaches data with prediction pixels and/or prediction error information, as claim 18 requires. RX-0271 at 8 (discussing P-Pictures); RX-0383C (Stevenson WS) at Q/A 375. Further, Dr. Stevenson testified that a person of ordinary skill in the art would understand that the MPEG-2 Video's teachings could be used in Kovacevic to handle known video encoding standards. *Id.* at Q/A 374-75. Dr. Acton's testimony, on the other hand, does not substantively address MPEG-2 Video. *See* CX-0579C (Acton RWS) at Q/A 264-65. Accordingly, assuming claim 11 would have been obvious, the administrative law judge finds that claim 18 also would have been obvious.

L. Obviousness – Kovacevic (or Kovacevic-Chu) in view of H.264

1. Claim 15

Respondents argue, in part:

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The combination with H.264 discloses claim 15. RX-0383C.0090 (Stevenson) Q363. The processing schemes required by claim 15—namely fixed length coding, variable length coding, and context adaptive binary arithmetic coding—are all used in the H.264 standard. RX-0383C.0090 (Stevenson) Q363. For example, in discussing video coding, H.264 discloses that “[t]he syntax element coeff_token is decoded using one of the five VLCs specified in the five right-most columns of table 9-5.” RX-0383C.0090 (Stevenson) Q363; *see* RX-0270.00177 (H.264) at § 9.2.1. “VLCs” in the disclosed text refers to variable length coding. RX-0383C.0090 (Stevenson) Q363. Similarly, section 9.3 of the H.264 standard discloses “CABAC parsing process for slice data.” RX-0383C.0090 (Stevenson) Q363; *see* RX-0270.00184 (H.264) at § 9.3. Moreover, the named inventor of the ‘059 Patent, Stephen Gordon, confirmed that all video encoding standards use variable and fixed length coding. RX-0670.0143-0145 (Gordon) at 140:21-142-11. Broadcom’s expert also describes the FLC and VLC processes as standard video decoding processes. CX-0003C.0007 (Acton) at Q22.

Resps.Br. at 159.⁶⁶

With respect to H.264, Broadcom argues:

Additionally, Respondents have not established by clear and convincing evidence that a POSA would be motivated to modify Kovacevic to process H.264 encoded video streams, or modify Kovacevic in view of the H.264 standard, because in paragraph [0066] Kovacevic explicitly states that it simply “exploit[s] similarities between MPEG-1 and MPEG-2 data to process both MPEG-1 and MPEG-2 data using a single methodology.” CX-0579C (Acton WS) at Q/A 257.

Broadcom Br. at 277.

Having considered the parties’ arguments, and assuming claim 11 would have been obvious, the administrative law judge has determined that respondents have shown, through clear

⁶⁶ Respondents argue that the H.264 standard (RX-0270, which is also known as MPEG-4 Part 10 and Advanced Video Coding, (“H.264”)) was “published in 2003” and is prior art “under 35 U.S.C. §§ 102(a) and (b).” Respondents note that the ‘059 Patent’s background admits that H.264 is prior art.” Broadcom does not clearly rebut this argument. Accordingly, the administrative law judge has determined that the H.264 standard is prior art under 35 U.S.C. § 102(a) and § 102(b).

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and convincing evidence, that claim 15 also would have been obvious based on Kovacevic (or Kovacevic-Chu) in view of the H.264 standard (RX-0270). In particular, the processing schemes described in claim 15 are all used in the H.264 standard. RX-0383C (Stevenson WS) at Q/A 363. Modifying Kovacevic's multimedia system to incorporate the decoding scheme of H.264 is an example of applying a known technique, to a known device, to yield predictable results. *Id.* Dr. Acton's testimony relies on an overly stringent in its view of why a person of ordinary skill in the art would not be able to apply a familiar item, such as Kovacevic, beyond its primary purpose. *KSR*, 550 U.S. at 420 ("Common sense teaches, however, that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle."). Accordingly, assuming claim 11 would have been obvious, the administrative law judge finds that claim 15 also would have been obvious.

2. Claim 20

Respondents argue:

Kovacevic and/or Kovacevic-Chu with H.264 renders claim 20 obvious. RX-0383C.0094 (Stevenson) Q377; RDX-0013.00148-00161. One of ordinary skill would have been motivated to combine Kovacevic and/or Kovacevic-Chu with H.264 for the same reasons discussed for Claim 14. RX-0383C.0094 (Stevenson) Q377. Further, H.264 discloses a deblocking filter process. RX-0383C.0094 (Stevenson) Q377; see RX-0270.00163 (H.264) at § 8.7 Deblocking Filter Process. Thus, this combination satisfies Claim 20.

Resps. Br. at 164.

Broadcom argues:

Respondents have not shown that Kovacevic, or Kovacevic in view of Chu and the H.264 standard, renders obvious claim 20, which requires "code for filtering said generated decoded video stream utilizing one or both of an overlapped transform process and/or a

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deblocking process.” Additionally, as discussed above Kovacevic explicitly states at paragraph [0066] that it is directed to “exploiting similarities between MPEG-1 and MPEG-2 data.” Respondents have not shown by clear and convincing evidence that a POSA would have been motivated to modify Kovacevic, or Kovacevic in view of Chu, to process H.264 encoded video streams. CX-0579C (Acton WS) at Q/A 271.

Broadcom Br. at 279.

Dr. Acton testified as follows:

Q271. Please explain why you do not agree with Dr. Stevenson.

A It is my opinion that Kovacevic, which is RX-0337, in view of the H.264 standard, which is RX-0270, does not render obvious claim 20 because claim 20 depends from claim 11, which, as I previously discussed, is not anticipated and/or rendered obvious by Kovacevic. Additionally, as I explained with respect to claim 14, Kovacevic explicitly states at paragraph [0066] that it is specifically directed to “exploiting similarities between MPEG-1 and MPEG-2 data to process both MPEG-1 and MPEG-2 data using a single methodology.” Thus, POSA would not be motivated to modify Kovacevic to process H.264 encoded video streams.

CX-0579C (Acton RWS) at Q/A 271.

Having considered the parties’ arguments, and assuming claims 11 and 19 would have been obvious, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that claim 20 also would have been obvious based on Kovacevic (or Kovacevic-Chu) in view of the H.264 standard (RX-0270). In particular, the H.264 standard discloses a deblocking filter process. RX-0270 at 163; RX-0383C (Stevenson WS) at Q/A 377. Further, a person of ordinary skill in the art would have been able, and motivated, to use the teachings from H.264 in connection with Kovacevic. *Id.* Dr. Acton’s testimony relies on an overly stringent in its view of why a person of ordinary skill in the art would not be able to apply a familiar item, such as Kovacevic, beyond its primary purpose. *KSR*, 550 U.S. at 420 (“Common sense teaches, however, that familiar items may have obvious uses beyond their

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primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.”). Accordingly, assuming claims 11 and 19 would have been obvious, the administrative law judge finds that claim 20 also would have been obvious.

M. Obviousness – Wise in view of Kovacevic (claims 11-19)

Respondents argue that U.S. Patent Publication No. US 2003/0156652 (“Wise”) (RX-0339) “in view of Kovacevic renders obvious claims 11-19 of the ‘059 Patent under any proposed construction.” Resps. Br. at 164.

Respondents argue that:

U.S. Patent Publication No. US 2003/0156652 (“Wise”) was filed on October 10, 2001, and published on August 21, 2003. RX-0383C at Q378-379; RX-0339. Thus, Wise qualifies as prior art to the ‘059 Patent under 35 U.S.C. §§ 102(a), (b), (e), and 103(a).

Id. at 146.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 279-83 (discussing Wise without disputing its prior-art status); Broadcom Reply, Section IV(D) (same).

Accordingly, the administrative law judge has determined that Wise is prior art under 35 U.S.C. § 102(a), §102(b), and § 102(e).

1. Claim 11

- a) [preamble] A computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section being executable by a machine to perform steps comprising:*

Respondents argue:

Wise discloses a “a computer-readable storage having stored thereon, a computer program having at least one code section for processing an encoded video stream, the at least one code section

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being executable by a machine to perform steps comprising.” RX-0383C (Stevenson) Q385; RDX-0014.1-2 (Wise Chart). Broadcom does not dispute that this limitation is met under any proposed construction. *See* CPreHg. Br. at 371-378.

Respondents’ Construction: Regarding Respondents’ proposed construction for “computer readable storage”—*i.e.*, “transitory and nontransitory computer-readable storage”—Wise discloses a video decoder system including ROM, which is “computer-readable storage,” that stores programs for decoding different video encoding standards, which amount to “at least one code section for processing an encoded video stream.” RX-0383C (Stevenson) Q385; RDX-0014.1-2 (Wise Chart); RX-0339 (Wise) at ¶ [3352]. Further, Wise’s invention decodes “a plurality of differently encoded input signals” such as “well known standards known as JPEG, MPEG and H.251.” RX-0383C (Stevenson) Q385; RX-0339 (Wise) at ¶ [0002].

Complainant’s Construction: Likewise, Wise satisfies Complaint’s construction—plain and ordinary meaning. RX-0383C (Stevenson) Q385; RDX-0014.1-2 (Wise Chart).

Resps. Br. at 165.

Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 280-81 (contesting limitations [B], [C], and [D]); Broadcom Reply, Section III(D) (contesting limitation [B]).

Paragraph 3352 of Wise follows:

[3352] The present invention also relates to an improved pipeline system having a spatial decoder system for video data including a Huffman decoder, an index to data and an arithmetic logic unit, and a microcode ROM having separate stored programs for each of a plurality of different picture compression/decompression standards, such programs being selectable by a token, whereby processing for a plurality of different picture standards is facilitated. . . .

RX-0339, ¶ 3352.

The administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Wise discloses a computer-readable storage, *i.e.*, the ROM, that

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stores code for processing an encoded video stream, as the preamble requires. *See* RX-0383C (Stevenson WS) at Q/A 385; RX-0339, ¶¶ 2, 3352. Further, Dr. Acton does not provide any rebuttal with respect to the preamble. *See* CX-0579C (Acton RWS) at Q/A 272-84 (Dr. Acton does not offer any opinions concerning the preamble). Accordingly, the administrative law judge finds that Wise discloses subject matter that satisfies the preamble.

b) *[A] receiving on a chip, packetized data within the encoded video stream;*

Respondents argue:

Wise discloses “receiving on a chip, packetized data within the encoded video stream.” RX-0383C (Stevenson) Q386; RDX-0014.2-7 (Wise Chart). Wise’s system includes a spatial decoder chip, in which “the data arrives through the Start Code Detector.” RX-0383C (Stevenson) Q386; RDX-0014.4-5 (Wise Chart); RX-0339 (Wise) at ¶ [0368], Figs. 11, 58. The Start Code Detector “may be positioned as the first processing stage in the pipeline” and receive input data streams in bytes. RX-0383C (Stevenson) Q386; RDX-0014.4-5 (Wise Chart); RX-0339 (Wise) at ¶¶ [0052], [1581]-[1584], [1592].

Respondents’ Construction: Regarding Respondents’ proposed construction—“a packetized elementary video stream”—Wise discloses “a pipeline system having an input data stream, and a processing stage for receiving the input data stream,” which is shown in Fig. 58 as an “coded video data.” RX-0383C (Stevenson) Q386; RX-0339 (Wise) at ¶ [0067], Fig. 11; RDX-0383.5-6 (Stevenson Demonstratives). In describing the type of stream Wise handles, it states, “[the] video decoder and decompression system handles a plurality of separately encoded bit streams arranged as a single serial bit stream of digital bits.” RX-0383C (Stevenson) Q386; RX-0339 (Wise) at Abstract. Because Wise does not have to demultiplex its encoded bit stream of video data to access the start code, one of ordinary skill would understand it to operate on a packetized elementary video stream.

Complainant’s Construction: For these same reasons, the Wise also satisfies Complaint’s construction—plain and ordinary meaning. RX-0383C (Stevenson) Q386.

Resps. Br. at 165-66.

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Broadcom does not clearly rebut this argument. *See generally* Broadcom Br. at 280-81 (contesting limitations [B], [C], and [D]); Broadcom Reply, Section III(D) (contesting limitation [B]).

The evidence and argument cited in respondents' brief shows that Wise's spatial decoder system includes a chip that receives packetized data within an encoded video stream, as limitation [A] requires. *See, e.g.,* RX-0383C (Stevenson WS) at Q/A 386. Accordingly, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that Wise discloses subject matter that satisfies this limitation.

- c) ***[B] determining on said chip, an identifier within said received packetized data that defines one of a plurality of encoding types associated with packets in the encoded video stream;***

Respondents argue, in part:

... While Wise's start code detector "detect[s] MPEG start-codes, H.261 start-codes, and JPEG marker codes," one of ordinary skill would find it obvious to use a different identifier within the video stream, such as the "next byte" indication of a video encoding types in Kovacevic, which is distinct from a start code and within received packetized data. RX-0383C (Stevenson) Q388; RX-0339 (Wise) at ¶ [0448]; Tr. (Stevenson) at 723:3-724:23. As discussed previously in Section V.E.2.b.ii at page 149 (Limitation 11[b]), Kovacevic describes how other bytes are used as an identifier, such as its "next byte" after the start code. RX-0383C (Stevenson) Q388; RX-0337 (Kovacevic) at ¶¶ [0064]-[0065]. Thus, one of ordinary skill would modify the start code detector of Wise to look past the start code of the packetized elementary video stream—satisfying Respondents' construction for "packetized data within the encoded video stream"—and generate tokens for the encoding type based on the "next byte" of Kovacevic. RX-0383C (Stevenson) Q388-390.

One of ordinary skill would have been motivated to use Kovacevic's "next byte" identifier in Wise's system to comply with common standards and increase robustness of the system's stream identification. RX-0383C (Stevenson) Q391. Combining the two would be a simple and predictable change to the code detector of Wise. RX-0383C (Stevenson) Q391. For example,

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Kovacevic discloses determining a video encoding type identifier distinct from a start code within packetized data that defines one of multiple encoding types of packets in the encoded video stream. RX-0383C (Stevenson) Q391; RX-0337 (Kovacevic) at ¶¶ [0061]-[0065].

Resps. Br. at 166-67.

Broadcom argues, in part, that “Respondents have not shown by clear and convincing evidence that Wise, alone or in view of Kovacevic, discloses or renders obvious at least claim 11’s recited “identifier,” regardless of which of the proposed claim constructions are adopted.” Broadcom Br. at 280.

The administrative law judge previously determined that Kovacevic does not disclose subject matter that satisfies this limitation. *See* § VI(G)(1)(c), *supra*.

While respondents’ brief contends that Wise discloses this limitation, their expert relies on a combination of Wise and Kovacevic in concluding that the limitation is disclosed. *See* RX-0383C (Stevenson WS) at Q/A 387 (Dr. Stevenson does not cite to any portion of Wise in his answer). In the subsequent Q/A, Dr. Stevenson proposes a combining Wise and Kovacevic in the very first sentence:

Q388. How does Wise in view of Kovacevic render limitation 11[b] obvious?

A388. While Wise states at RX-0339 at ¶ [0448] that it uses a “start code detector” to “detect MPEG start-codes, H.261 start-codes, and JPEG marker codes,” one would find it obvious to use a different identifier within the video stream, such as the “next byte” indication of a video encoding types in Kovacevic, which is distinct from a start code and within received packetized data. For example, RX-0337 at ¶¶ [0064]-[0065] describes how other bytes are used as an identifier, such as its “next byte” after the start code. Specifically, it states, “In step 760, it is determined if a next byte has a value equal to a hexadecimal 0xFF. If the next byte does not have a value equal to a hexadecimal value of 0xFF, it is determined the received packet is associated with MPEG-2 data ... Returning to step 760, if it is determined the next byte has a value

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equal to hexadecimal value of 0xFF, it is determined the received packet is associated with MPEG-1 data.” (RX-0337 at ¶¶ [0064]-[0065].) Therefore, a POSITA could modify the start code detector of Wise to look past the start code and generate tokens indicating the encoding type based on the “next byte” of Kovacevic.

RX-0383C (Stevenson WS) at Q/A 388.⁶⁷

The administrative law judge has also determined that Wise does not disclose using an identifier. As Dr. Stevenson’s testimony shows, Wise discloses a start code, not an identifier. *See id.*; *see also* CX-0579C (Acton RWS) at Q/A 276. Thus, neither Wise nor Kovacevic disclose a start code.

Further, the administrative law judge finds that respondents have not shown, through clear and convincing evidence, that a person of ordinary skill would modify Wise in the manner suggested. *See* CX-0579C (Acton RWS) at Q/A 276. As Dr. Acton testified, Kovacevic uses “next byte” to distinguish between MPEG-1 and MPEG-2, and Wise already distinguished between these two standards by using start codes. *Id.*

Accordingly, the administrative law judge has determined that Wise, in view of Kovacevic, does not disclose this limitation.

d) *[C] selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier; and*

Respondents argue:

⁶⁷ Wise, at ¶ 448, states: “The system of the present invention also provides a combination of the standard-independent indices generation circuits, which are strategically placed throughout the system in combination with the token decode circuits. For example, the system is employed for specifically decoding either the H.261 video standard, or the MPEG video standard or the JPEG video standard. These three compression coding standards specify similar processes to be done on the arriving data, but the structure of the datastreams is different. As previously discussed, it is one of the functions of the Start Code Detector to detect MPEG start-codes, H.261 start-codes, and JPEG marker codes, and convert them all into a form, *i.e.*, a control token which includes a token stream embodying the current coding standard. . . .” RX-0339 (Wise), ¶ 448.

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Limitation 11[c]: The Wise-Kovacevic combination teaches “selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier.” RX-0383C (Stevenson) Q393; RDX-0014.21-34 (Wise Chart); RDX-0383.8 (Stevenson Demonstratives). As noted for limitation 11[b], the combined disclosures of Wise and Kovacevic render obvious the claimed “identifier” under any proposed construction. RX-0383C (Stevenson) Q393. And, while Wise states that it uses a “start code detector” to “detect MPEG start-codes, H.261 start-codes, and JPEG marker codes” (RX-0339 at ¶ [0448]), one of ordinary skill would find it obvious to use a different identifier within the video stream, such as using the “next byte” as described in Kovacevic. RX-0383C (Stevenson) Q393. Therefore, one of ordinary skill would use the identifier of Kovacevic to generate tokens describing the encoding type as described in Wise. RX-0383C (Stevenson) Q393. The modified Wise-Kovacevic “CODING_STANDARD tokens” would be passed through the pipeline processor, decoded in the relevant state machines, and passed through other, non-relevant state machines. RX-0383C (Stevenson) Q393; RX-0339 (Wise) at ¶¶ [0448], [0057], [0384]-[0385]. Wise performs “selecting” using CODING_STANDARD tokens, namely the Huffman decoder and parser use that token “to select tables needed for a particular identified coding standard.” RX-0383C (Stevenson) Q393; RX-0339 (Wise) at ¶¶ [0059]-[0060], [0374], [0375].

Resps. Br. at 167-68.

Broadcom argues:

Respondents have not shown that Wise in view of Kovacevic discloses “selecting on said chip, a decoding process from a plurality of decoding processes based on said determined identifier,” or “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process” because the alleged Wise-Kovacevic system does not disclose using an identifier to determine an encoding type associated with the packets in the encoded video stream CX-0579C (Acton WS) at Q/A 279-82.

Resps. Br. at 281.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown that “Wise-Kovacevic” discloses selecting a decoding process

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based on an identifier because neither Wise nor Kovacevic discloses an identifier. Further, a person of ordinary skill in the art would not modify Wise in the manner respondents suggest because doing so would fundamentally change how Wise operates. *See* CX-0579C (Acton RWS) at Q/A 278 (“modifying Wise to search for stream_id specifically, which, as I discussed previously is what Kovacevic’s, “next byte” is, would require restructuring the entire decoding process.”); *see also id.* at Q/A 282 (“Wise discloses a multi-chip system in which the decoding portion is performed on separate chips, while the Start Code Detector exists on a separate chip. This is in contrast to claim 11 of the ‘059 patent, which requires that the identification and decoding occur on a single chip.”); *see also Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App’x 755, 758 (Fed. Cir. 2015) (“combinations that change the ‘basic principles under which the [prior art] was designed to operate,’ . . . may fail to support a conclusion of obviousness.”).

Accordingly, the administrative law judge has determined that Wise, in view of Kovacevic, does not disclose this limitation.

- e) ***[D] decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process.***

Respondents argue:

Limitation 11[d]: The Wise-Kovacevic system renders obvious “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process” because the combined system would include Wise’s Huffman Decoder and Parser, which decodes differently encoded bit streams using the selected standard-dependent program, which is “utilizing said selected decoding process,” as recited in the claim. RX-0383C (Stevenson) Q394; RDX-0014.35-36 (Wise Chart); RDX-0383.8 (Stevenson Demonstratives); RX-0339 (Wise) at ¶¶ [0375], [0080]. For example, Wise states that the parser state machine operates with a different program—the “selected decoding process”—for each of the standards and issues the correct command to the Huffman decoder at different times consistent with the standard in operation, which allows the

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Huffman decoder to decode data words encoded according to the Huffman coding provisions of either H.261, JPEG or MPEG standards. RX-0383C (Stevenson) Q394; RX-0339 (Wise) at ¶¶ [0080], [0374]-[0375], [0442].

Resps. Br. at 168.

Broadcom argues that “Respondents have not shown that the alleged Wise-Kovacevic system performs decoding on a single chip, as required by claim 11, because Wise discloses a multi-chip system where the decoding is performed on separate chips.” Broadcom Br. at 281.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence that the “Wise-Kovacevic system”⁶⁸ uses an identifier to determine an encoding type and because it is not clear that the Huffman Decoder and parser that respondents rely upon are on a single chip, as the claim requires. *See* CX-0579C (Acton RWS) at Q/A 282.

2. Claims 12

Respondents argue:

The Wise-Kovacevic system renders obvious “determining on said chip, a start code within said received packetized data that separates packets within the encoded video stream” because it incorporates Wise’s Start Code Detector. RX-0383C (Stevenson) Q395; RDX-0014.36-37 (Wise Chart); RDX-0383.7 (Stevenson Demonstratives).

Respondents’ Construction: Respondents’ claim construction requires that the start code be “distinct from the identifier.” As noted for claim 11, the Wise-Kovacevic combination would utilize Kovacevic’s “next byte” after the start code of Wise. RX-0383C (Stevenson) Q388-390. Therefore, the Wise-Kovacevic system, when matching the start code as described in Wise, would match a code distinct from Kovacevic’s “next byte,” which is the identifier in the combined system.

⁶⁸ Although respondents refer to a “Wise-Kovacevic system,” no single system exists; the moniker is a shorthand that refers to the hypothetical combination of Wise and Kovacevic.

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Complainant's Construction: For these same reasons, the combination of Wise and Kovacevic also satisfies Complainant's construction—plain and ordinary meaning.

Resps. Br. at 168-69.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579C (Acton WS) at Q/A 285-306.

Broadcom Br. at 283.

The administrative law judge previously determined that respondents have not shown that claim 11 is obvious based on Wise and Kovacevic. The administrative law judge finds that claim 12 is not obvious due to its dependency from claim 11. *See MEMS Tech. Berhad v. Int'l Trade Comm'n*, 447 F. App'x 142, 158 (Fed. Cir. 2011) ("Because independent claim 1 was not obvious over Baumhauer alone or in view of Kress, the Commission correctly determined that dependent claims 2, 9, 15, 17, 20, 28, and 29 were also not obvious.").

If claim 11 is later found obvious, the administrative law judge would find claim 12 obvious based on Dr. Stevenson's analysis. *See* RX-0383C (Stevenson WS) at Q/A 395.

3. Claim 13

Respondents argue:

The Wise-Kovacevic system renders obvious "matching a plurality of bytes within said received packetized data with a determined byte sequence" because it discloses that "the start code detector searches for a specific start code corresponding to one of multiple compression standards," such as MPEG and H.261. RX-0383C (Stevenson) Q396; RDX-0014.37-38 (Wise Chart); RX-0339 (Wise) at Abstract, ¶ [0963]. Wise further describes that searching employs a fifteen bit wide shift register to match the start code to entries in a lookup table. RX-0383C (Stevenson) Q396; RX-0339 (Wise) at ¶¶ [0325]-[0326] and [1586]-[1596]. Wise also states

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that a start code can be 3 bytes, and matching that is matching a plurality of bytes. RX-0383C (Stevenson) Q396; RX-0339 (Wise) at ¶ [0477].

Resps. Br. at 169.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579C (Acton WS) at Q/A 285-306.

Broadcom Br. at 283.

The administrative law judge previously determined that respondents have not shown that claims 11 and 12 are obvious based on Wise and Kovacevic. The administrative law judge finds that claim 13 is not obvious due to its dependency from claims 11 and 12. *See MEMS Tech. Berhad v. Int'l Trade Comm'n*, 447 F. App'x 142, 158 (Fed. Cir. 2011) ("Because independent claim 1 was not obvious over Baumhauer alone or in view of Kress, the Commission correctly determined that dependent claims 2, 9, 15, 17, 20, 28, and 29 were also not obvious.").

If claims 11 and 12 are later found obvious, the administrative law judge would find claim 13 obvious based on Dr. Stevenson's analysis. *See* RX-0383C (Stevenson WS) at Q/A 396.

4. Claim 14

Respondents argue:

Wise discloses "removing said plurality of bytes from said received packetized data, if said plurality of bytes matches said determined byte sequence." RX-0383C (Stevenson) Q397; RDX-0014.39 (Wise Chart). The Wise-Kovacevic system would render claim 14 obvious because Wise states when performing the operations of the Start Code Detector:

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Since the contents of the detect shift register has been identified as a start code, its contents must be removed from the two wire interface to ensure that no further processing takes place using these 3 bytes.

RX-0383C Q397; RX-0339 (Wise) at ¶ [0477]; *see also* RX-0339 at ¶¶ [0462], [1600]-[1602]. Therefore, Wise discloses removing the matched plurality of bytes. RX-0383C Q397.

Resps. Br. at 169-70.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579C (Acton WS) at Q/A 285-306.

Broadcom Br. at 283.

The administrative law judge previously determined that respondents have not shown that claims 11-13 are obvious based on Wise and Kovacevic. The administrative law judge finds that claim 14 is not obvious due to its dependency from claims 11-13. *See MEMS Tech. Berhad v. Int'l Trade Comm'n*, 447 F. App'x 142, 158 (Fed. Cir. 2011) ("Because independent claim 1 was not obvious over Baumhauer alone or in view of Kress, the Commission correctly determined that dependent claims 2, 9, 15, 17, 20, 28, and 29 were also not obvious.").

If claims 11-13 are later found obvious, the administrative law judge would find claim 14 obvious based on Dr. Stevenson's analysis. *See* RX-0383C (Stevenson WS) at Q/A 397.

5. Claims 15 and 16

Respondents argue, in part:

Based on the knowledge of one ordinary skill at the time of the '059 Patent, the Wise-Kovacevic system renders obvious "decoding ... utilizing one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process and/or a context adaptive binary arithmetic coding (CABAC) process, if said

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determined identifier corresponds to H.264 video encoding” (claim 15), as well as “decoding ... utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to VC-1 video encoding” (claim 16). RX-0383C (Stevenson) Q398, 400; RDX-0014.40-44 (Wise Chart).

Claims 15 and 16 are similar to claim 17 below, except that they require identifiers for standards that had yet to be established at the time of Wise and Kovacevic, namely identifiers for H.264 and VC-1, respectively. However, the ‘059 Patent admits that H.264 and VC-1 standards are prior art (JX-0002 (‘059 Patent) at 2:21-24), and those of ordinary skill would have known at that time that those standards use variable length coding processes. RX-0383C (Stevenson) Q398-400; RX-0678 (‘081 Prov. App.) at 54-58, 366-367. The ‘081 provisional application—which contains a specification of VC Version 9.0, also known as Windows Media Video V9 Decoding Specification, what the standard was called before it became VC-1—evidences the state of the art with regard to the VC-1 standard, specifically that it includes fixed length and variable length coding. RX-0383C (Stevenson) Q400; *see also* RX-0678 (‘081 Prov. App.) at 54-58. Similarly, Wiegand evidences the same for the H.264 Standard.

Resps. Br. at 170.

For Claim 15, Broadcom argues:

Respondents have failed to show that either the combination of Wise in view of Kovacevic or Wise in view of Kovacevic and Wiegand renders obvious claim 15, which requires “code for decoding said at least a portion of said received packetized data utilizing one or more of a fixed length coding (FLC) process, a variable length coding (VLC) process and/or a context adaptive binary arithmetic coding (CABAC) process, if said determined identifier corresponds to H.264 video encoding.” As an initial matter, Respondents have not shown by clear and convincing evidence that it would have been obvious to modify Wise and Kovacevic in view of Wiegand and that a POSA would have had a reasonable expectation of success in making the modification. As Dr. Stevenson admits, (CX-0383 (Stevenson WS) at Q/A 398), Wise predates the H.264 standard and Kovacevic explicitly states at paragraph [0066] that it is specifically directed to “exploiting similarities between MPEG-1 and MPEG-2 data.” Thus, a POSA would not be motivated to modify the Wise-Kovacevic system to process H.264 encoded video streams. CX-0579C (Acton WS) at Q/A 293-296.

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Broadcom Br. at 281.

For claim 16, Broadcom argues:

Respondents have not shown that Wise in view of Kovacevic discloses or renders obvious claim 16, which requires “code for decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to VC-1 video encoding.” Respondents have not established by clear and convincing evidence that POSA would not be motivated to modify Wise in view of Kovacevic to process VC-1 encoded video streams because Wise predates the VC-1 standard and Kovacevic explicitly states at paragraph [0066] that it is specifically directed to “exploiting similarities between MPEG-1 and MPEG-2 data.” Thus, a POSA would not have been motivated to modify the Wise-Kovacevic system to process VC-1 encoded video streams. CX-0579C (Acton WS) at Q/A 298.

Additionally, if Dr. Stevenson and Respondents are relying on U.S. Provisional Application 60/501,081 (“the ‘081 provisional application”) (RX-0678), as discussed above in the Kovacevic analysis, the ‘081 provisional application fails to meet the prior art requirements of 35 U.S.C. § 102(a). *See Mortgage Grader*, 2014 WL 10763261 at *4.

Broadcom Br. at 282.⁶⁹

a) Claim 15

The administrative law judge previously determined that claim 11 is not obvious based on Wise and Kovacevic. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 15 is obvious based on Wise, Kovacevic, and Wiegand. As Dr. Stevenson testified, implementing H.264 functionality in the “Wise-Kovacevic system” would have been desirable and predictable, particularly in light of Wise’s recognition that it can be used with “standards may include JPEG, MPEG, and/or H.261,

⁶⁹ In reply, respondents argue: “Respondents do not rely on the ‘081 provisional application as a prior art reference, but to show the state of the art as to VC-1, namely that it used FLC and VLC coding. Broadcom does not dispute this or that VC-1 is prior art to the ‘059 Patent. Indeed, the ‘059 Patent’s background admits that VC-1 was known.” Resps. Reply at 66.

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or any other standards and any combination of such picture standards[.]” *See* RX-0383C (Stevenson WS) at Q/A 398-99; RX-0339, ¶ 53.

b) Claim 16

The administrative law judge previously determined that claim 11 is not obvious based on Wise and Kovacevic. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 16 is obvious based on Wise, Kovacevic, and VC-1. As Dr. Stevenson testified, implementing VC-1 functionality in the “Wise-Kovacevic system” would have been desirable and predictable, particularly in light of Wise’s recognition that it can be used with “standards may include JPEG, MPEG, and/or H.261, or any other standards and any combination of such picture standards[.]” *See* RX-0383C (Stevenson WS) at Q/A 400; RX-0339, ¶ 53.

6. Claim 17

Respondents argue:

The Wise-Kovacevic system renders obvious “decoding said at least a portion of said received packetized data utilizing one or both of a FLC process and/or a VLC process, if said determined identifier corresponds to one or more of H.261, H.263, H.263+, MPEG-1, MPEG-2 and/or MPEG-4 video encoding.” RX-0383C (Stevenson) Q401; RDX-0014.44-47 (Wise Chart). Wise discloses a VLC decoding process and a FLC decoding process as part of the operation of the Huffman Coder for H.261 and MPEG. RX-0383C (Stevenson) Q401; RX-0339 (Wise) at ¶ [1690], Fig. 119. And, as discussed for limitations 11[b] and 11[d], that decoding process is performed by the Huffman Decoder and Parser when the identifier determined by the Wise-Kovacevic system corresponds to H.261. RX-0383C Q401.

Resps. Br. at 171-72.

Broadcom argues:

Respondents have not shown that dependent claims 12-20 are invalid in view of the asserted prior art because Respondents have

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not shown by clear and convincing evidence that independent claim 11 is anticipated or rendered obvious by the asserted prior art. CX-0579C (Acton WS) at Q/A 285-306.

Broadcom Br. at 283.

The administrative law judge previously determined that respondents have not shown that claim 11 is obvious based on Wise and Kovacevic. The administrative law judge finds that claim 17 is not obvious due to its dependency from claim 11. *See MEMS Tech. Berhad v. Int'l Trade Comm'n*, 447 F. App'x 142, 158 (Fed. Cir. 2011) ("Because independent claim 1 was not obvious over Baumhauer alone or in view of Kress, the Commission correctly determined that dependent claims 2, 9, 15, 17, 20, 28, and 29 were also not obvious.").

If claim 11 is later found obvious, the administrative law judge would find claim 17 obvious based on Dr. Stevenson's analysis. *See* RX-0383C (Stevenson WS) at Q/A 401.

7. Claim 18

Respondents argue:

The Wise-Kovacevic system renders obvious "said decoded packetized data compris[ing] one or both of prediction pixels information and/or prediction error information." RX-0383C (Stevenson) Q402; RDX-0014.48-50 (Wise Chart). This is because Wise discloses performing motion compensation in which "[t]he prediction uses motion vectors to provide offsets into the past and/or future reference pictures containing previously decoded pel values that are used to form the prediction error signal." RX-0383C (Stevenson) Q402; RX-0339 (Wise) at ¶ [0129]; *see also* RX-0339 at ¶ [0401]. And, motion compensation is performed by the Temporal Decoder of Wise in accordance with the received CODING_STANDARD Token. RX-0383C (Stevenson) Q402; RX-0339 (Wise) at ¶ [1370].

To the extent that Wise does not expressly disclose that its spatial decoder chip and the temporal decoder chip can be implemented in a single chip, and to the extent that is required, Wise renders it obvious. For example, Wise discloses that the spatial decoder and the temporal decoder are readily combinable. RX-0383C (Stevenson) Q402; RX-0339 (Wise) at ¶¶ [0623]-[0632]; RDX-

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0383.9 (Stevenson Demonstratives). Therefore, combining these chips would have been obvious because Wise discloses that and because in the 10 years from Wise (to the time of the alleged invention of the '059 Patent) many systems combined the processing functions of spatial and temporal decoders into one chip. RX-0383C (Stevenson) Q402.

Resps. Br. at 172.

Broadcom argues:

Respondents have not shown by clear and convincing evidence that Wise in view of Kovacevic renders obvious claims 18 or 19, which recite that “decoded packetized data comprises one or both of prediction pixels information and/or prediction error information” and “code for generating a decoded video stream utilizing at least a portion of said decoded packetized data,” respectively. Respondents have failed to show that the alleged Wise-Kovacevic system renders claims 18 and 19 obvious because Wise discloses multiple chips, not a single chip as claimed by the '059 Patent. CX-0579C (Acton WS) at Q/A 301-304.

Broadcom Br. at 282.

Respondents reply:

Broadcom also argues that Wise does not render claim 11 obvious “because Wise discloses a multi-chip system where the decoding is performed on separate chips.” CPostHg. Br. at 281. Broadcom is incorrect. Wise discloses that its input circuit, start code detector, and Huffman decoder are all on the same chip. RX-0383C (Stevenson) Q393-394; RDX-0383.006-008; RX-0339 (Wise), Fig. 58. Accordingly, Broadcom’s critiques of the Wise-Kovacevic combination for claim 11 lack merit.

Resps. Reply at 67-68.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the “Wise-Kovacevic system” discloses packetized data comprising prediction pixels information or prediction error information for the reasons provided with respect to claim 11. *See* CX-0579C (Acton RWS) at Q/A 302. Further, Wise does not disclose placing the claimed components on a

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single chip. *Id.* at Q/A 282, 302. Dr. Stevenson's testimony to the contrary is not clear and convincing, and is unsupported with respect to industry developments in the time between Wise and the '059 Patent. Accordingly, the administrative law judge has determined that claim 18 would not have been obvious based on Wise and Kovacevic.

8. Claim 19

Respondents argue:

The Wise-Kovacevic system renders obvious "code for generating a decoded video stream utilizing at least a portion of said decoded packetized data." RX-0383C (Stevenson) Q403; RDX-0014.50-56 (Wise Chart). Wise discloses decoding performed by the Temporal Decoder that generates a decoded video stream utilizing at least a portion of said decoded packetized data this because it takes decoded data from the Huffman Decoder and Parser of the Spatial Decoder and uses generate a decoded video stream. RX-0383C (Stevenson) Q403; RX-0339 (Wise) at ¶¶ [0044]-[0046], [0313], [0314], and [0363], Figs. 58, 83; RDX-0383.9 (Stevenson Demonstratives).

As discussed for claim 18, to the extent that Wise does not expressly disclose that its spatial decoder chip and the temporal decoder chip can be implemented in a single chip, and to the extent that is required, Wise renders it obvious. Or alternatively, claim 19 does not require a single chip satisfy all limitations. Either way, the Wise-Kovacevic system renders obvious claim 19. RX-0383C (Stevenson) Q403.

Resps. Br. at 172-73.

Broadcom argues:

Respondents have not shown by clear and convincing evidence that Wise in view of Kovacevic renders obvious claims 18 or 19, which recite that "decoded packetized data comprises one or both of prediction pixels information and/or prediction error information" and "code for generating a decoded video stream utilizing at least a portion of said decoded packetized data," respectively. Respondents have failed to show that the alleged Wise-Kovacevic system renders claims 18 and 19 obvious because Wise discloses multiple chips, not a single chip as claimed by the '059 Patent. CX-0579C (Acton WS) at Q/A 301-304.

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Broadcom Br. at 282.

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the "Wise-Kovacevic system" discloses code for generating a decoded video stream using decoded packetized data for the reasons provided with respect to claim 11. *See* CX-0579C (Acton RWS) at Q/A 304. Further, Wise does not disclose placing the claimed components on a single chip. *Id.* at Q/A 282, 302, 304. Dr. Stevenson's testimony to the contrary is not clear and convincing, and is unsupported with respect to industry developments in the time between Wise and the '059 Patent. Accordingly, the administrative law judge has determined that claim 19 would not have been obvious based on Wise and Kovacevic.

N. Obviousness – Wise in view of Kovacevic and Wiegand

Respondents argue that "Wise and Kovacevic in view of Wiegand renders obvious claim 20 of the '059 Patent under any proposed construction." "Wiegand" is the H.264/AVC Video Coding Standard (RX-0279).⁷⁰

For claim 20, respondents argue:

Wise-Kovacevic in view of Wiegand renders obvious "code for filtering said generated decoded video stream utilizing one or both of an overlapped transform process and/or a deblocking process." RX-0383C (Stevenson) Q404; RDX-0014.56-57 (Wise Chart). Specifically, it would have been obvious to one of ordinary skill to include a processor that performs a deblocking filter after the video stream is decoded in the Temporal Decoder of the Wise-Kovacevic system. RX-0383C (Stevenson) Q404. In Wise, the Temporal Decoder performs various filter operations. RX-0383C

⁷⁰ Respondents argue that the H.264/AVC Video Coding Standard (RX-0279) ("Wiegand") was "published in IEEE Transactions on Circuits and Systems for Video Technology" in July 2003 and is prior art "under 35 U.S.C. §§ 102(a) and (b)." Broadcom does not clearly rebut this argument. Accordingly, the administrative law judge has determined that Wiegand is prior art under 35 U.S.C. § 102(a) and § 102(b).

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(Stevenson) Q404; RX-0339 (Wise) at Table B.12.2 1-D. To the extent that a deblocking filter is not recited as one of the filter operations, it would have been obvious to include H.264 in the standards that Wise accommodates, as discussed with regard to claim 15, which includes a deblocking filter. RX-0383C (Stevenson) Q404. And because that filter is part of the H.264 standard, one of ordinary skill would have configured the Temporal Decoder to include the deblocking filter of the H.264 standard to accommodate decoding H.264. RX-0383C (Stevenson) Q404; RX-0279 (Wiegand) at 562. Several advantages of including a deblocking filter were well known—“Application of an adaptive deblocking filter is a well-known method of improving the resulting video quality, and when designed well, this can improve both objective and subjective video quality”—making it a desirable and obvious modification. RX-0383C (Stevenson) Q404; RX-0279 (Wiegand) at 562.

Resps. Br. at 173-74.

Broadcom argues:

Respondents have not shown that either the combination of Wise in view of Kovacevic or Wise in view of Kovacevic and Wiegand renders obvious claim 20, which recites “code for filtering said generated decoded video stream utilizing one or both of an overlapped transform process and/or a deblocking process.” Respondents have not shown that a POSA would have had a reasonable expectation of success modifying the alleged Wise-Kovacevic system in view of Wiegand because the Wise-Kovacevic system does not disclose deblocking or overlapped transform processes. Additionally, Respondents have not established by clear and convincing evidence that a POSA would have modified the alleged Wise-Kovacevic system in view of the H.264 standard because Wise predates the H.264 standard, and Kovacevic states at paragraph [0066] that it is specifically directed to “exploiting similarities between MPEG-1 and MPEG-2 data.” Thus, a POSA would not be motivated to modify the Wise-Kovacevic system to process H.264 encoded video streams. CX-0579C (Acton WS) at Q/A 306.

Broadcom Br. at 283.

In reply, respondents argue “But as Respondents have shown, and as Dr. Stevenson testified, one would expect the combination to work due to the similarities between the filter

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operations of Wise's temporal decoder and Wiegand's deblocking filter. RX-0383C (Stevenson) Q404. And the advantages of deblocking filters known to those skilled in the art would motivate one to make the combination. *Id.*"

Having considered the parties' arguments, the administrative law judge has determined that respondents have not shown that a person of ordinary skill in the art would have modified the combination of Wise and Kovacevic (the so-called "Wise-Kovacevic system") in the manner respondents suggest. In particular, Dr. Stevenson's assertion that a person of ordinary skill would have had success in combining three systems (Wise, Kovacevic, and Wiegand) is speculative, particularly "because the proposed Wise-Kovacevic combination does not disclose deblocking or overlapped transform processes." CX-0579C (Acton RWS) at Q/A 306.

Accordingly, the administrative law judge has determined that claim 20 would not have been obvious based on Wise, Kovacevic, and Wiegand.

O. Obviousness – Quasar Chip (claims 11-20)

Respondents argue:

The EM8550 Quasar chip anticipates or renders obvious claims 11-20 of the '059 Patent under Complainant's proposed claim constructions. RX-0383C at Q435; RDX-0016. In addition, claim 15 would have been obvious in view of the EM8550 Quasar chip and the H.264 Standard; claim 16 would have been obvious in view of the EM8550 Quasar chip and VC-1 standard; claim 18 would have been obvious in view of the EM8550 Quasar chip and MPEG2 Standard; and claim 20 would have been obvious in view of the EM8550 Quasar chip and H.264 Standard. RX-0383C at Q435; RDX-0016.

Resps. Br. at 176. Respondents' brief, however, limits obviousness to claims 11, 12, 15, 16, and 18-20. *See id.* at 176-87.

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1. Claim 11

For limitations [a], [c], and [d] from claim 11, respondents argue that if they are found to infringe claim 11, the 8550 Quasar chip “anticipates or renders obvious the ‘059 Patent for the same reasons.” Resps. Br. at 178, 180 (citing RX-0383C (Stevenson WS) at Q/A 438, 440, 441). Respondents and Dr. Stevenson, however, argue that the 8550 Quasar chip discloses subject matter, not that it “renders obvious” limitations [a], [c], or [d]. For example, Dr. Stevenson testified as follows:

Q441. How does the Quasar Chip disclose the limitation “decoding on said chip, at least a portion of said received packetized data in the encoded video stream utilizing said selected decoding process”?

A441. To the extent Broadcom’s successfully argues that the processors in Sigma’s Accused Products perform a decoding function, then Sigma’s EM8550/Quasar Chip anticipates or renders obvious the ‘059 patent for the same reasons. This is because the
[

] My analysis

for limitations 11[a-c] also applies equally here.

RX-0383C (Stevenson WS) at Q/A 441. Respondents (and Dr. Stevenson) do not argue that the 8550 should be modified in any way. *See* Resps. Br. at 178, 180; RX-0383C (Stevenson WS) at Q/A 438, 440, 441.

Further, respondents have not analyzed “the differences between the claimed invention and the prior art” as 35 U.S.C. § 103 requires. *Graham v. John Deere*, 383 U.S. at 17 (“Under § 103, the scope and content of the prior art are to be determined; differences between the prior

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art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved.”).

Accordingly, the administrative law judge finds that respondents have failed to show that claim 11 would have been obvious based upon the Quasar Chip alone.

2. Claim 12

Respondents argue: “Broadcom contends Respondents cannot show [claim 12] is met because it would not have been obvious to one of ordinary skill to combine the Quasar chip documents.” Resps. Br. at 181 (RX-0383C (Stevenson WS) at Q/A 442). Dr. Stevenson’s testimony in Q/A 442 does not discuss obviousness.

Accordingly, the administrative law judge finds that respondents have failed to show that claim 12 would have been obvious based upon the Quasar Chip alone.

3. Claim 15

Respondents argue, in part:

The EM8550 Quasar chip meets claim 15 for the same reasons as claim 11. RX-0383C at Q445. [

] RX-0383C at Q445-

450.

Resps. Br. at 182.

Broadcom argues:

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Respondents have not established for dependent claims 15, 16, 18, and/or 20 that it would be obvious to combine the “Quasar Chip” with any of the H.264 Standard, VC-1, and/or MPEG-2 Video. [CX-0579C (Acton RWS)] at Q/A 387, 389, 395, 401.

Broadcom Br. at 288.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the 8550 Quasar chip “renders obvious” claim 15 based upon the same evidence and analysis relied upon in discussing claim 11. *See* CX-0579C (Acton RWS) at Q/A 387.

4. Claim 16

Respondents argue, in part:

The EM8550 Quasar chip meets claim 16 for the same reasons as claims 11 and 15. RX-0383C at Q451. [

]. *Id.*;

see RX-0678.

Resps. Br. at 183.

Broadcom argues:

Respondents have not established for dependent claims 15, 16, 18, and/or 20 that it would be obvious to combine the “Quasar Chip” with any of the H.264 Standard, VC-1, and/or MPEG-2 Video. [CX-0579C (Acton RWS)] at Q/A 387, 389, 395, 401.

Broadcom Br. at 288.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the 8550 Quasar chip “renders obvious” claim 16 based upon the same evidence and analysis relied upon in discussing claim 11. *See* CX-0579C (Acton RWS) at Q/A 389.

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5. Claim 18

Respondents argue “To the extent the EM8550 Quasar chip does not anticipate or render obvious claim 18 of the ‘059 Patent on its own, the EM8550 Quasar chip in view of the MPEG2 Standard renders claim 18 obvious. RX-383C at Q454-458; RX-271” Resps. Br. at 186.

The cited testimony, however, does not address obviousness based on the 8550 Quasar Chip alone. *See* RX-0383C (Stevenson WS) at Q/A 453-458. Accordingly, the administrative law judge finds that respondents have failed to show that claim 18 would have been obvious based upon the Quasar Chip alone.

6. Claim 19

Respondents argue:

The EM8550 Quasar chip meets claim 19 for the same reasons as claim 11. RX-383C at Q/A 459. This is because the EM8550 Quasar chip alone or in combination with the knowledge of one of ordinary skill at the time of the invention anticipates and/or renders obvious this limitation. *Id.*

Resps. Br. at 186.

The cited testimony is conclusory and does not substantively address obviousness based on the 8550 Quasar Chip alone. *See* RX-0383C (Stevenson WS) at Q/A 459.⁷¹ Accordingly, the administrative law judge finds that respondents have failed to show that claim 19 would have been obvious based upon the Quasar Chip alone.

7. Claim 20

Respondents argue:

⁷¹ The relevant testimony states: “This is because the Quasar Chip alone or in combination with the knowledge of a POSITA at the time of the invention anticipates and/or renders obvious this limitation. Claim 19 requires code for generating a decoded video stream utilizing at least a portion of the decoded packetized data. As discussed above, the Quasar Chip discloses [].”

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To the extent the EM8550 Quasar chip does not anticipate or render obvious claim [20] of the '059 Patent on its own, the EM8550 Quasar chip in view of the H.264 Standard renders claim 20 obvious. RX-383C at Q461-462. Claim 20 requires code for generating a decoded video stream utilizing at least a portion of said decoded packetized data. *Id.* at Q462. The EM8550 Quasar chip in combination with H.264 renders this claim obvious. *Id.*
I

J.

Resps. Br. at 187.

Broadcom argues:

Respondents have not established for dependent claims 15, 16, 18, and/or 20 that it would be obvious to combine the “Quasar Chip” with any of the H.264 Standard, VC-1, and/or MPEG-2 Video. [CX-0579C (Acton RWS)] at Q/A 387, 389, 395, 401.

Broadcom Br. at 288.

The administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the 8550 Quasar “renders obvious” claim 11 based upon the same evidence and analysis relied upon in discussing claim 11. *See* CX-0579C (Acton RWS) at Q/A 401.

For the combination of the Quasar Chip and the H.264 standard, the administrative law judge has determined that respondents have shown, through clear and convincing evidence, that the 8550 Quasar chip discloses the subject matter particular to claim 20, and that a person of ordinary skill in the art would have been able to modify the 8550 Quasar chip to accommodate the new H.264 standard, as had been done with rolling out previous standards. *Id.* at Q/A 445.

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P. Obviousness – Quasar Chip in view of H.264 Standard

1. Claim 15

The administrative law judge previously determined that claim 11 is not obvious based on the 8550 Quasar chip. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 15 is obvious based on the 8550 Quasar chip and the H.264 Standard.

In particular, respondents have shown, through clear and convincing evidence, that RX-0270 discloses decoding using a FLC, VLC, or CABAC process with a H.264 identifier, as claim 15 requires. *See* RX-0383C (Stevenson WS) at Q/A 449-50. Further, a person of ordinary skill in the art would have been able to modify the 8550 to accommodate the new H.264 standard, [

].

2. Claim 20

The administrative law judge previously determined that claim 11 is not obvious based on the 8550 Quasar chip. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 20 is obvious based on the 8550 Quasar chip and the H.264 Standard. In particular, respondents have shown, through clear and convincing evidence, that RX-0270 discloses filtering the decoded video stream utilizing one or both of an overlapped transform process and/or a deblocking process.

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Q. Obviousness – Quasar Chip in view of VC-1 standard

The administrative law judge previously determined that claim 11 is not obvious based on the 8550 Quasar chip. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 16 is obvious based on the 8550 Quasar chip and the VC-1 Standard.

In particular, respondents have shown, through clear and convincing evidence, that RX-0270 discloses decoding using a FLC or VLC with a VC-1 identifier, as claim 16 requires. *See* RX-0383C (Stevenson WS) at Q/A 451. Further, a person of ordinary skill in the art would have been able to modify the 8550 to accommodate the VC-1 standard, [

].

R. Obviousness – Quasar Chip in view of MPEG-2 standard

Respondents argue, in part:

To the extent the EM8550 Quasar chip does not anticipate or render obvious claim 18 of the '059 Patent on its own, the EM8550 Quasar chip in view of the MPEG2 Standard renders claim 18 obvious. RX-383C at Q454-458; RX-271. . . .

Resps. Br. at 186.

The administrative law judge previously determined that claim 11 is not obvious based on the 8550 Quasar chip. If it is later determined that claim 11 is obvious, the administrative law judge would find that respondents have also shown that claim 18 is disclosed based on the 8550 Quasar chip and the MPEG-2 Video Standard, but respondents have not shown that a person of ordinary skill in the art would modify the Quasar chip based on the MPEG-2 Video standard.

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In particular, respondents have shown, through clear and convincing evidence, that RX-0271 discloses packetized data comprising prediction pixels information or prediction error information, as claim 18 requires. *See* RX-0383C (Stevenson WS) at Q/A 458. However, Dr. Stevenson's motivation-to-combine analysis simply refers to Q/A 452, which does not have any analysis. Accordingly, the administrative law judge finds that respondents have not shown claim 18 would have been obvious.

S. Obviousness – Secondary Considerations

Respondents' entire argument is:

Broadcom has not provided evidence of secondary considerations supporting non-obviousness of the '059 Patent. Respondents agree that no secondary considerations exist

Resps. Br. at 187; see also Resps.

Broadcom has not clearly argued that secondary considerations support a non-obviousness finding. *See generally* Broadcom Br., Section V(B)(6) (*e.g.*, commercial success, unexpected results, long-felt need, failure of others, etc. are not discussed); Broadcom Reply, Section III(D).

Accordingly, the administrative law judge has determined that, with respect to all of the obviousness arguments respondents have raised, no secondary consideration supports a non-obviousness finding.

T. Written Description

Respondents' entire argument is:

The '059 Patent is invalid for lack of written description, lack of enabling disclosure, and/or indefiniteness based on the "packetized data within the encoded video stream" term. RX-0383C Q318-321. If the term "packetized data within the encoded video stream" is construed to encompass a transport stream, claims 11-20 of the '059 Patent are invalid under § 112 *for lack of written*

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description. *Id.* Specifically, the ‘059 Patent provides no support or disclosure for the “packetized data within the encoded video stream” being a transport stream or for the claimed identifier covering syntax in the transport stream, such as the “stream_type” syntax of MPEG-2 Systems standard. *Id.* at Q319. The ‘059 Patent mentions neither “transport” nor “transport stream,” and one of ordinary skill would not understand those concepts to be part of the ‘059 Patent. *Id.* at Q320. To the contrary, the ‘059 Patent consistently discloses “video elementary codestream ‘401” being input into the “code in port” of the “multistandard video decoder.” *Id.* at Q320; JX-0002 (‘059 Patent) at Figs. 4, 4a, 4b, 5, 6, 7 and 8. And, before the ‘059 Patent, those skilled in the art recognized a distinction between transport streams and elementary streams and, therefore, would have understood that the lack of discussion of any transport streams in the ‘059 Patent means that transport streams are not part of its invention. RX-0383C (Stevenson) Q321.

Resps. Br. at 187-88 (emphasis added).⁷²

Broadcom argues:

Respondents have not shown that claims 11-20 of the ‘059 Patent are invalid for failure to satisfy the written description requirement regardless of how the term “packetized data within the encoded video stream” is construed. Respondents contend that to the extent “packetized data within the encoded video stream” is defined to include a transport stream, the written description requirement is not satisfied. CX-0383C (Stevenson WS) at Q/A 319. Respondents’ contention is refuted by the evidence of record. Specifically, the evidence shows that a POSA would have understood that an encoded video stream can include several layers of communication, including transport stream packets or PES packets. For example, the MPEG-2 (Part 1) encapsulation standard states at pages vii and 5 that it includes “transport packets,” “program stream packets,” and “Packetized Elementary Stream (PES) packets.” CX-0579C (Acton WS) at Q/A 225.

Broadcom Br. at 272-73.

Respondents reply:

⁷² Respondents present no argument concerning enablement or indefiniteness. *See* RX-0383C (Stevenson WS) at Q/A 319-21 (Dr. Stevenson’s testimony pertains to the written description requirement).

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Broadcom contends that “packetized data within the encoded video stream” is broad enough to include a transport stream or program stream. CPostHg. Br. 274. Broadcom, however, fails to show any support in the specification for this overly broad interpretation. *Id.* Instead, Broadcom relies on the use of the word “may” in the sentence: “the encapsulated video payload 100 *may* comprise a delimiter 104 and elementary stream data 105.” CPostHg. Br. at 273 (emphasis in original). But Broadcom recognizes elsewhere that the different identified standards may have different formats for their delimiters, start codes, and stream data. *See, e.g.,* Tr. (Acton) at 876:4-877:1. That does not change the fact that they would nonetheless still be in an elementary stream. Broadcom’s arguments amount to its contention that one of skill would understand how to determine an encoding type using a transport stream or program stream—which is no surprise given that the standards indicating as much predated the ‘059 Patent by years (*see, e.g.,* Section I.A.1.a). But that is the test for enablement, not the separate written description requirement. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). Broadcom fails to show that one of skill would read the ‘059 Patent and understand that the inventor was in possession of anything other than analyzing an elementary stream. *Id.* at 1351 (“[T]he [written description] test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art.”)

Broadcom also relies on the reference elsewhere to multiple standards. CPostHg. Br. at 273. Reference to those standards, however, is in the context of an *elementary* video stream encoded according to those standards, and does not support using any other streams from them. JX-0002 (‘059 Patent) at 4:35-42. Put simply, the ‘059 Patent discloses *video encoding* standards, whereas the MPEG-2 Transport Stream is a *transport container* standard. That other streams “are also basic elements of standards since the mid-1990s” further shows that by specifically referring to only *elementary* streams in the ‘059 Patent, one of skill would understand that the ‘059 Patent only meant to cover elementary streams.

Respondents Reply at 73-74.

Having considered the parties’ arguments, the administrative law judge has determined that respondents have not shown, through clear and convincing evidence, that the specification does not comply with the written description requirement. Respondents’ arguments are

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repetitious claim construction arguments. Respondents have failed to show that the inventors did not possess and convey the claimed subject matter (*e.g.*, receiving packetized data within an encoded video stream). Further, as Dr. Acton testified, a person of ordinary skill in the art would have understood that “an encoded video stream can include several layers of communication.” CX-0579C (Acton RWS) at Q/A 225. The patentee is not required to disclose every last, particular detail with respect to a claim term that covers more than one technical variant. *See Ariad*, 598 F.3d at 1351 (explaining that there are no “bright-line rules governing, for example, the number of species that must be disclosed to describe a genus claim, as this number necessarily changes with each invention, and it changes with progress in a field.”). Accordingly, the administrative law judge has determined that respondents have not shown the ‘059 Patent does not comply with the written description requirement.

VII. DOMESTIC INDUSTRY – ECONOMIC PRONG

In arguing that it has a domestic industry for products that practice the asserted patents exists, Broadcom relies on the set-top-box products represented by the []. *See* § I(D) (finding that the [] is representative), *supra*; Broadcom Br. at 288.

Broadcom’s investments are reported for its set-top box (STB) division. As Broadcom does not track its investments by product, *see* CX-0001C (Aberle WS) at Q/A 38, Broadcom provided a sales allocation “to determine the amount attributable to the DI Products rather than the STB Division as a whole or the DI Product Lines, which include the DI Products and other non-asserted SoCs.” CX-0005C (Mulhern WS) at Q/A 97, 102. The sales allocation for 2015 is [], and the sales allocation for 2016 is []. *See* CX-0005C (Mulhern WS) at Q/A 104; *see also* CDX-0003C (Mulhern Demonstrative) at 7.

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A. Employment of Labor or Capital

Broadcom argues, in part:

Broadcom has significant investments in labor in the United States relating to the DI Products. These investments include employee costs such as salary, bonus, fringe benefits, and payroll taxes. CX-0001C (Aberle WS) at Q/A 34. Broadcom's investments in its R&D employees are properly considered under 19 U.S.C. § 1337(a)(3)(B). *See Certain Digital Video Receivers and Hardware and Software Components Thereof*, Inv. No. 337-TA-1001, I.D. at *580 (June 27, 2017) (holding that labor expenses relating to R&D were significant and appropriate under subsection (B)).

Broadcom Br. at 291.

With respect to labor and capital, respondents' entire argument is:

Complainant's labor investments rely primarily on R&D. *See* CDX-0003.006. Each of those claimed investments should be excluded. CX-0548C. Complainant's allocations should further be limited to products actually under development. Properly allocating Complainant's investments reduces them to less than [] U.S. dollars. CX-0546C, CX-0548C, CX-1354C; RDX-1089; Tr. (Mulhern) 93:19-94:8. Compared to Complainant's investments of [] in labor, a dubious investment of [] is not significant.

Resps. Br. at 297. In reply, respondents' entire argument for subsections (a)(3)(A) and (a)(3)(B) is:

Complainant also improperly tries to claim research and development investments under statutory subsections (A) (plant and equipment) and (B) (labor or capital). 19 U.S.C. § 1337(a)(3). That, however, renders the provision allowing investments under research and development surplusage—Complainant identifies no investments under (C) that it does not try to claim under (A) or (B). RPostHg. Br. at 295; Tr. (Mulhern) 96:3-97:4; RDX-1091[C.]

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Resps. Reply at 99. Thus, respondents have not presented any expert supporting their position, and they have not cited to any of their own exhibits in support of their arguments.⁷³

The administrative law judge has determined that Broadcom has satisfied the domestic industry requirement under § 337(a)(3)(B).

In 2015 and 2016, Broadcom employed [] engineers who were involved with R&D activities related to the DI products (e.g., cable, satellite, and IP SoCs). CX-0001C (Aberle WS) at Q/A 33; CX-0005C (Mulhern WS) at Q/A 86; CX-0544C. Broadcom invested approximately [] in the United States in fiscal year 2015 and fiscal year 2016, respectively, associated with the R&D engineers dedicated to the DI Product Lines. CX-0001C (Aberle WS) at Q/A 33; CX-0005C (Mulhern WS) at Q/A 89; CX-0544C (Broadcom Labor Investments); CX-0178C (Broadcom Operating Expenses). When Broadcom's sales allocation is applied to these figures, Broadcom's investments in the R&D engineers in the United States dedicated to the DI Products is [] in fiscal year 2015 and [] in fiscal year 2016. CX-0005C (Mulhern WS) at Q/A 82; CX-0544C.⁷⁴

⁷³ RDX-1091C is a demonstrative created during Ms. Mulhern's cross-examination.

⁷⁴ There is a basis for Broadcom's use of sales allocations to determine how much of Broadcom's investment is related to the asserted patents and the DI products. *See Certain Laminated Floor Panels*, Inv. No. 337-TA-545, Order No. 17 at 4 (Mar. 2, 2006) (using "an allocation based on percentages of sales revenues") (not reviewed per Commission Notice (EDIS Doc. ID No. 251615)); *Certain Silicon Microphone Packages and Products Containing Same*, Inv. No. 337-TA-888, Order No. 47 at 12, (May 8, 2014) (finding a domestic industry after evaluating an "allocation of investments based on relative percentages from sales figures") (not reviewed per Commission Notice (EDIS Doc. ID No. 535361)); CX-0005C (Mulhern WS) at Q/A 98 (opining that a sales-based allocation is appropriate because "In general, a sales-based allocation approach allocates total costs in proportion to product sales. This means that higher selling products are assigned a higher proportion of total costs. An advantage of a sales-based allocation approach is that it captures the importance of the DI Products relative to Broadcom's other STB SoC products.").

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In addition, in 2106, Broadcom employed [] product-line engineers, who develop and commercialize Broadcom SoCs. CX-0001C (Aberle WS) at Q/A 36-37. Broadcom spent [] in compensating the product-line engineers in 2016. *Id.* at Q/A 37. When Broadcom's sales allocation is applied to these figures, Broadcom's investments in the United States in the Product Line engineers dedicated to the DI Products is [] in fiscal year 2015 and [] in fiscal year 2016. CX-0005C (Mulhern WS) at Q/A 82; CX-0544C.

The administrative law judge has determined that the R&D engineering and the product-line engineering employment figures relied on by Broadcom are significant under § 337(a)(3)(B). In particular, the number of R&D engineering and the product-line engineering employees, along with their relatively high compensation (on average), are significant. *See* CX-0005C (Mulhern WS) at Q/A 136 (“from a quantitative perspective, Broadcom's U.S. investments in R&D and testing activities are significant in absolute terms and account for a substantial proportion of total worldwide investments in such activities.”), Q/A 138 (“U.S. expenses on R&D and testing activities accounted for approximately [] percent of Broadcom's total worldwide expenses for these activities”). Further, the activities of Broadcom's employees adds considerable value to the DI products. *Id.* at Q/A 136 (“Broadcom's U.S. R&D and testing activities include the development of product designs and Architecture, hardware and software development, integration activities to ensure the SoCs function properly in the overall STB, as well as testing, validation and quality control activities”). Thus, Broadcom's investment in its employees—for the R&D engineering and product-line engineers, whether analyzed jointly or separately—is quantitatively and qualitatively significant. *See Lelo Inc. v. Int'l Trade Comm'n*, 786 F.3d 879, 883 (Fed. Cir. 2015) (“The plain text of § 337 requires a quantitative analysis in determining whether a

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[complainant] has demonstrated a ‘significant investment in plant and equipment’ or ‘significant employment of labor or capital.’”).

B. Investment in Plant and Equipment

Broadcom argues, in part:

Broadcom’s investments in plant and equipment related to its DI Products are also significant. . . . In fiscal year 2015, Broadcom allocated [] in facility expenses to the STB Division in the United States. . . . In fiscal year 2016, Broadcom allocated [] in facility expenses to the STB Division in the United States. . . . Using the sales allocation method described above, Broadcom invested [] in real estate in the United States dedicated to the DI Products in fiscal years 2015 and 2016, respectively. CX-0005C (Mulhern WS) at Q/A 131; CDX-0003C.0008 (Mulhern Demonstratives)[.]

In fiscal year 2015 and 2016, Broadcom also invested in equipment for the DI Product lines. Specifically, Broadcom incurred costs relating to the depreciation of equipment and other equipment expenses including prototyping costs (which are related to the masks used to produce the SoCs), hardware and software used in the design of the SoCs, and manufacturing expenses (which are the costs associated with the testing and verification activities performed by the engineers). . . . Using the sales allocation described above, in fiscal year 2015, Broadcom invested [] in the United States in technical equipment and other operating expenses, respectively, dedicated to the DI Products. . . . Using the sales allocation above, in fiscal year 2016, Broadcom invested [] in the United States in technical equipment and other operating expenses, respectively, dedicated to the DI Products. . . .

Broadcom Br. at 293.

Respondents’ entire argument is:

Complainant’s labor investments rely primarily on R&D. *See* CDX-0003.006. Each of those claimed investments should be excluded. CX-0548C. Complainant’s allocations should further be limited to products actually under development. Properly allocating Complainant’s investments reduces them to less than four million U.S. dollars. CX-0546C, CX-0548C, CX-1354C; RDX-1089; Tr. (Mulhern) 93:19-94:8. Compared to

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Complainant's investments of [] in labor, a dubious investment of [] is not significant.

Resps. Br. at 297. In reply, respondents' entire argument for subsections (a)(3)(A) and (a)(3)(B) is:

Complainant also improperly tries to claim research and development investments under statutory subsections (A) (plant and equipment) and (B) (labor or capital). 19 U.S.C. § 1337(a)(3). That, however, renders the provision allowing investments under research and development surplusage—Complainant identifies no investments under (C) that it does not try to claim under (A) or (B). RPostHg. Br. at 295; Tr. (Mulhern) 96:3-97:4; RDX-1091[C.]

Resps. Reply at 99. Thus, respondents have not presented any expert supporting their position, and they have not cited to any of their own exhibits in support of their arguments.⁷⁵

The administrative law judge has determined that Broadcom has satisfied the domestic industry requirement under § 337(a)(3)(A).

Broadcom's investments in plant and equipment include facility expenses and office expenses. CX-0001C (Aberle WS) at Q/A 41, 46-49. Broadcom utilizes approximately [] square feet for domestic R&D related to the STB Division. *Id.* at Q/A 40, 52 (Broadcom has "main" facilities in Irvine, California; San Jose, California; Santa Clara, California; and Andover, Massachusetts). The allocation of Broadcom's global real estate for the R&D and testing activities within the STB Division (inclusive of the cable modem products) was [] for 2015 and [] for 2016. *Id.* at Q/A 41; *see also* CX-0005C (Mulhern WS) at Q/A 116.⁷⁶

⁷⁵ RDX-1091C is a demonstrative created during Ms. Mulhern's cross examination.

⁷⁶ The monetary allocation dropped in 2016 due to Avago's acquisition of Broadcom. CX-0001C (Aberle WS) at Q/a 42.

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For equipment, Broadcom's Divisional Finance Controller, Mr. Aberle, explained that Broadcom's equipment costs for the STB division include "operating expenses associated with a variety of technical equipment" such as "emulators testing equipment verification equipment design workstations servers and other lab consumables." CX-0001 (Aberle WS) at Q/A 43. Typical costs include "depreciation repairs maintenance and equipment rental testing and lab expenses." *Id.* at Q/A 44. Additional expenses include "communications; [] hardware; [] software; IT maintenance and supplies; manufacturing expense office supplies, furniture, and equipment; outsourced engineering; prototyping costs; and workstation hardware." *Id.* at Q/A 46. In 2015, after applying the sales allocation, Broadcom invested [

] in the United States in technical equipment and other operating expenses, respectively, dedicated to the DI Products. CX-0005C (Mulhern WS) at Q/A 121, 127; CX-0549C (Broadcom R&D, Plant, Equipment Expenses); CX-0550C (Broadcom Allocation); CX-0178C (Broadcom Operating Expenses); CDX-0003C.0008 (Mulhern Demonstratives). The corresponding investments for 2016 were []. *Id.*

The administrative law judge has determined that the facility and equipment expenses relied upon by Broadcom are significant under § 337(a)(3)(A). In particular, the physical outlay of the facility ([] square feet) is large, and the [] in expenses (which has been apportioned to the STB division by overall headcount relative to Broadcom as a whole) for real estate for 2015-2016 is a significant investment. *See* CX-0005C (Mulhern WS) at Q/A 115-16; *see also Certain Air Mattress Systems, Components Thereof and Methods of using the Same*, Inv. No. 337-TA-971, Comm'n Op. at 45 (May 17, 2017) (finding investments in plant and equipment were significant where the "record shows that all of the investments relied on by Complainants are made with respect to the articles protected by the patent[.]"). The expense is

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also significant insofar as the facilities are a key part in designing and developing products. *See* CX-0001 (Aberle WS) at Q/A 32, 36, 43-49. Further, Broadcom's equipment expenses ([] and operating expenses ([])) for 2015-2016 are significant monetary investments; the expenses are also necessary for designing and developing products. *Id.*; *see also Certain Air Mattress Systems, supra*. Thus, Broadcom's investments in plant and equipment are significant both quantitatively and qualitatively.

C. Investment in Engineering and Research and Development

Broadcom argues prong (C) of the domestic industry requirement in the alternative:

To the extent the ALJ finds that Broadcom's investments are not properly under 19 U.S.C. § 1337(a)(3)(A) and (B), these investments can be considered under 19 U.S.C. § 1337(a)(3)(C), as they relate to the R&D of Broadcom's DI Products. 19 U.S.C. § 1337(a)(3)(C). There is a nexus between Broadcom's investments into its DI Products and the Asserted Patents. Specifically, the functionalities in the Asserted Patents relate to core technologies incorporated into the DI Products. CX-0002C (Hellman WS) at Q/A 15, 107. For example, the video decoder is one of the most complicated portions of the SoC. CX-0002C (Hellman WS) at Q/A 15. Additionally, the graphics and display processing functions are critical in order to meet customer demands for performance. *Id.* Given the complicated nature of and the core functionality of the features covered by the Asserted Patents, a nexus exists between Broadcom's investments into the DI Products and the Asserted Patents. *Certain Integrated Circuit Chips And Prods. Containing The Same*, Inv. No. 337-TA-859, Comm'n Op. at *39 (Aug. 22, 2014) ("To the extent that the Patented technology arises from endeavors in the United States, such a nexus would ordinarily exist. But engineering and research and development investments—particularly engineering and development investments—need not end there. 'Exploitation' is a generally broad term that encompasses activities such as efforts to improve, develop, or otherwise take advantage of the asserted Patent.").

Broadcom's investments in the United States in labor for the DI Products are much more significant and substantial than Broadcom's investments in labor outside of the United States for the DI Products. For example, nearly [] of Broadcom's total

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investments in its R&D engineering engineers are directed to activities and personnel in the United States. . . . Over [] of Broadcom's total investments in its Product Line engineers are directed to activities and personnel in the United States. . . .

While Broadcom's R&D activities generally occur early in the lifecycle of a product, the investments Broadcom made in 2015 and 2016 are appropriate to consider because Broadcom's future products will also be covered by the Asserted Patents, and the ratio of DI products to other products in Broadcom's DI Product Lines is expected to be the same in the future. . . .

Broadcom Br. at 295-96.

Respondents' entire argument is two sentences:

Complainant never shows a nexus between its alleged investments and the claimed features, which is a prerequisite for any domestic industry under 19 U.S.C. § 1337(a)(3)(C). It does not appear that Complainant relies on exploitation of the patented features (*see* CX-0005C, CX-0001C), and Complainant's evidence fails to support such an allegation.

Resps. Br. at 297. In reply, respondents' entire argument is:

Finally, Complainant offers no evidence of a nexus between its alleged domestic industry products and the asserted patents. CPostHg. Br. at 295-96. Complainant instead declares, without evidence or expert support, that the claimed features are important to the products and, ergo, a nexus exists. *Id.* at 295. Complainant similarly argues without evidence or expert analysis that Broadcom must be continuing to conduct research and development into the claimed features. *Id.* at 296. Complainant was required to show any nexus and any continuing activity. It failed to do so.

Resps. Reply at 99. Thus, respondents have not presented any expert supporting their position, have not cited to any exhibits, and do not cite any precedent in support of their arguments.

In *Certain Integrated Circuit Chips and Products Containing the Same*, the Commission explained that:

[T]he complainant must establish that there is a nexus between the claimed investment and the asserted patent, regardless of whether

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the domestic-industry showing is based on licensing, engineering, or research and development.

... To the extent that the patented technology arises from endeavors in the United States, such a nexus would ordinarily exist.

Inv. No. 337-TA-859, Comm'n Op. at 38-39 (Aug. 22, 2014) (footnote omitted). The

Commission also added:

For subparagraphs (a)(3)(A) and (B), we would only examine whether Realtek's "investment in plant and equipment" or "employment of labor or capital" relates to protected articles. This opinion does not change any analysis to be conducted under subparagraphs(a)(3)(A) or (B). As Realtek has expressly abandoned any arguments pertaining to these subparagraphs, we do not address them. For subparagraph (C), however, as discussed above, a domestic industry "with respect to" articles is necessary, but there is an additional requirement that the investment constitutes an exploitation of the asserted patent.

Id. at 48.

The administrative law judge previously found that Broadcom satisfied the domestic industry requirement under (a)(3)(A) and (a)(3)(B). *See* §§ VII(A)-(B), *supra*. However, the administrative law judge does not rule in the alternative that Broadcom could satisfy the domestic industry requirement with respect to subsection (a)(3)(C). In particular, Broadcom has not presented a separate analysis of the substantiality of its investments. Indeed, most of Broadcom's arguments for subsection (a)(3)(C) are blended with its arguments for (a)(3)(A) and (a)(3)(B). Accordingly, the administrative law judge does not make an alternative finding that Broadcom would satisfies subsection (a)(3)(C).

* * *

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VIII. CONCLUSIONS OF FACT AND LAW

Jurisdiction

- 1) The Commission has personal jurisdiction in this investigation.
- 2) The Commission has subject matter jurisdiction in this investigation.
- 3) The Commission has *in rem* jurisdiction in this investigation.
- 4) Sigma is an importer of the accused products.
- 5) VIZIO is an importer of the accused products.

Representative Products

- 6) Sigma's [].
- 7) VIZIO products [] are representative of VIZIO products.
- 8) The [] is representative of Broadcom's DI products.

U.S. Patent No. 7,310,104

- 9) Broadcom has not shown that Sigma's SX-6 SoC infringes the asserted claims.
- 10) Broadcom has not shown that VIZIO products [] infringe the asserted claims.
- 11) Broadcom has not shown that the [] practices claims 1-6 and 9-22.
- 12) Respondents have not shown, through clear and convincing evidence, that the asserted claims are invalid under 35 U.S.C. §§ 102 or 103.
- 13) Respondents have not shown, through clear and convincing evidence, that the asserted claims are invalid under 35 U.S.C. § 112.

U.S. Patent No. 8,284,844

- 14) Broadcom has not shown that Sigma's SX-6 SoC infringes the asserted claims.
- 15) Broadcom has not shown that VIZIO products [] infringe the asserted claims.
- 16) The [] practices claims 1-13, thus satisfying the domestic industry's technical prong requirement.

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- 17) Respondents have shown, through clear and convincing evidence, that Reader anticipates claims 1, 2 and 5-9.
- 18) Respondents have shown, through clear and convincing evidence, that Fandrianto anticipates claims 1-10.
- 19) Respondents have not shown, through clear and convincing evidence, that Diaz, Bakhmutsky, or the Quasar Chips anticipate the asserted claims.
- 20) Respondents have not shown, through clear and convincing evidence, that the asserted claims are invalid under 35 U.S.C. § 103.

U.S. Patent No. 7,590,059

- 21) Broadcom has not shown that Sigma's SX-6 SoC infringes the asserted claims.
- 22) Broadcom has not shown that VIZIO products [] infringe the asserted claims.
- 23) The [] practices claims 11-20, thus satisfying the domestic industry's technical prong requirement.
- 24) Respondents have not shown that the asserted claims are patent-ineligible under 35 U.S.C. § 101.
- 25) Respondents have not shown, through clear and convincing evidence, that the asserted claims are invalid under 35 U.S.C. §§ 102 or 103.
- 26) Respondents have not shown, through clear and convincing evidence, that the asserted claims are invalid under 35 U.S.C. § 112.

Domestic Industry

- 27) The domestic industry's economic prong requirement has been satisfied under § 337(a)(3)(A), as there is a significant investment in plant and equipment with respect to the Broadcom articles protected by U.S. Patent Nos. 8,284,844 and 7,590,059 (and U.S. Patent No. 7,310,104 if it is later found that the [] practices a claim from this patent).
- 28) The domestic industry's economic prong requirement has been satisfied under § 337(a)(3)(B), as there is a significant employment of labor or capital with respect to the Broadcom articles protected by U.S. Patent Nos. 8,284,844 and 7,590,059 (and U.S. Patent No. 7,310,104 if it is later found that the [] practices a claim from this patent).

IX. ORDER CONCERNING PUBLIC VERSION

To expedite service of the public version, the parties are hereby ordered to file with the

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Commission Secretary no later than May 29, 2018, a jointly marked copy of this initial determination that includes bold, red brackets to show any portion considered by the parties (or their suppliers of information) to be confidential. The parties shall simultaneously file a joint list indicating each page on which such a bracket is to be found and which party contends the corresponding information is confidential. At least one copy of such a filing shall be served upon the office of the undersigned, and the brackets shall be formatted in bold, red text. If a party (including any supplier of information) considers nothing in the initial determination to be confidential, and thus makes no request that any portion be redacted from the public version, then a statement to that effect shall be filed.

X. INITIAL DETERMINATION ON VIOLATION

Accordingly, it is the initial determination of the undersigned that no violation of section 337 (19 U.S.C. § 1337) has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products containing the same.

Further, this initial determination, together with the record of the hearing in this investigation consisting of (1) the transcript of the hearing, with appropriate corrections as may hereafter be ordered, and (2) the exhibits received into evidence in this investigation, is hereby certified to the Commission.

In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential by the undersigned under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this initial determination upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order, as amended, issued in this investigation.

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Pursuant to 19 C.F.R. § 210.42(h), this initial determination shall become the determination of the Commission unless a party files a petition for review pursuant to § 210.43(a) or the Commission, pursuant to § 210.44, orders on its own motion a review of the initial determination or certain issues herein.

A handwritten signature in black ink, appearing to read 'D. Shaw', is written over a horizontal line.

David P. Shaw
Administrative Law Judge

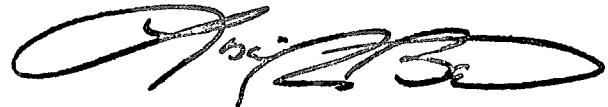
Issued: May 11, 2018

**CERTAIN SEMICONDUCTOR DEVICES AND CONSUMER AUDIOVISUAL
PRODUCTS CONTAINING THE SAME**

INV. NO. 337-TA-1047

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **INITIAL DETERMINATION** has been served upon the following parties as indicated, on JUN 12 2018.



Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT BROADCOM CORP.:	
John M. Caracappa, Esq. STEPTOE & JOHNSON LLP 1330 Connecticut Avenue, NW	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____
FOR RESPONDENT SIGMA DESIGNS, INC.:	
Kecia J. Reynolds, Esq. PILLSBURY WINTHROP SHAW PITTMAN LLP 1200 Seventeenth St. NW Washington, DC 20036	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____
FOR RESPONDENT VIZIO, INC.:	
Cono A. Carrano, Esq. AKIN GUMP STRAUSS HAUER & FELD LLP Robert S. Strauss Building 1333 New Hampshire Avenue, N.W. Washington, DC 20036-1564	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____

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**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

In the Matter of

**CERTAIN SEMICONDUCTOR
DEVICES AND CONSUMER
AUDIOVISUAL PRODUCTS
CONTAINING THE SAME**

Inv. No. 337-TA-1047

RECOMMENDED DETERMINATION ON REMEDY AND BONDING

Administrative Law Judge David P. Shaw

Pursuant to the notice of investigation, 82 Fed. Reg. 17688 (Apr. 12, 2017), this is the recommended determination on remedy and bonding in Certain Semiconductor Devices and Consumer Audiovisual Products Containing the Same, United States International Trade Commission Investigation No. 337-TA-1047.

For the reasons stated herein, the administrative law judge recommends that if the Commission finds a violation of section 337 in this investigation, it should (1) issue a limited exclusion order covering products that infringe the patent claims as to which a violation of section 337 has been found; (2) issue a cease and desist order; and (3) require a bond in the amount of [] during the Presidential review period.

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I. PROCEDURAL BACKGROUND

On March 7, 2017, complainant Broadcom Corporation filed a complaint alleging that multiple respondents unlawfully import certain semiconductor devices and consumer audiovisual products containing the same, including, without limitation, certain system-on-chip (“SoC”) and similar processing components and circuits used in digital televisions and other consumer audiovisual products. Compl., ¶ 1. The complaint asserted the following five patents: U.S. Patent No. 8,284,844 (the “‘844 Patent”); U.S. Patent No. 7,590,059 (the “‘059 Patent”); U.S. Patent No. 8,068,171; U.S. Patent No. 7,310,104 (the “‘104 Patent”); and U.S. Patent No. 7,342,967. *Id.*

By publication of a notice in the Federal Register, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted this investigation to determine:

[W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor devices and consumer audiovisual products containing the same by reason of infringement of one or more of claims 1–14 of the ‘844 patent; claims 11–30 of the ‘059 patent; claims 1–5 and 7 of the ‘171 patent; claims 1, 10, 11, 16, 17 and 22 of the ‘104 patent; and claims 1–4 of the ‘967 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337[.]

82 Fed. Reg. 17688 (April 12, 2017). The Commission did not direct the administrative law judge to take evidence, information, or argument regarding the public interest in this investigation. *See id.*

The Commission named Broadcom Corporation as complainant. *Id.* The Commission named the following companies as respondents: Funai Electric Company, Ltd., Funai Corporation, Inc., and P&F USA, Inc. (collectively, the “Funai respondents”); MediaTek Inc.,

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MediaTek USA Inc., and MStar Semiconductor Inc. (collectively, the “MediaTek and MStar respondents”); LG Electronics Inc. and LG Electronics U.S.A., Inc. (collectively, the “LG respondents”); Sigma Designs, Inc. (“Sigma”); and Vizio, Inc. (“VIZIO”). *Id.* The Office of Unfair Import Investigations did not participate as a party in the investigation. *Id.*

During the pre-hearing phase of this investigation, the administrative law judge issued unreviewed initial determinations granting Broadcom motions to terminate the investigation as to certain claims and patents. *See* Initial Determination, § I(C). By the time post-hearing briefs were filed, only claims of the ‘104, ‘844, and ‘059 Patents remained at issue. *Id.* Additionally, the administrative law judge issued unreviewed initial determinations terminating the Funai respondents, the LG respondents, and the MediaTek and Mstar respondents, thus leaving Sigma and VIZIO as the remaining respondents with respect to the final initial determination. *Id.*

On May 11, 2018, the administrative law judge issued the final initial determination in this investigation, finding that no violation of section 337 of the Tariff Act, as amended, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation, of certain semiconductor devices and consumer audiovisual products containing the same.

The Commission Rules provide that subsequent to issuing an initial determination on the question of violation of section 337, the administrative law judge shall issue a recommended determination containing findings of fact and recommendations concerning: (1) the appropriate remedy in the event that the Commission finds a violation of section 337; and (2) the amount of the bond to be posted by the respondents during Presidential review of Commission action under section 337(j). 19 C.F.R. § 210.42(a)(1)(ii).

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II. LIMITED EXCLUSION ORDER

A. General Law Relating to Limited Exclusion Orders

The Commission has broad discretion in selecting the form, scope, and extent of the remedy in a section 337 proceeding. *Viscofan, S.A. v. Int'l Trade Comm'n*, 787 F.2d 544, 548 (Fed. Cir. 1986). A limited exclusion order (or “LEO”) directed to respondents’ infringing products is among the remedies that the Commission may impose. Indeed, upon finding a violation of section 337, the statute provides that the Commission “shall direct that the articles concerned, imported by any person violating the provision of this section, be excluded from entry into the United States, unless, after considering the effect of such exclusion upon the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers, it finds that such articles should not be excluded from entry.” 19 U.S.C. § 1337(d)(1); *see Certain Automated Teller Machines, ATM Modules, Components Thereof, and Products Containing the Same*, Inv. No. 337-TA-972, Comm’n Op. at 28 (May 19, 2017) (“*Automated Teller Machines*”); *Spansion, Inc. v. Int'l Trade Comm'n*, 629 F.3d 1331, 1359-60 (Fed. Cir. 2010).

B. The Parties’ Arguments

Broadcom’s entire argument is:

Where a violation of Section 337 is found, the Commission may issue either a limited exclusion order, directed against products imported by persons found in violation, or a general exclusion order directed against all infringing products. 19 U.S.C. § 1337(d); *see also Certain Automated Teller Machines, ATM Modules, Components Thereof, and Prods. Containing the Same*, Inv. No. 337-TA-972, Comm’n Op. at 28 (May 19, 2017); *Spansion, Inc. v. Int'l Trade Comm'n*, 629 F.3d 1331, 1359-60 (Fed. Cir. 2010). Should a violation of Section 337 be found in this Investigation, the appropriate remedy is a limited exclusion order that covers each Respondent’s products that infringe one or more claims of the Asserted Patents.

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Broadcom Br. at 297.

Respondents' entire argument is:

Complainant fails to show a violation. Consequently, Complainant is not entitled to any relief. If the Commission reaches a contrary conclusion, to avoid restricting legitimate trade, any remedy should be a limited exclusion order limited to (1) the specific parties who import into the U.S., sell for importation into the U.S., or sell within the U.S. the specific products and models found to infringe the asserted claims of the asserted patents. Any limited exclusion order should also include an exception to allow for each Respondent to continue service and repair for any products already sold to consumers before the effective date of any order that might issue.

Further, no potential exclusion order should cover any VIZIO future products that may contain a []. No current or past VIZIO product uses an [] and no potential future VIZIO product is currently expected to use either SoC. RX1086C.0007. Mr. Hwang testified that no [] has ever been provided to VIZIO in the United States for any purpose, including testing. *Id.*

The VIZIO [] should also be outside the scope of any exclusion order. The [] did not enter the United States for any purpose, including testing, prior to the close of the evidentiary record. RX1086C.0008. Further, VIZIO canceled its planned [] model entirely. *Id.*

Finally, Broadcom did not present any evidence regarding the [] SoC and neither SoC is identified in the parties' Joint Stipulation of Representative Products as being represented by any other SoC. Accordingly, Broadcom has failed to present any evidence that VIZIO products containing [] infringes any of the asserted claims and VIZIO products containing [] should be exempt from any exclusion order.

Resps. Br. at 298-88.

Broadcom replies:

Respondents argue that any exclusion order should not include the [], which is set to use a

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[]. RPostHB at 298. However, Respondents did not advance these arguments in their Pre-hearing Brief. Pursuant to Ground Rule 7, therefore, they have waived any argument as to whether or not the [] are properly covered by an exclusion order. *See* RPreHB at 397-398.

Further, Respondents admit that the [] is representative of the []. RPostHB at 308. The evidence shows that the [] infringes the Asserted Patents, and thus, the [] also infringes the Asserted Patents. CPostHB at 27-62, 160-171, 247-254. . . . If a violation is found, the [] and any products incorporating the [] should be included in any exclusion order that issues.

Broadcom Reply at 98-99 (footnotes and general legal principles omitted).

Respondents' entire reply concerning remedy and bond follows:

Respondents addressed the issues of Remedy and Bond in their Posthearing Brief, and Complainant's Posthearing Brief raises no new issues. Although the Commission should find no violation based on the evidentiary record, the Respondents will submit any additional briefing regarding Remedy and Bond if directed to do so by the Commission.

Resps. Reply at 100.

C. Recommendation Concerning Limited Exclusion Order

The administrative law judge recommends that if the Commission finds a violation of section 337, and subject to the Commission's public interest determination, the Commission should issue a limited exclusion order covering all of the infringing articles imported, sold for importation, or sold after importation by respondents. The administrative law judge recommends that the limited exclusion order should apply to respondents' affiliated companies, parents, subsidiaries or other related business entities, or their successors or assigns.

The administrative law judge finds that the limited exclusion order would cover at least

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all products including a []¹ The administrative law judge declines to make any explicit recommendations concerning VIZIO's future products, products that are not imported into the United States, cancelled products, products that were not adjudicated during the investigation, or the [] identified in respondents' brief).²

Further, the administrative law judge recommends that the Commission should not permit a limited service-and-repair exception. Respondents have not described what service and repair activities they perform or explained why an exception to an exclusion order is necessary to perform those activities.

III. CEASE AND DESIST ORDER

A. General Law Relating to Cease and Desist Orders

Section 337 provides that in addition to, or in lieu of, the issuance of an exclusion order, the Commission may issue a cease and desist order as a remedy for a violation of section 337. 19 U.S.C. § 1337(f)(1). The Commission generally issues cease and desist orders "when, with respect to the imported infringing products, respondents maintain commercially significant inventories in the United States or have significant domestic operations that could undercut the remedy provided by an exclusion order." *Automated Teller Machines*, Inv. No. 337-TA-972, Comm'n Op. at 28; *see, e.g., Certain Table Saws Incorporating Active Injury Mitigation Technology and Components Thereof*, Inv. No. 337-TA-965, Comm'n Op. at 4-6 (Feb. 1, 2017);

¹ On September 1, 2017, Broadcom, Sigma, and VIZIO filed a stipulation that states: "[]." Supplement to Joint Stipulation regarding Identification of Representative Products (EDIS Doc. ID No. 621949) at 4. In the same document, VIZIO stated: "Regarding VIZIO audiovisual products containing Sigma, MediaTek or MStar SoCs, VIZIO defers to Sigma's, MediaTek's and MStar's designation of representative SoCs." *Id.*

² Respondents have not requested a certification provision.

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Certain Protective Cases and Components Thereof, Inv. No. 337-TA-780, Comm’n Op. at 28 (Nov. 19, 2012) (citing *Certain Laser Bar Code Scanners and Scan Engines, Components Thereof and Products Containing Same*, Inv. No. 337-TA-551, Comm’n Op. at 22 (June 14, 2007)).³

B. The Parties’ Arguments

With respect to VIZIO, Broadcom argues that the Commission should issue a cease and desist order if a violation is found:

. . . VIZIO maintain[s] commercially significant inventory in the United States. . . .

As of July 7, 2017, VIZIO stipulated that it had [] of Accused Products in inventory in the United States. JX-0010C (Broadcom/VIZIO Stipulation); CX-0005C (Mulhern WS) at Q/A 153; CDX-0003C.012 (Mulhern Demonstratives); CX-0542C (VIZIO Dollar Sales); CX-0516C (Jerney Depo Designations) at 92; CX-0541C (VIZIO Unit Sales); CX-0558C (VIZIO Inventory); CX-0195C (VIZIO Sales). VIZIO’s Senior Finance Manager, Mr. Jerney, testified that in addition to the inventory listed in the stipulation (JX-0010C), additional inventory of VIZIO-branded products is held in [

] CX-0005C (Mulhern WS) at Q/A 156; CX-0516C (Jerney Dep. Tr.) at 91:5 – 92:22. Mr. Hwang, VIZIO’s Senior Direct of Product Management testified that [

] CX-0005C (Mulhern WS) at Q/A 157; CX-0517C (Hwang Dep. Tr.) at 119:13 – 120:12, 137:3 – 139:13, 140:2 – 141:17. The estimated quantity of Accused VIZIO Products in VIZIO’s warehouses is [

] CX-0005C (Mulhern WS) at Q/A 159; CDX-

³ Some commissioners have adopted different approaches to analyzing when it is appropriate to issue cease and desist orders, particularly with respect to the question of whether a commercially significant inventory is a prerequisite for obtaining a cease and desist order. *See Certain Network Devices, Related Software and Components Thereof (II)*, Inv. No. 337-TA-945, Comm’n Op. at 126 n.74 (June 1, 2017) (“*Network Devices (II)*”); *Automated Teller Machines*, Inv. No. 337-TA-972, Comm’n Op. at 28 n.19.

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0003C.012 (Mulhern Demonstratives); CX-541C (VIZIO Unit Sales); CX-0542C (VIZIO Dollar Sales); CX-0558C (VIZIO Inventory); CX-0195C (VIZIO Sales). Because [

]. Alternatively, [

] that could undercut the remedy provided by an exclusion order, justifying the issuance of a cease and desist order.

Broadcom Br. at 298-99 (argument concerning LG omitted).

Respondents' entire argument is:

Complainant appears to seek cease-and-desist orders against only LG and VIZIO as Sigma maintains no domestic inventory. The Commission normally considers a commercially significant inventory a prerequisite to issuance of a cease-and-desist order. *Certain Integrated Repeaters*, Inv. No. 337-TA-435, Comm'n Op. on Remedy, the Public Interest, & Bonding at 27 (Aug. 16, 2002). Complainant, however, has not established that LG's or VIZIO's domestic inventory is significant. JX-0008C, JX-0010C. To the extent any cease-and-desist order issues, it should be limited to the specific products and models found to infringe.

Resps. Br. at 299.

C. Recommendation Concerning Cease and Desist Order

Having considered the parties' arguments, the administrative law judge recommends that the Commission issue a cease and desist order if a violation is found, subject to any public interest determination of the Commission. Specifically, the administrative law judge recommends that the Commission issue an order directing VIZIO to cease and desist from engaging in unfair acts related to this investigation.

In particular, a cease and desist order is warranted to prevent any circumvention of the Commission's exclusion order.⁴ The hearing concluded over six months ago; any inventory

⁴ To the extent necessary, the administrative law judge finds that VIZIO's on-hand inventory (as stipulated in JX-0010C) is commercially significant. *See* CX-0005C (Mulhern WS) at Q/A 152-

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beyond the stipulated units in inventory after the end of the hearing would likely have been used to support VIZIO's commercial operations. Likewise, any inventory imported and sold during the Presidential review period (or beyond) would also circumvent the exclusion order. Finally, VIZIO has not provided evidence of the service-and-repair services it does provide, nor has it sufficiently described the services it intends to provide.

IV. BOND

A. General Law Relating to Bond

Pursuant to section 337(j)(3), the administrative law judge and the Commission must determine the amount of bond to be required of a respondent, during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to issue a remedy. The purpose of the bond is to protect the complainant from any injury. 19 U.S.C. § 1337(j)(3); 19 C.F.R. §§ 210.42(a)(1)(ii), 210.50(a)(3).

When reliable price information is available, the Commission has often set bond by eliminating the differential between the domestic product and the imported, infringing product. *Certain Microsphere Adhesives, Processes for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. at 24 (1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *Network Devices (II)*, Inv. No. 337-TA-945, Comm'n Op. at 128; *Certain Integrated Circuit Telecommunication Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995). A 100 percent bond has been required when no effective alternative existed. *Automated*

59; see also CX-0541C (VIZIO Unit Sales); CX-0542C (VIZIO Dollar Sales); CX-0558C (VIZIO Inventory); CX-0195C (VIZIO Sales).

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Teller Machines, Inv. No. 337-TA-972, Comm'n Op. at 29-30; *Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997) (a 100% bond imposed when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be *de minimis* and without adequate support in the record).

B. The Parties' Arguments

Broadcom argues, in part:

A bond in the amount of [] should be imposed during the Presidential review period. Broadcom's SoCs are not directly competitive with the SoCs sold by LG and Sigma or incorporated in LG and VIZIO's audiovisual products. CX-0005C (Mulhern WS) at Q/A 163. Thus, a price comparison is not appropriate in this Investigation.

[]
[] CX-0530C to CX-0535C (Broadcom Licenses); CX-0561C (Broadcom/[] Licenses); CX-0005C (Mulhern WS) at Q/A 176. These licenses do not provide useful guidance on a reasonable royalty. CX-0005C (Mulhern WS) at Q/A 176. However, a reasonable royalty rate equal to the median royalty rate in the semiconductor industry ([]) is appropriate in this Investigation. CX-005C at Q/A 177-178; CX-0230 (Industry Standard Royalty Rate).

Alternatively, if the ALJ finds that [] is not appropriate, a bond of 100% should be imposed. *See, e.g., Certain Liquid Crystal Display Modules and Products Containing Same*, Inv. No. 337-TA-634, Final Initial and Recommended Determinations, 2009 WL 2418534 at *108 (June 12, 2009) (finding that reliable evidence of a price comparison and reasonable royalty were not available and imposing a 100% bond).

Broadcom Br. at 300.

Respondents' entire argument is:

The bond during the Presidential review period should be

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“sufficient to protect the complainant from any injury.” 19 U.S.C. § 1337(j)(3); 19 C.F.R. § 210.50. The burden is on Complainant to establish the need for any bond and its amount. *Certain Rubber Antidegradants, Components Thereof*, Inv. No. 337-TA-533, Comm’n Op. at 38-39 (Apr. 2008). Broadcom’s domestic industry products are a handful of SoCs, and Respondents do not import SoCs. Consequently Broadcom’s domestic industry cannot be harmed by the importation of non-competing products. Further, Complainant failed to show any injury from Respondents’ activities during any Presidential review period. Where Complainant has put forward no evidence demonstrating injury during the presidential review period, the Commission lacks authority under Section 337(j)(3) to impose any bond and should not impose one.

The Commission sets bond rates based on: (i) royalty rates complainants charged to licensees for the asserted patent or (ii) an average of the amounts by which infringing imports undersell complainants’ product, based on a percentage of the value of the imported product upon entry. *See, e.g., Certain Reclosable Plastic Bags & Tubing*, Inv. No. 337-TA-266, Comm’n Op. at 6 (1987); *Certain Acid Washed Denim Garments & Accessories*, Inv. No. 337-TA-324, Comm’n Op. at 27 (1992).

If the Commission sets a bond, it should be set at a percentage of the average SoC value. Complainant proposes a bond of [

], which is high for the industry.

Complainant also proposes a bond of the value of the accused SoC incorporated in an imported AV product, which would be impossible for Customs to police. A bond of [] on the average sales price of [] (CX-0383) and [] (CX-0348).

Because Complainant has not shown any harm, the ALJ should recommend zero bond.

Resps. Br. at 299-300.

In reply, Broadcom argues:

Without any support, Respondents suggest that Broadcom’s proposed bond of [] is too high for the industry. RPostHB at 300. Respondents’ conclusory and unsupported argument fails. Broadcom proposed a bond of [], which is the **standard**, median royalty rate for the semiconductor industry. CX-005C (Mulhern WS) at Q/A 177-78; CX-0230 (Industry Standard Royalty Rate). Where, as here, a price comparison is not possible,

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the Commission has used alternative approaches for calculating the bond, including a reasonable royalty. *See, e.g., Certain Integrated Circuit Telecomm. Chips and Prods. Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995). Because the accused products are semiconductor chips, and a price comparison is not possible, the standard, median industry royalty rate (*i.e.*, Broadcom's proposed bond rate) is appropriate in this Investigation.

Respondents also argue that a bond is not necessary because Broadcom and Respondents do not directly compete and Broadcom has not shown injury from Respondents' actions. RPostHB at 299. This argument is also without merit. The purpose of a bond is to protect the complainant from injury, and there is no requirement that the complainant and respondent be direct competitors. Indeed, the ITC has issued a bond in many different investigations where the complainant and respondent(s) do not directly compete. *See, e.g., Certain Baseband Processor Chips and Chipsets, Transmitter, and Receiver (Radio) Chips, Power Control Chips, and Prods. Containing Same, Including Cellular Tel. Handsets*, Inv. No. 337-TA-543, Comm'n Det., 2011 WL 6121182 at *80 (Oct. 2011); *Certain Wireless Comm'n Devices, Portable Music and Data Processing Devices, Computers and Components Thereof*, Inv. No. 337-TA-745, Recommended Det., 2012 WL 1881015 at *5 (May 9, 2012). Accordingly, a bond is appropriate.

Broadcom Reply at 99-100 (emphasis in original).

C. Recommendation Concerning Bond

Having considered the parties' arguments, the administrative law judge recommends that the Commission impose a bond of [] if a violation is found. Broadcom's economic expert explained that [] represents a reasonable royalty rate equal to the median royalty rate in the semiconductor industry. *See* CX-0005C (Mulhern WS) at Q/A 171-78. Although respondents identified and retained an economic expert who disagreed with Ms. Mulhern's opinions, respondents did not call their expert to testify at the hearing. *See id.* at Q/A 179-82; *see also* Rebuttal Expert Report of Thomas D. Vander Veen, Ph.D. (EDIS Doc. ID No. 624366); Respondents' Joint Identification

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of Expert Witnesses at 4 (EDIS Doc. ID No. 618628); Respondents' Pre-Hearing Statement (EDIS Doc. ID No. 629111) (Complainant's economics expert is the only economics expert listed); *see generally* Tr. (Dr. Vander Veen did not testify).

Accordingly, the administrative law judge finds that Broadcom has met its burden of showing that a bond is appropriate, and that a bond in the amount of [] is appropriate.

V. ORDER CONCERNING PUBLIC VERSION

To expedite service of the public version, each party is hereby ordered to file with the Commission Secretary no later than May 30, 2018, a copy of this recommended determination with brackets to show any portion considered by the party (or its suppliers of information) to be confidential, accompanied by a list indicating each page on which such a bracket is to be found.⁵ At least one copy of such a filing shall be served upon the office of the undersigned, and the brackets shall be marked in red. If a party (and its suppliers of information) considers nothing in the recommended determination to be confidential, and thus makes no request that any portion be redacted from the public version, then a statement to that effect shall be filed.

* * *

⁵ Confidential business information ("CBI") is defined in 19 C.F.R. § 201.6(a) and § 210.5(a). When redacting CBI or bracketing portions of documents to indicate CBI, a high level of care must be exercised in order to ensure that non-CBI portions are not redacted or indicated. Other than in extremely rare circumstances, block redaction and block-bracketing are prohibited. In most cases, redaction or bracketing of only discrete CBI words and phrases will be permitted.

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VII. RECOMMENDED DETERMINATION

Subject to any public interest determination of the Commission, the administrative law judge recommends that if the Commission finds a violation of section 337, it should: (1) issue a limited exclusion order covering products that infringe the patent claims as to which a violation of section 337 has been found; (2) issue a cease and desist order; and (3) require a bond in the amount of 3.9% of the value of the SoCs during the Presidential review period.

A handwritten signature in black ink, appearing to read 'D. Shaw', is positioned above a horizontal line.

David P. Shaw
Administrative Law Judge

Issued: May 23, 2018

**CERTAIN SEMICONDUCTOR DEVICES AND CONSUMER AUDIOVISUAL
PRODUCTS CONTAINING THE SAME**

INV. NO. 337-TA-1047

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **RECOMMENDED DETERMINATION**
has been served upon the following parties as indicated, on JUN 12 2018.



Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT BROADCOM CORP.:	
John M. Caracappa, Esq. STEPTOE & JOHNSON LLP 1330 Connecticut Avenue, NW	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____
FOR RESPONDENT SIGMA DESIGNS, INC.:	
Kecia J. Reynolds, Esq. PILLSBURY WINTHROP SHAW PITTMAN LLP 1200 Seventeenth St. NW Washington, DC 20036	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____
FOR RESPONDENT VIZIO, INC.:	
Cono A. Carrano, Esq. AKIN GUMP STRAUSS HAUER & FELD LLP Robert S. Strauss Building 1333 New Hampshire Avenue, N.W. Washington, DC 20036-1564	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Express Delivery <input type="checkbox"/> Via First Class Mail <input type="checkbox"/> Other: _____